19-5169; Rev 0; 4/10

EVALUATION KIT AVAILABLE

Stereo 2.4W Class D Amplifier

MAX98302

General Description

The MAX98302 stereo 2.4W Class D amplifier provides Class AB audio performance with Class D efficiency. This device offers five selectable gain settings (6dB, 9dB, 12dB, 15dB, and 18dB) set by a single gain-select input (GAIN).

Active emissions limiting, edge-rate, and overshoot control circuitry greatly reduces EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices. These features reduce application component count.

The MAX98302 industry-leading 1.65mA at 3.7V, 2.25mA at 5V, quiescent current extends battery life in portable applications.

The MAX98302 is available in a 14-pin TDFN-EP (3mm x 3mm x 0.75mm) package specified over the extended -40°C to +85°C temperature range.

Applications

Notebook and Netbook Computers
Cellular Phones
MP3 Players
Portable Audio Players
VoIP Phones

Features

- ♦ **Industry-Leading Quiescent Current: 1.65mA at 3.7V, 2.25mA at 5V**
- ♦ **Spread Spectrum and Active Emissions Limiting**
- ♦ **Five Selectable Gains**
- ♦ **High -67dB PSRR at 217Hz**
- ♦ **Click-and-Pop Suppression**
- ♦ **Thermal and Overcurrent Protection**
- ♦ **Low-Current Shutdown Mode**
- ♦ **Space-Saving, 3mm x 3mm x 0.75mm, 14-Pin TDFN-EP Package**

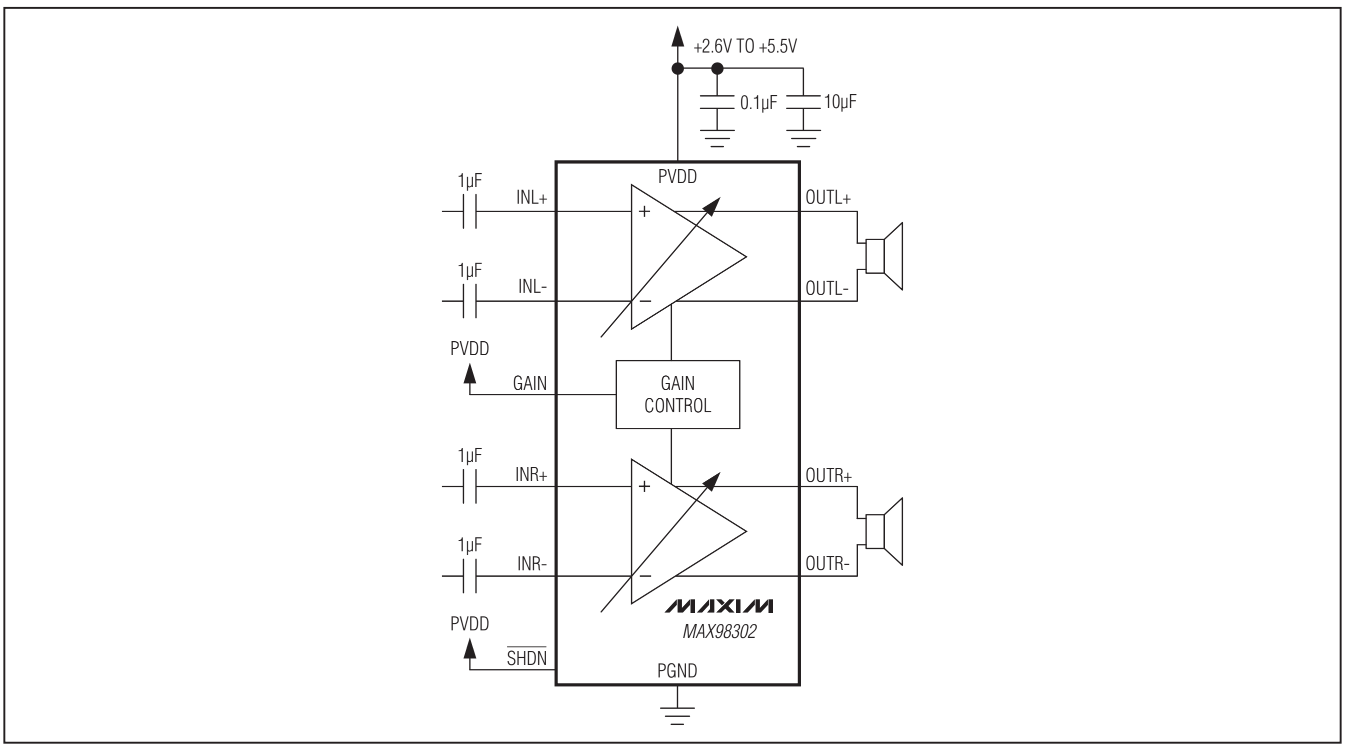
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX98302ETD+	-40°C to +85°C	14 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

PVDD to PGND.. -0.3V to 6V
All Other Pins to PGND ....-0.3V to (PVDD + 0.3V)
Continuous Current into PVDD, PGND,
OUTL_, OUTR_ .... ±600mA
Continuous Input Current (all other pins)........................ ±20mA
Duration of Short Circuit Between OUTL_,
OUTR_ to PVDD or PGND ....Continuous
Duration of Short Circuit Between OUTL+ to OUTL-,
OUTR+ to OUTR- ....Continuous
Continuous Power Dissipation for Single Layer Board (T_A = +70°C)
14-Pin TDFN (derate 18.5mW/°C above +70°C)....1481.5mW
14-Pin TDFN θ_{JA} (Note 1)...54°C/W
14-Pin TDFN θ_{JC} (Note 1)...8°C/W
Continuous Power Dissipation for Multilayer Board (T_A = +70°C)
14-Pin TDFN (derate 24.4mW/°C above +70°C)....1951.2mW
14-Pin TDFN θ_{JA} (Note 1)...41°C/W
14-Pin TDFN θ_{JC} (Note 1)...8°C/W
Junction Temperature ....+150°C
Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range............................ -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, AV = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLIFIER CHARACTERISTICS						
Supply Voltage Range	V_{PVDD}	Inferred from PSRR test	2.6		5.5	V
Undervoltage Lockout	UVLO				2.5	V
Quiescent Supply Current	I_{DD}	V_{PVDD} = 5.0V, T_A = +25°C		2.25	3.4	mA
		V_{PVDD} = 3.7V		1.65		
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V, T_A = +25°C		0.1	10	µA
Turn-On Time	t_{ON}			3.7	10	ms
Bias Voltage	V_{BIAS}			1.3		V
Voltage Gain	A_V	Connect GAIN to PGND	17.5	18	18.5	dB
		Connect GAIN to PGND through 100kΩ ±5% resistor	14.5	15	15.5	
		Connect GAIN to PVDD	11.5	12	12.5	
		Connect GAIN to PVDD through 100kΩ ±5% resistor	8.5	9	9.5	
		GAIN unconnected	5.5	6	6.5	
Input Resistance	R_{IN}	A_V = 18dB	14	20		kΩ
		A_V = 15dB	14	20		
		A_V = 12dB	14	20		
		A_V = 9dB	19	28		
		A_V = 6dB	26	40		
Output Offset Voltage	V_{OS}	T_A = +25°C (Note 4)		±4	±20	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, AV = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Click and Pop	K_{CP}	Peak voltage, A-weighted, 32/samples per second, R_L = 8Ω + 68µH (Notes 4, 5)	Into shutdown		-54		dBV
			Out of shutdown		-54		
Common-Mode Rejection Ratio	CMRR	f_{IN} = 1kHz, input referred			62		dB
Crosstalk		P_{OUT} = 300mW, R_L = 8Ω + 68µH	f = 1kHz		92		dB
			f = 10kHz		80		
Power-Supply Rejection Ratio (Note 4)	PSRR	V_{PVDD} = 2.6V to 5.5V, T_A = +25°C		50	67		dB
		V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω + 68µH	f = 217Hz		67		
			f = 1kHz		65		
			f = 10kHz		58		
Output Power	P_{OUT}	THD+N = 10%, f_{IN} = 1kHz	R_L = 4Ω + 33µH		2.4		W
			R_L = 8Ω + 68µH		1.6		
			R_L = 8Ω + 68µH, V_{PVDD} = 3.7V		0.87		
		THD+N = 1%, f_{IN} = 1kHz	R_L = 4Ω + 33µH		2		W
			R_L = 8Ω +68µH		1.25		
			R_L = 8Ω + 68µH, V_{PVDD} = 3.7V		0.68		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz	R_L = 4Ω + 33µH, V_{PVDD} = 1W		0.04		%
			R_L = 8Ω + 68µH P_{OUT} = 0.5W		0.04		
Oscillator Frequency	f_{OSC}				300		kHz
Spread-Spectrum Bandwidth					±7		kHz
Efficiency	η	THD+N = 1%, f = 1kHz, R_L = 8Ω + 68µH			83		%
Output Noise	V_N	A_V = 6dB, A weighted (Note 4)			50		µV_{RMS}
Output Current Limit	I_{LIM}				2		A
Thermal Shutdown Level					160		°C
Thermal Shutdown Hysteresis					30		°C
DIGITAL INPUT ($\overline{SHDN}$ GAIN)							
Input Voltage High	V_{INH}			1.4			V
Input Voltage Low	V_{INL}					0.4	V
Input Leakage Current		T_A = +25°C				±1	µA

Note 2: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.

Note 3: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 4Ω, L = 33µH. For R_L = 8Ω, L = 68µH.

Note 4: Amplifier inputs AC-coupled to ground.

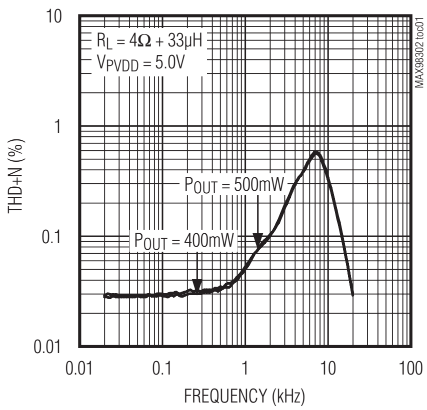
Note 5: Mode transitions controlled by $\overline{SHDN}$.

Stereo 2.4W Class D Amplifier

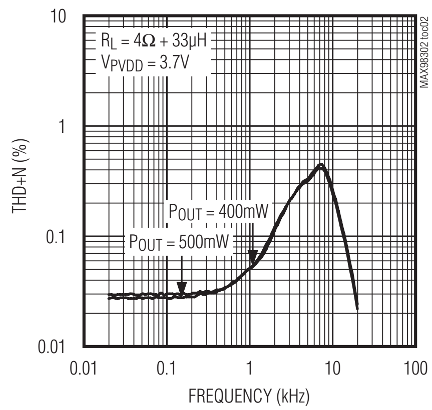
Typical Operating Characteristics

($V_{PVDD} = V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, unless otherwise specified, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)

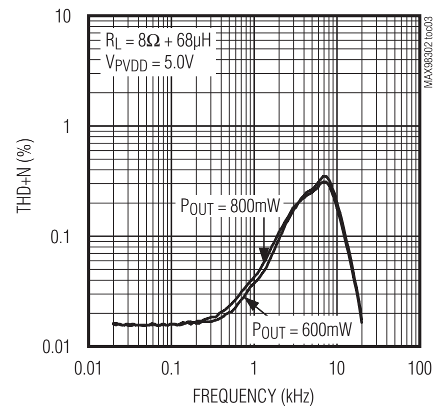
THD+N vs. FREQUENCY



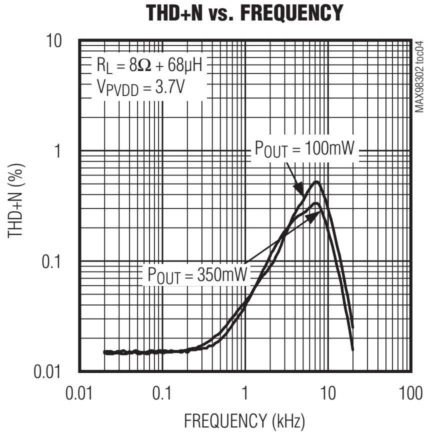
THD+N vs. FREQUENCY



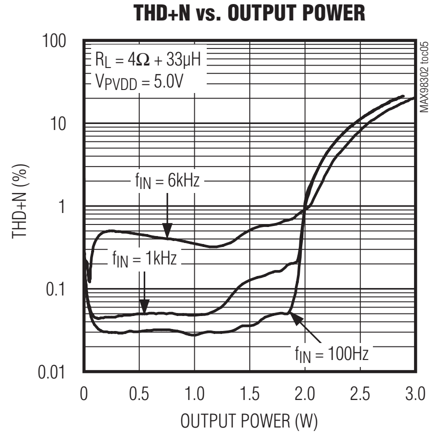
THD+N vs. FREQUENCY



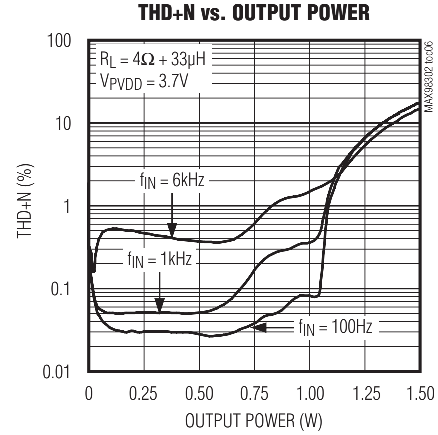
THD+N vs. FREQUENCY



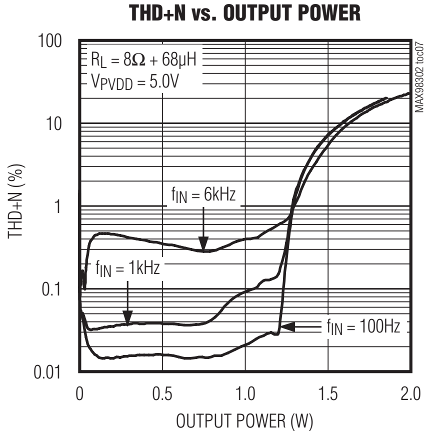
THD+N vs. OUTPUT POWER



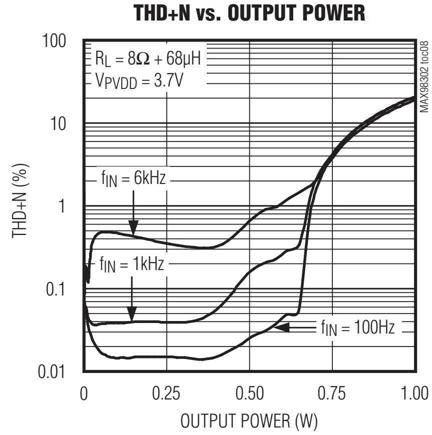
THD+N vs. OUTPUT POWER



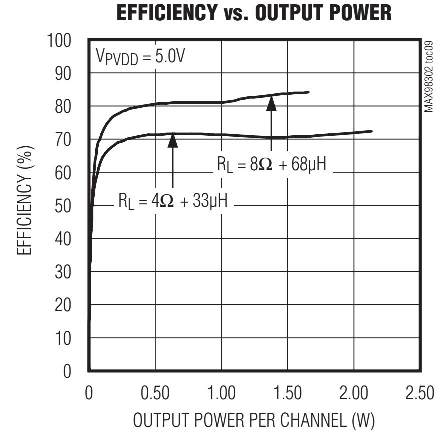
THD+N vs. OUTPUT POWER



THD+N vs. OUTPUT POWER



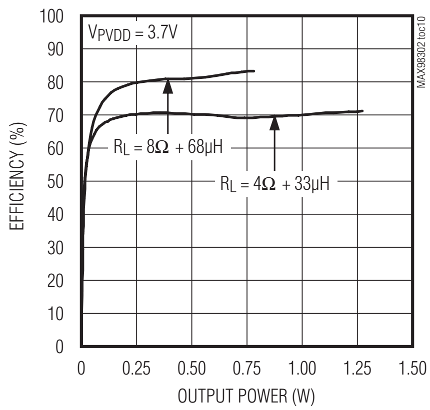
EFFICIENCY vs. OUTPUT POWER



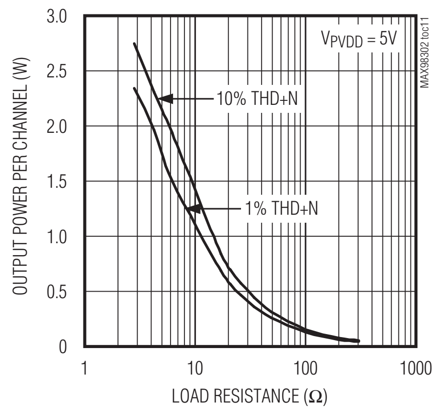
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{\overline{SHDN}} = 5.0V$, $V_{PGND} = 0V$, $A_V = 12dB$, $R_L = \infty$, unless otherwise specified, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, $T_A = +25°C$, unless otherwise noted.)

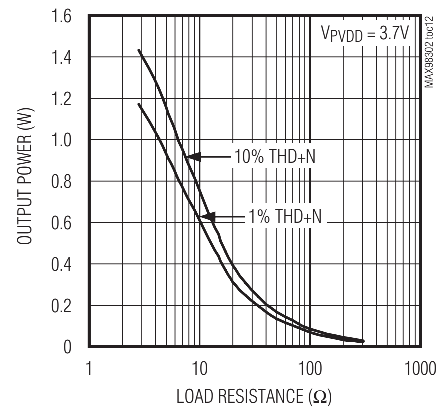
EFFICIENCY vs. OUTPUT POWER



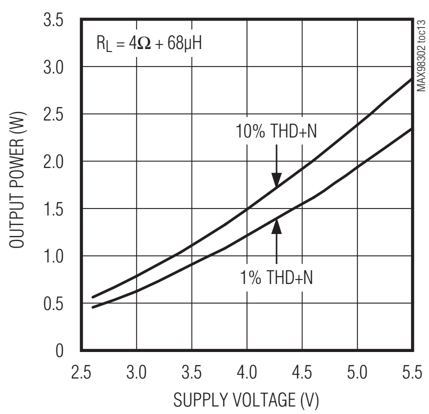
OUTPUT POWER vs. LOAD RESISTANCE



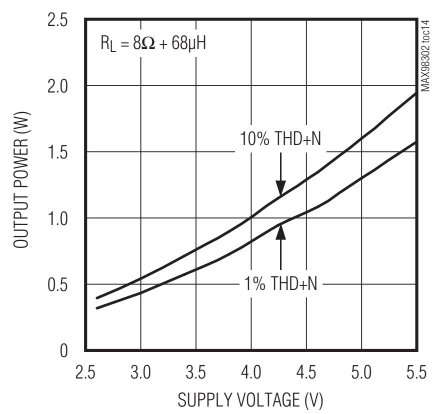
OUTPUT POWER vs. LOAD RESISTANCE



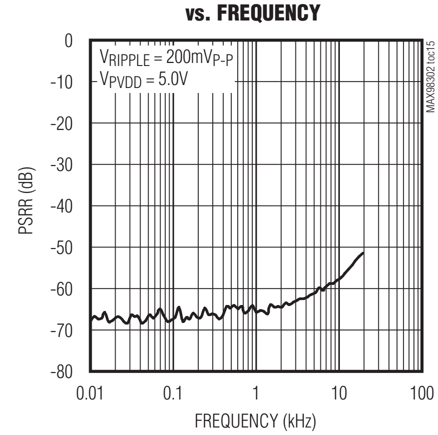
OUTPUT POWER vs. SUPPLY VOLTAGE



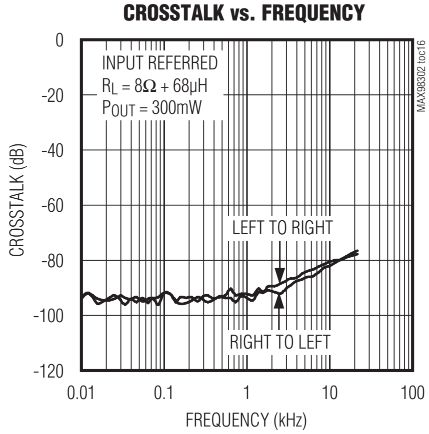
OUTPUT POWER vs. SUPPLY VOLTAGE



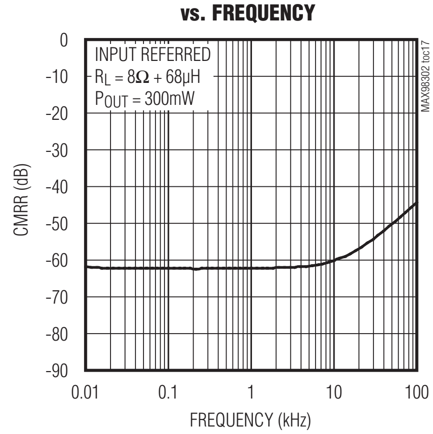
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



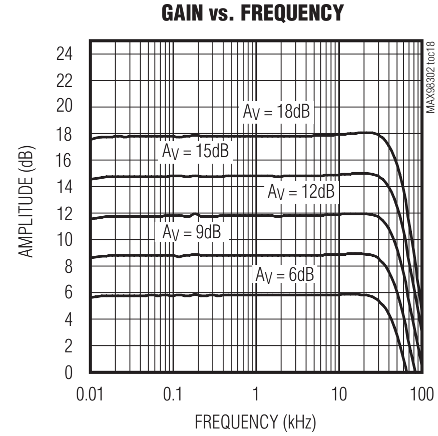
CROSSTALK vs. FREQUENCY



COMMON-MODE REJECTION RATIO vs. FREQUENCY



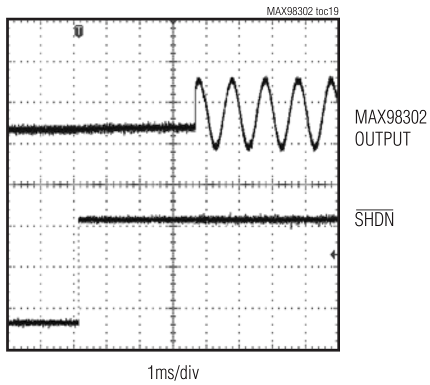
GAIN vs. FREQUENCY



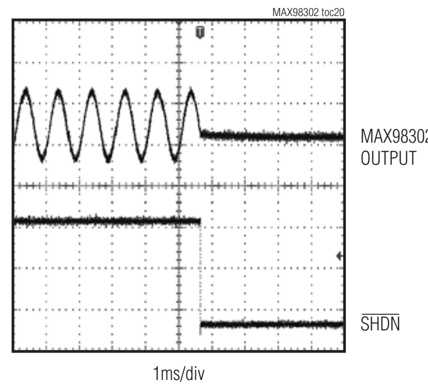
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, $R_L = \infty$, unless otherwise specified, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)

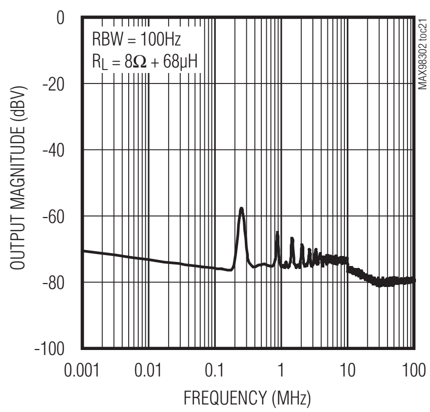
EXITING SHUTDOWN



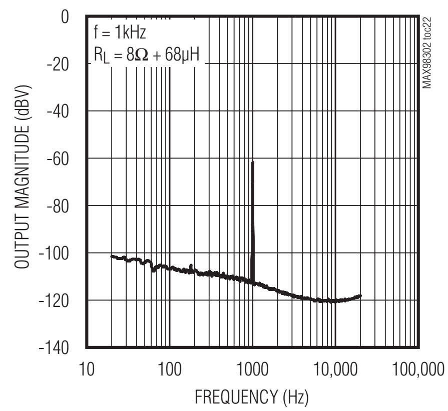
ENTERING SHUTDOWN



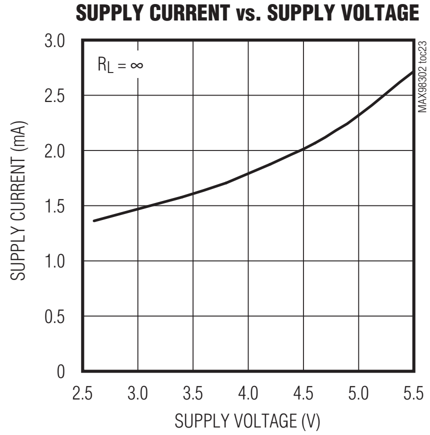
WIDEBAND OUTPUT SPECTRUM



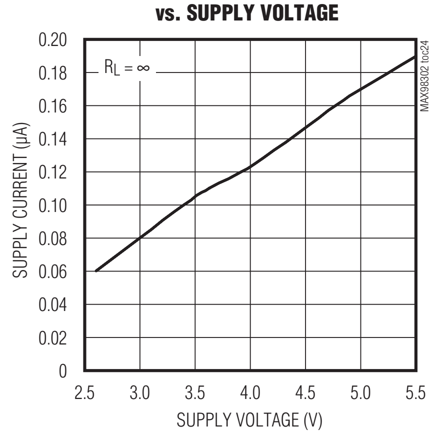
INBAND OUTPUT SPECTRUM



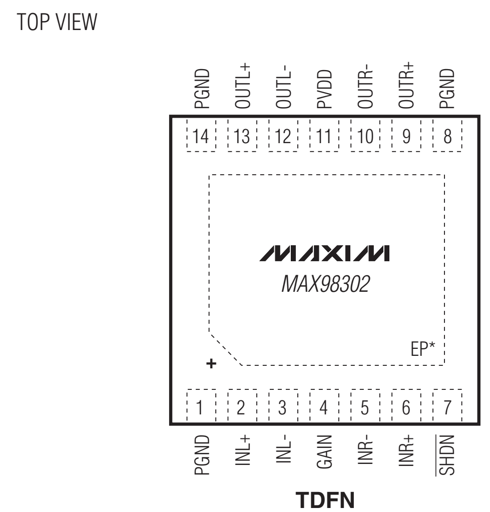
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



Pin Configuration



*CONNECT THE EP TO PGND TO ENHANCE THERMAL DISSIPATION.

Pin Description

PIN	NAME	FUNCTION
1, 8, 14	PGND	Ground
2	INL+	Noninverting Audio Left Input
3	INL-	Inverting Audio Left Input
4	GAIN	Gain Selection. See Table 1 for GAIN settings.
5	INR-	Inverting Audio Right Input
6	INR+	Noninverting Audio Right Input
7	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Drive $\overline{\text{SHDN}}$ low to place the device in shutdown.
9	OUTR+	Positive Right Speaker Output
10	OUTR-	Negative Right Speaker Output
11	PVDD	Power Supply. Bypass PVDD to PGND with a 0.1µF capacitor.
12	OUTL-	Negative Left Speaker Output
13	OUTL+	Positive Left Speaker Outpout
—	EP	Exposed Pad. Connect EP to a solid ground plane.

Detailed Description

The MAX98302 features industry-leading quiescent current, low-power shutdown mode, comprehensive click-and-pop suppression, and excellent RF immunity.

The MAX98302 offers Class AB audio performance with Class D efficiency in a minimal board-space solution.

The Class D amplifier features spread-spectrum modulation, edge-rate, and overshoot control circuitry that offers significant improvements to switch-mode amplifier radiated emissions.

The MAX98302 amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal-overload and short-circuit protection.

Class D Speaker Amplifier

The MAX98302 filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Ultra-Low-EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active emissions limiting edge-rate control circuitry and spread-spectrum modulation reduce EMI emissions, while maintaining up to 83% efficiency.

Maxim's spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The MAX98302's spread-spectrum modulator randomly varies the switching frequency by ±7kHz around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (2A typ), the MAX98302 disables the outputs for approximately 100μs. At the end of 100μs, the outputs are re-enabled. If the fault condition still exists, the MAX98302 continues to disable and re-enable the outputs until the fault condition is removed.

Selectable Gain

The MAX98302 offers five programmable gains selected using the GAIN input.

Table 1. Gain Control Configuration

GAIN PIN	MAXIMUM GAIN (dB)
Connect to PGND	18
Connect to PGND through 100kΩ ±5% resistor	15
Connect to PVDD	12
Connect to PVDD through 100kΩ ±5% resistor	9
Unconnected	6

Shutdown

The MAX98302 features a low-power shutdown mode, drawing 0.17μA of supply current. Drive $\overline{\text{SHDN}}$ low to put the MAX98302 into shutdown.

Click-and-Pop Suppression

The MAX98302 speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device. When entering shutdown, the differential speaker outputs ramp down to PGND quickly and simultaneously.

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter. The filter adds cost and size and decreases THD+N performance. The MAX98302's filterless modulation scheme does not require an output filter.

Because the switching frequency of the MAX98302 is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10μH. Typical 8Ω speakers exhibit series inductances in the 20μH to 100μH range.

Component Selection

Speaker Amplifier Power-Supply Input (PVDD)

PVDD powers the speaker amplifier. PVDD ranges from 2.6V to 5.5V. Bypass PVDD with 0.1μF and 10μF capacitors to PGND. Also, connect at least 10μF of system bulk capacitance to PVDD. Apply additional bulk capacitance at the device if long input traces between PVDD and the power source are used.

Input Filtering

The input-coupling capacitor (C_{IN}), in conjunction with the amplifier's internal input resistance (R_{IN}), forms a highpass filter that removes the DC bias from the incoming signal. These capacitors allow the amplifier to bias the signal to an optimum DC level.

Assuming zero-source impedance with a gain setting of A_V = 12dB, 15dB, or 18dB, C_{IN} is:

$$C_{IN} = \frac{8}{f_{-3dB}}[\mu F]$$

with a gain setting of A_V = 9dB, C_{IN} is:

$$C_{IN} = \frac{5.7}{f_{-3dB}}[\mu F]$$

with a gain setting of A_V = 6dB, C_{IN} is:

$$C_{IN} = \frac{4}{f_{-3dB}}[\mu F]$$

where f_{-3dB} is the -3dB corner frequency. Use capacitors with adequately low-voltage coefficients for best low-frequency THD performance.

Layout and Grounding

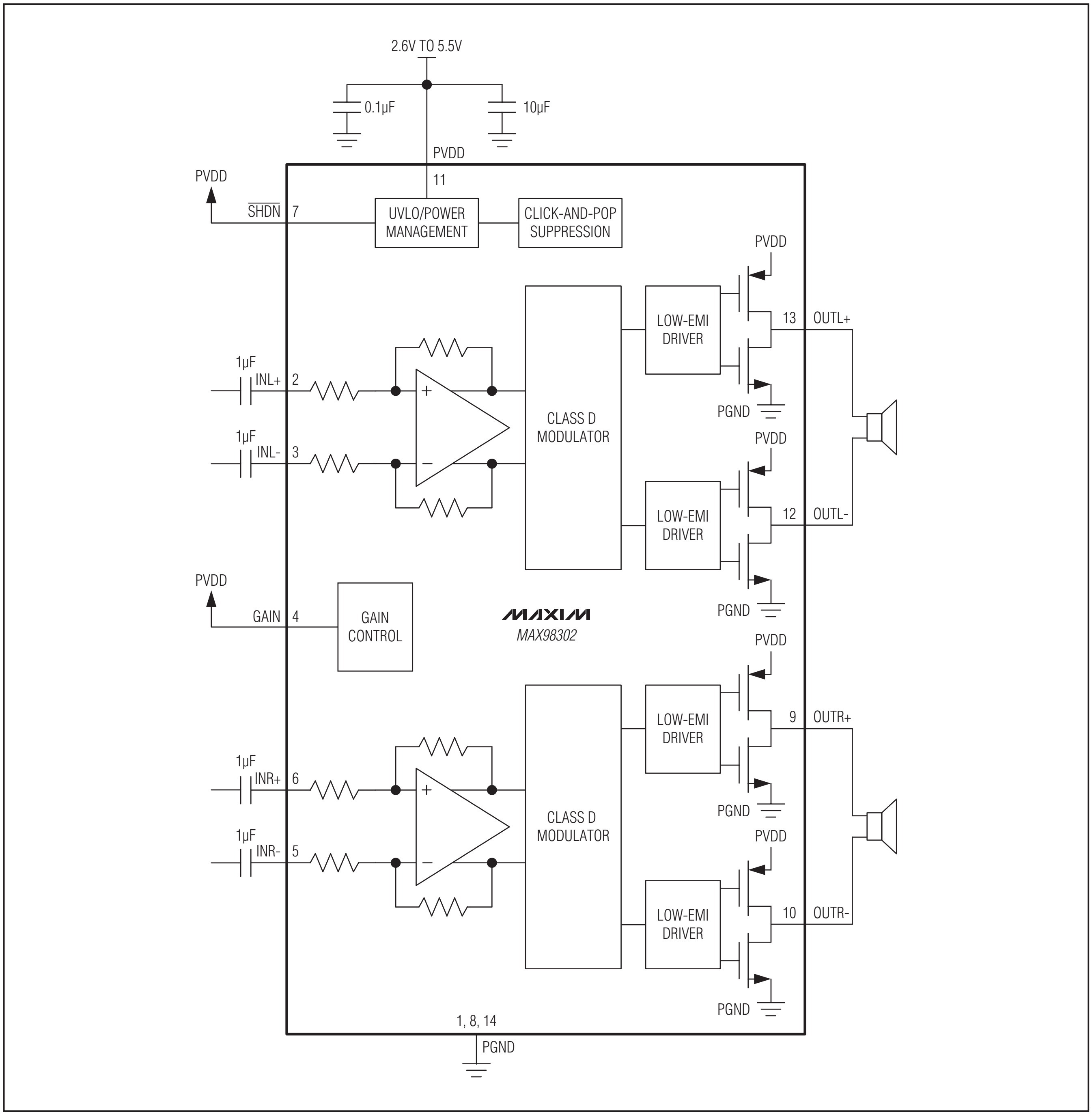
Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As load impedance decreases, the current drawn from the device outputs increase. At higher current, the resistance of the output traces decrease the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through a 100mΩ trace, 49mW is consumed in the trace. If power is delivered through a 10mΩ trace, only 5mW is consumed in the trace. Wide output, supply, and ground traces also improve the power dissipation of the device.

The MAX98302 is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

The MAX98302 TDFN-EP package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a heat conduction path from the die to the PCB. Connect the exposed thermal pad to the ground plane by using a large pad and multiple vias.

Block Diagram



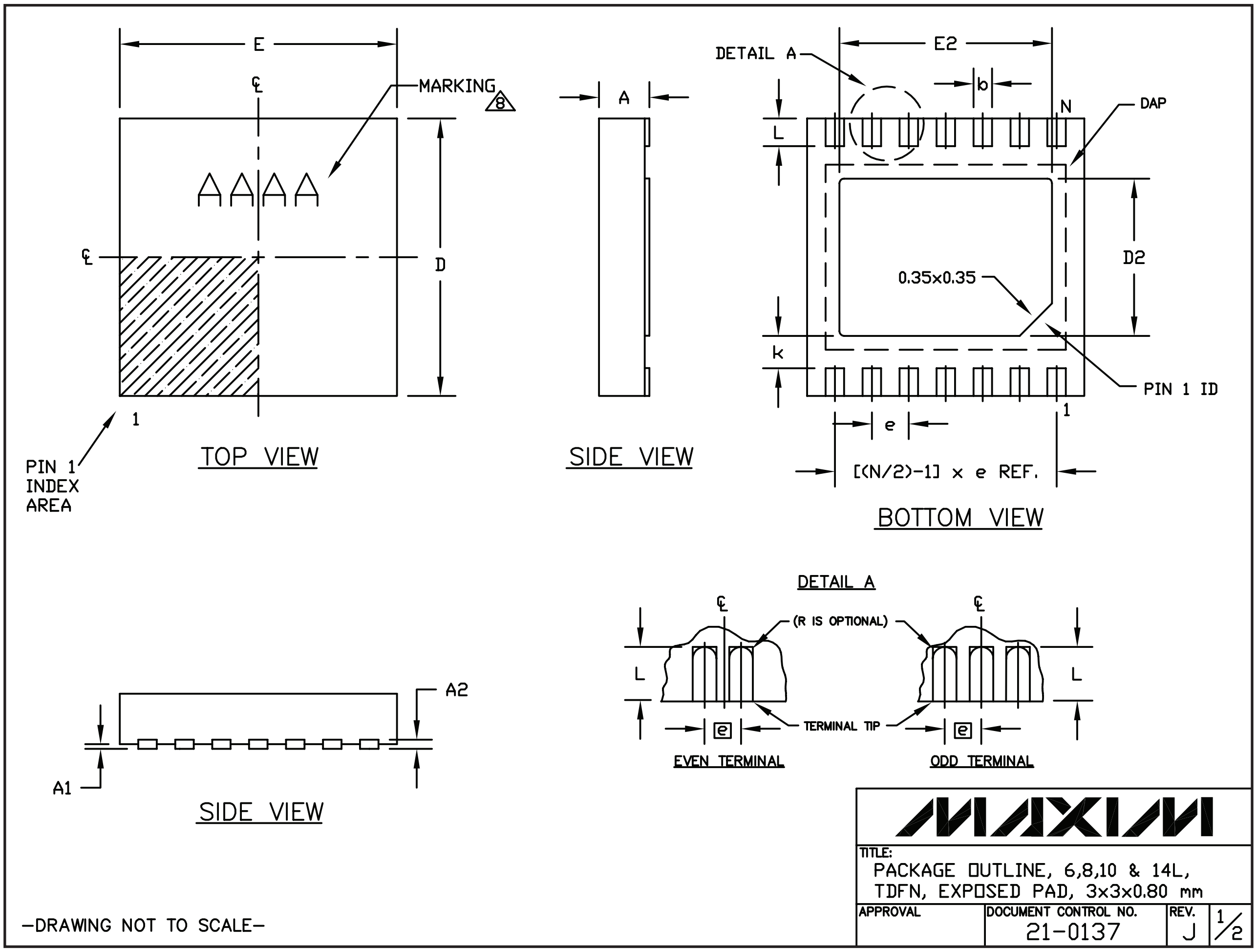
Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
14 TDFN-EP	T1433-2	21-0137



Package Information (continued)

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COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	J	2/2

-DRAWING NOT TO SCALE-

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release	—

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600