100BASE-TX/T4 MULTIPORT REPEATER CONTROLLER

GENERAL DESCRIPTION

The W89C880F, a 100Base-T4/TX Fast Ethernet MultiPort Repeater Controller (FastMPR), is designed for large Fast Ethernet networks. The W89C880F FastMPR complies fully with the IEEE802.3u clause 27 repeater standard. The FastMPR offers a low-cost, high-performance solution to alleviate the hub-to-network traffic distance limitation that Fast Ethernet faces. Two independent MII ports are provided: a normal MII port that can support up to 11 PHY with the MII interface and an extension port that can easily extend the distance between the hubs to as far as 100 meters. The FastMPR implements a simple and limited bridge functions, such as address learning/filtering, runt packet filtering, and two types of packet forwarding functions: fragment free and store-and-forward. The extension port can be disabled by a hardware setting allowing it to act as a normal MII interface port. The W89C880F offers a maximum of 12 ports. The device also supports one inter-FastMPR interface to construct a large hub with up to 6 FastMPRs. The W89C880F implements enhanced network status report functions, such as network utilization report, individual port partition status report, individual port jabber status report, and collision report. The FastMPR also supports T4/TX and translation mode, simultaneously connecting to a T4 or TX physical layer controller with the MII interface.

FEATURES

- Functions conform to IEEE802.3u clause 27 specifications
- Supports up to 12 MII repeater ports
- T4/TX translation function
- Asynchronous inter-FastMPR interface for up to 6 FastMPR hub applications
- A MII extension port with 100 meters hub-hub distance cascade capability
- Limited bridge function: address learning/filtering, packet store/forwarding, fragment-free
- 32 KB $\times$ 8, 64 KB $\times$ 8, 128 KB $\times$ 8 SRAM interface provided
- MII management function supported
- On-chip FIFO elasticity for physical signal retiming
- Port status direct report function
- On-chip network utilization report
- Individual port, jabber/partition/reconnection state machine
- Advanced CMOS process for lower power dissipation
- Single 5V power supply
- Packaged in 160-pin PQFP

PIN CONFIGURATION

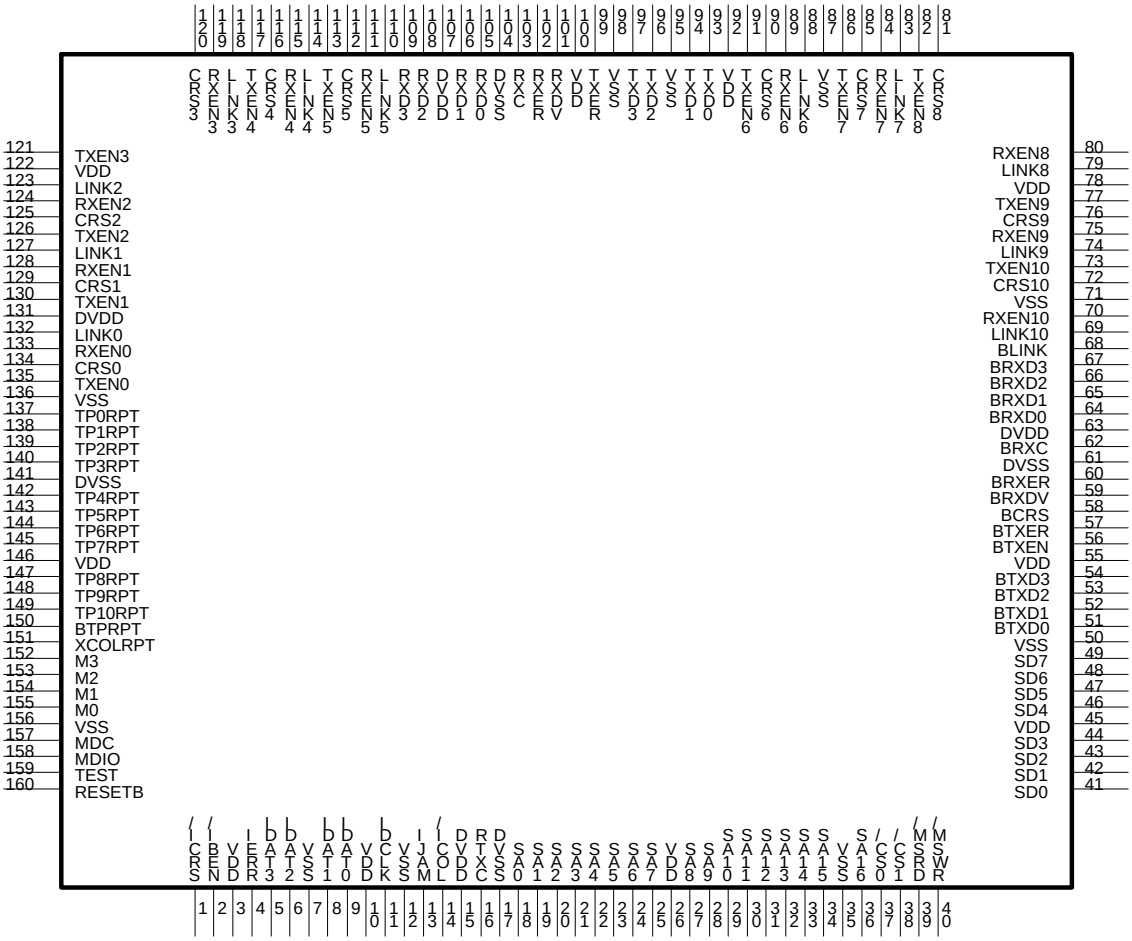


Figure 1

PIN DESCRIPTION

TRANSCEIVER INTERFACE PINS			
NAME	**NO.**	**I/O**	**DESCRIPTION**
CRS<10:0>	72, 76, 81, 85, 90, 112, 116, 120, 125, 129, 134	I	Carrier Sense Input from PHY. When the FastMPR receives a carrier sense signal from a specific port, it will echo RXEN to that specific port. CRS <10:0> refers to the carrier sense signal input of each port (TP10–0). "1" means the carrier is present.
RXEN<10:0>	70, 75, 80, 84, 89, 111, 115, 119, 124, 128, 133	O/L	Receive Enable Output. RXEN<10:0> refers to the Receive Enable output of ports TP10–0; 1 means receive is enabled. When CRSn = 1 and the CRS of other ports is deactivated, RXENn will be active and the FastMPR is ready to receive data. Only one of RXEN<10:0> can be active at any one time.
TXEN<10:0>	73, 77, 82, 86, 91, 113, 117, 121, 126, 130, 135	O/L	Transmit Enable Output. TXEN<10:0> refers to the transmit enable output of ports TP10–0; "1" means transmit is enabled. When one of CRS <10:0> = 1, TXEN will be active and the FastMPR is ready to transmit data to all other ports except the input port.
LINK<10:0>	69, 74, 79, 83, 88, 110, 114, 118, 123, 127, 132	I	PHY Link Status Input from PHY. The FastMPR will propagate the input link status of PHY, output the link status, and mix it with the received status information of each port in train to TP0–10RPT pins.
RXD<3:0>	109, 108, 106, 105	I	PHY Receive Data. The FastMPR receives data from PHY through these pins. Data are synchronized with the rising edge of RXC.
TXD<3:0>	97, 96, 94, 93	O/H	PHY Transmit Data. FastMPR transmits data to PHY through these pins. Data are synchronized with the rising edge of RTXC.
RXER	102	O	PHY Receive Error. "1" means an error has occurred in the data received from PHY.
TXER	99	O/H	FastMPR Transmit Error. "1" means that an RXER or FIFO error has occurred.
RXC	103	I	Receive Clock. Input from PHY. This pin is used to synchronize the data received from PHY. The FastMPR utilizes one of the RXEN<10:0> signals to decide which RXC input from the receive enable port of PHY should be chosen.
RTXC	16	I	Transmit Clock. An Input clock. This pin is used to synchronize FastMPR transmit data.
RXDV	101	I	Receive Data Valid. Input from PHY. When high, PHY has valid data present in RXD<3:0>.

Pin Description, continued

MANAGEMENT INTERFACE PINS			
NAME	**NO.**	**I/O**	**DESCRIPTION**
MDC	157	I	Management Clock. Input for FastMPR register read/write configuration. Maximum clock rate is 2.5 MHz. This pin is used to synchronize with MDIO.
MDIO	158	I/O/L	Management Data. When the address of the MDIO device matches the reset jumper setting of TP0–4RPT/AD<0:4> on the FastMPR, the FastMPR will respond to the MDIO read/write command.
PORT STATUS REPORT/JUMPER SETTING PINS			
TP0–4RPT/ AD<0:4>	137–140, 142	I/O/L	TP0-4 Port Status Output/FastMPR Device Address. After power-on reset, each of these pins can output the status train of one port, which sequentially reports four aspects of the FastMPR port status. The status train of each TPnRPT contains link/activity, partition, utilization, and jabber in sequence. The status train is latched by the signals M0–3. M0 is used to latch the link/activity status of all ports. M1 is used to latch the partition status of all ports. M2 is used to latch the network utilization at some instant in time. M3 is used to latch the jabber status. When these pins output the port status, they are active low. During power-on reset, these pins are used as the device address input pins of the FastMPR. If these pins are each connected with a pull-up resistor to the power supply, the input value of each pin is "1". If no pull-up resistor is connected to the pin, the input value is "0". When the MDIO command address matches the device address, the FastMPR will respond to MDIO read/write commands.
TP5RPT/ DISBG	143	I/O/L	TP5 Port Status Output /Extension port Enable. After power-on reset, this pin can sequentially output four aspects of TP5 port status: link/activity, partition, network utilization, and jabber. This pin outputs the port status, it is active low. During power-on reset, if no pull-up resistor is connected to this pin, the extension port is enabled. If a pull-up resistor is connected to this pin, the extension port is disabled. In this situation, the extension port acts as a normal MII interface and the FastMPR can support up to twelve ports.
TP6RPT/ SRAMSEL0	144	I/O/L	TP6 Port Status Output/SRAM size select. After power-on reset, this pin can sequentially output four aspects of TP6 port status: link/activity, partition, network utilization, and jabber. When the pin outputs the port status, it is active low. During power-on reset, if no pull-up resistor is connected to this pin, 64 KB data buffer is selected. If a pull-up resistor is connected to this pin, the buffer size is 128 KB.

Pin Description, continued

PORT STATUS REPORT/JUMPER SETTING PINS			
NAME	**NO.**	**I/O**	**DESCRIPTION**
TP7RPT/ SRAMSEL1	145	I/O/L	TP7 Port Status Output/SRAM interface select. After power-on reset, this pin can sequentially output four aspects of TP7 port status: link/activity, partition, network utilization, and jabber. When this pin outputs the port status, it is active low. During power-on reset, if no pull-up resistor is connected to this pin, a 32 KB × 8 × 2 or 64 KB × 8 × 2 SRAM interface is selected. If a pull-up resistor is connected to this pin, then 64 KB × 8 × 1 or 128 KB × 8 × 1 buffer SRAM size is selected.
TP8RPT/ FRAGSEL0	147	I/O/L	TP8 Port Status Output/Extension port fragment free window select 0. After power-on reset, this pin can sequentially output four aspects of TP8 port status: link/activity, partition, network utilization, and jabber. When this pin outputs the port status, it is active low. During power-on reset, regardless of whether a pull-up resistor is connected to this pin or not, the FastMPR can select a fragment-free window. The size of the fragment-free window is chosen by a combination of FRAGSEL0 and FRAGSEL1.
TP9RPT/ FRAGSEL1	148	I/O/L	TP9 Port Status Output/Extension port fragment-free window select 1. After power-on reset, this pin can sequentially output four aspects of TP9 port status: link/activity, partition, network utilization, and jabber. When this pin outputs the port status, it is active low. During power-on reset, whether a pull-up resistor is connected to this pin or not, the FastMPR can select the fragment-free window. The size of the fragment-free window is chosen by FRAGSEL0 and FRAGSEL1as shown below ("0" means no pull-up resistor is connected, "1" means pull-up resistors are connected). Window value (bytes) disable 16 64 96 FRAGSEL 0 1 0 1 0 FRAGSEL 1 1 1 0 0 This is a limited tunable latency function for cut-through operation in filtering runt packets.
TP10RPT	149	I/O/L	TP10 Port Status Output. After power-on reset, this pin can sequentially output four aspects of TP10 port status: link/activity, partition, network utilization, and jabber.
BTPRPT	150	I/O/L	Extension port Status Output. After power-on reset, when the extension port is enabled, BTPRPT outputs the link/activity status. If the extension port is disabled, BTPRPT sequentially outputs the status train of link/activity, partition, netwok utilization, and jabber status. During the network utilization report period, this pin has no function. When this pin outputs the port status, it is active low.

Pin Description, continued

PORT STATUS REPORT/JUMPER SETTING PINS			
NAME	**NO.**	**I/O**	**DESCRIPTION**
XCOLRPT	151	I/O/L	Any Collision status Output/Carrier Integrity Monitor Select. This is an active high pin. After power-on reset, this pin outputs the FastMPR port collision status (with the exception of the extension port).
M0	155	O/L	Port Status Output select 0. After power-on reset, this output pin latches the link/activity status report from the TP0–10RPT and BTPRPT pins.
M1	154	O/L	Port Status Output select 1. This output pin latches the partition status report from the TP0–10RPT and BTPRPT pins.
M2	153	O/L	Port Status Output select 2. This output pin latches the network utilization report from the TP0–9RPT pins.
M3	152	O/L	Port Status Output select 3. This output pin latches the jabber status report from the TP0–10RPT, BTPRPT pins.
EXTENSION PORT INTERFACE PINS			
BCRS	58	I	Extension port Carrier Input. This is the carrier sense signal coming from the FastMPR extension port. "1" means the extension port has carrier present.
BTXEN	56	O/L	Extension port Transmit Enable Output. "1" means the extension port is transmit enabled.
BRXD<3:0>	67–64	I	Extension port Receive Data. Input data from PHY connected to bridge port. Data are synchronous with the rising edge of BRXC.
BTXD<3:0>	54–51	O/L	Extension port Transmit Data. Output data from FastMPR. Data are synchronous with the rising edge of RTXC.
BRXER	60	I	Extension port Receive Error. "1" means that an error has occurred in the data received by PHY.
BTXER	57	O/L	Extension port Transmit Error. "1" means that an RXER or FIFO error event has occurred.
BRXC	62	I	Extension port Receive Clock. Input from PHY. This pin is used to synchronize the received data of PHY connected to the extension port.
BRXDV	59	I	Extension port Receive Data Valid. Input from PHY. "1" means PHY has valid data present on BRXD<3:0>.
BLINK	68	I	Extension port Link Status Input. Input from PHY. "1" means PHY link is good.
INTER-FastMPR INTERFACE PINS			
IDAT<3:0>	5, 6, 8, 9	I/O/Z	Inter-FastMPR interface Data. These pins are used to cascade several FastMPR chips into one larger unit. The FastMPRs use the inter-FastMPR interface to send/receive data to/from other FastMPRs. The data are transmitted in NRZ format. During idle state, IDAT<3:0> are in high-impedance state.

Pin Description, continued

INTER-FastMPR INTERFACE PINS			
NAME	**NO.**	**I/O**	**DESCRIPTION**
IDCLK	11	I/O/Z	Inter-FastMPR interface Data Clock. This is a bidirectional pin. If the FastMPR issues a carrier output to the integrator through its $\overline{\text{ICRS}}$ pin, the integrator sends an acknowledge reply later through the $\overline{\text{IBEN}}$ pin to the FastMPRs. Once an $\overline{\text{ICRS}}$ has been issued and a valid $\overline{\text{IBEN}}$ has been received, the FastMPR sends IDCLK, IJAM, and IDAT<3:0> to the inter-FastMPR interface integrator. The other FastMPRs do not issue carrier outputs to the integrator, but instead receive IDCLK, IJAM, and IDAT<3:0> from the integrator after receiving valid $\overline{\text{IBEN}}$. If $\overline{\text{IBEN}}$ is not asserted, IDCLK is in high-impedance state.
IERR	4	I/O/Z	Inter-FastMPR interface Data Error. This pin indicates whether an error occurred during a InterFastMPR interface transaction. When the FastMPR transmits data to the inter-FastMPR interface integrator, the assertion of IERR means a transmit error on the interface occurred. When the FastMPR receives data from the inter-FastMPR interface integrator, the assertion of IERR means a receive error occurred on the interface.
$\overline{\text{ICRS}}$	1	O/L	Inter-FastMPR interface Carrier Sense output. If asserted, the FastMPR will output a packet to the inter-FastMPR interface integrator. After the FastMPR that asserted $\overline{\text{ICRS}}$ receives a valid $\overline{\text{IBEN}}$ from the integrator, the FastMPR will send data to IDAT<3:0>.
$\overline{\text{IBEN}}$	2	I	Inter-FastMPR interface Enable. If asserted, the FastMPR that issued $\overline{\text{ICRS}}$ earlier will output IDAT<3:0>, IDCLK, IJAM, and IERR to the inter-FastMPR interface integrator.
$\overline{\text{ICOL}}$	14	I	Inter-FastMPR interface Collision. "0" means a collision event has occurred. $\overline{\text{ICOL}}$ is asserted only when more than one FastMPR outputs a carrier to the inter-FastMPR interface integrator at the same time.
IJAM	13	I/O/Z	Inter-FastMPR interface Jamming. When the FastMPR enters the collision state, it asserts IJAM and propagates IJAM to the inter-FastMPR interface integrator. When another FastMPR receives IJAM from an integrator, it means that a collision has occurred on the other FastMPR. When IJAM is asserted, the assertion of IERR means the FastMPR is in the one_port_left state, and the deassertion of IERR means the FastMPR is in the multi_FastMPR collision state.

Pin Description, continued

SRAM INTERFACE PINS			
NAME	**NO.**	**I/O**	**DESCRIPTION**
SA<16:0>	36, 34–27, 25–18	O/L	SRAM Address Bus. The FastMPR supports different SRAM sizes for buffer use, including 32 KB × 8, 64 KB × 8, and 128 KB × 8. SA15, SA16 must be kept low when these two address pins are not used.
SD<7:0>	49–46, 44–41	I/O/L	SRAM Data Bus.
$\overline{CS0}$	37	O/L	SRAM Chip Select 0. This pin is used to enable the Bank 0 SRAM.
$\overline{CS1}$	38	O/L	SRAM Chip Select 1. This pin is used to enable the Bank 1 SRAM.
$\overline{MSRD}$	39	O/L	SRAM Read command.
$\overline{MSWR}$	40	O/L	SRAM Write command.
MISCELLANEOUS			
$\overline{RESET}$	160	I	FastMPR RESET. This pin is active low. It needs a minimum 50 µS reset pulse width, when V_{DD} is valid and stable.
TEST	159	I	Test Pin. Set this pin to enter test mode.
POWER/GROUND PINS			
DV_{DD}	15, 63, 107, 131		Digital Power Supply.
DV_{SS}	17, 61, 104, 141		Digital Ground.
V_{DD}	92, 100		MII Bus Power Supply.
V_{SS}	95, 98		MII Bus Ground.
V_{DD}	78, 122		MII Port Interface Power Supply.
V_{SS}	87, 136		MII Port Interface Ground.
V_{DD}	146		LED Interface Power Supply.
V_{SS}	156		LED Interface Ground.
V_{DD}	3, 10		Inter-FastMPR interface Power Supply.
V_{SS}	7, 12		Inter-FastMPR interface Ground.
V_{DD}	55		Extension port Power Supply.
V_{SS}	71		Extension port Ground.
V_{DD}	26, 45		SRAM Interface Power Supply.
V_{SS}	35, 50		SRAM Interface Ground.

Note:

"I" means input, "O" means output, "H" means 24 mA high drive/sink cell, "L" means 4 mA low drive/sink cell, and "Z" means high-impedance.

SYSTEM DIAGRAM

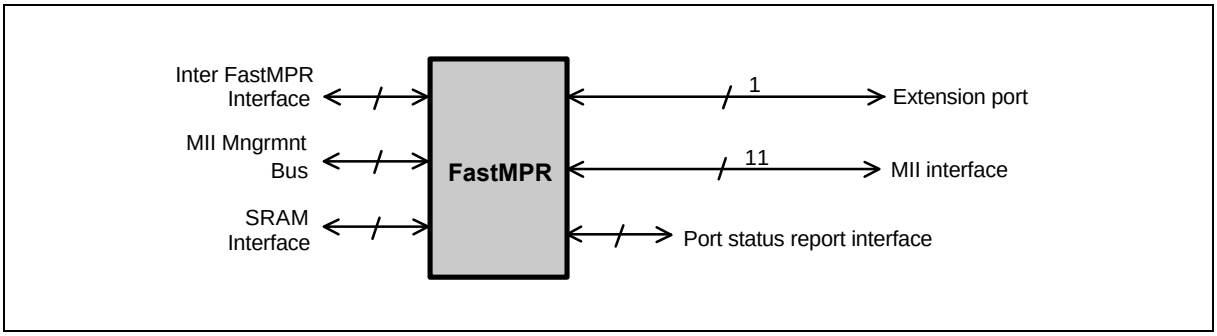


Figure 2

BLOCK DIAGRAM

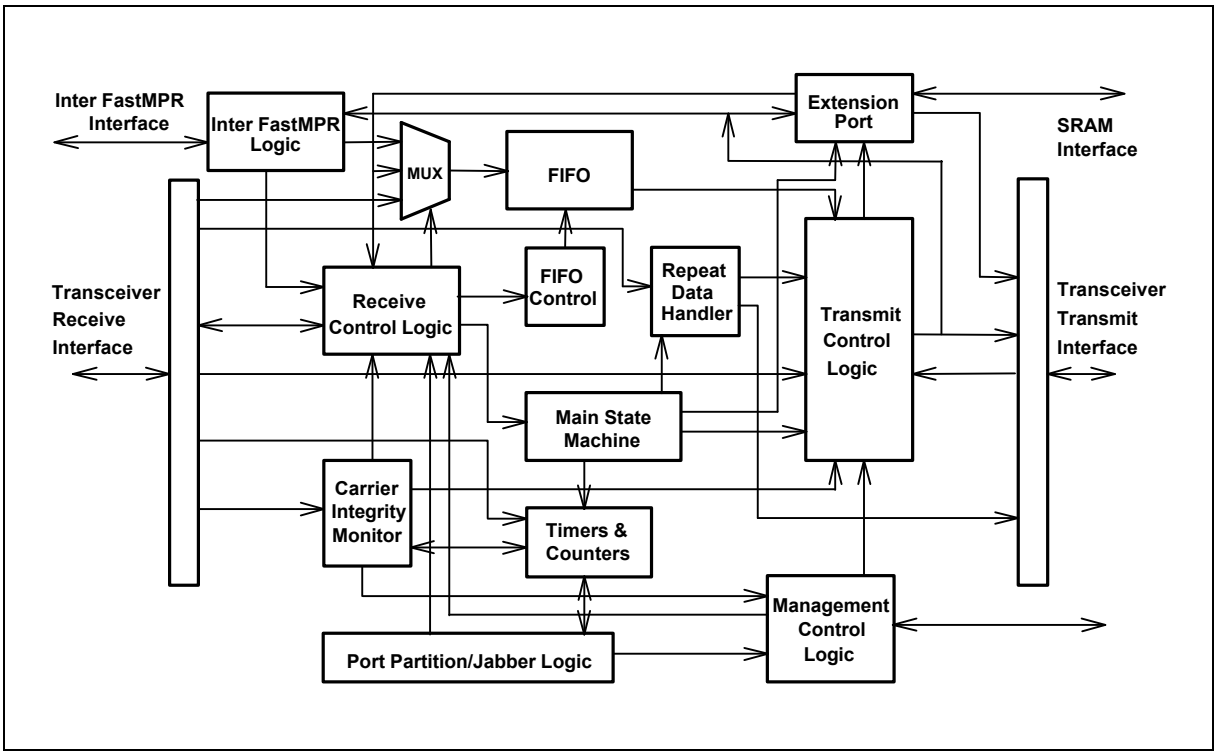


Figure 3

FUNCTIONAL DESCRIPTION

Basic MII Port Functions

The Media Independent Interface (MII) is an interface bus composed of 18 signal pins that is defined by the IEEE802.3u specification. The MII offers a path for transferring data, status signals, and control signals between MAC and PHY. Its functions are summarized below.

Data transfer: The MII bus utilizes TXD[0:3] and RXD[0:3] to transfer data. When an error occurs in PHY, it will assert the RXER pin on the hub and then the hub asserts TXER on every other port.

Media status: If PHY detects a collision or carrier, it will notify the FastMPR that a collision has occurred, that the link status is good, and so forth.

Management function: The FastMPR has four hardware-dependent registers, which are controlled by both the MII interface and pin settings. The details are described in the MII Management section.

This interface is used to provide media independence for various types of wiring, such as unshielded twisted pair, shielded twisted pair, fiber optic cable, and potentially other media. A media access device can be used with this interface to form a LAN adapter or a hub port with any of these media.

The FastMPR provides two MII interfaces. One interface is for general purpose use; it supports the MII management function and can drive up to 11 physical layers. The other interface provides Fast Ethernet network extension functions. The extension port implementation allows a 100 Mbps Fast Ethernet network to be easily segmented with a network distance limitation of 100 meters (similar to 10 Mbps Ethernet). A FastMPR application is shown in the following diagram.

General Application Architecture

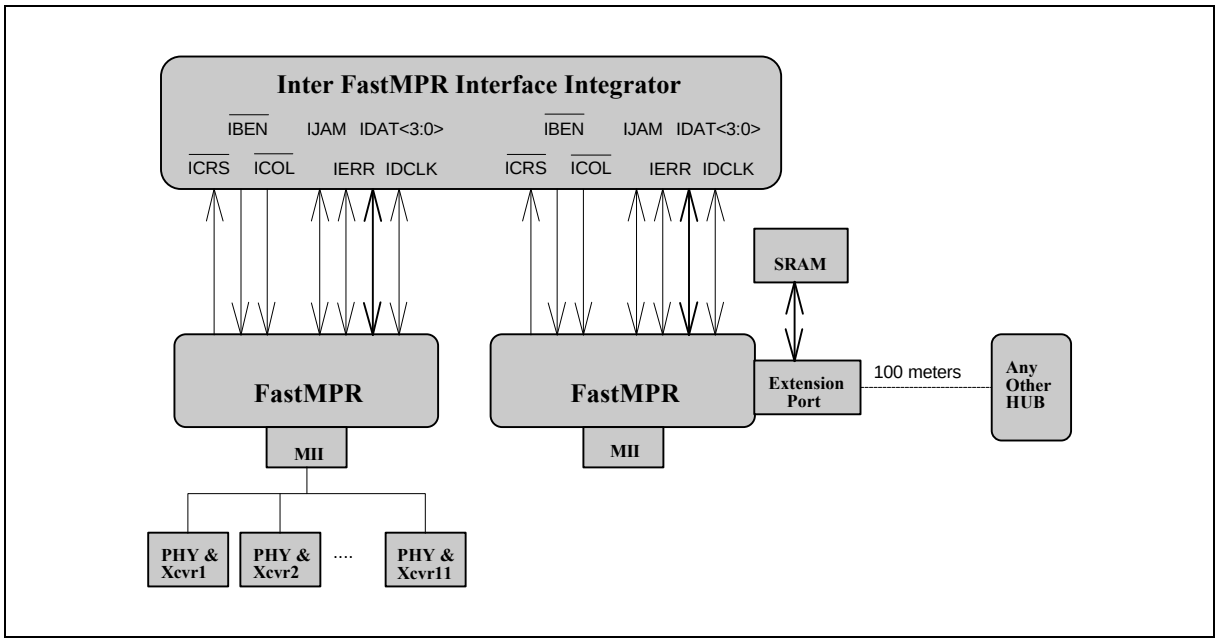


Figure 4

The following section gives a detailed description of each FastMPR function block:

MII Port Switch

The FastMPR connects to the physical layer controller (PHY) through the input pins RXDV, RXER, RXC, and RXD<3:0> and the output pins TXER and TXD<3:0>. The direction of the data or signal transfer is assigned by the FastMPR by asserting TXEN or RXEN. When it asserts TXEN, the FastMPR is ready to regenerate and transfer packets to the connected port. The PHY device will then fetch the packet and put it on the media through the PMD transceiver. When PHY sends out a CRS, the FastMPR asserts RXEN to this PHY, before repeating this packet to all other TP ports.

MII Data Error Handling

If a receive error occurs while the PHY controller is receiving data, the controller will issue a receive error signal RXER to the FastMPR. The FastMPR will then repeat the data stream to all other ports after a short delay. The FastMPR will also assert TXER at the location RXER to indicate that there is a receive error at this location.

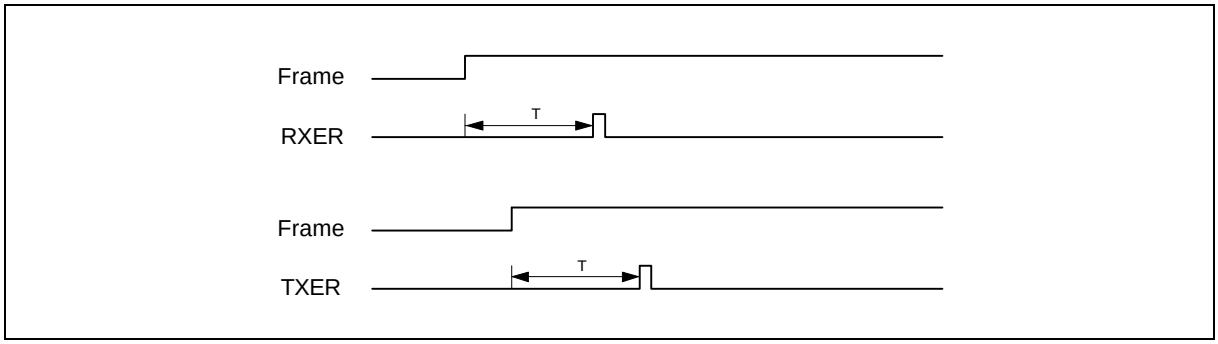


Figure 5

In the figure shown above, the upper timing diagram represents the receiving port, and the lower diagram is a repeated frame with some hub latency. These two timing diagrams are similar and keep the same T latency between the SFD (start of frame delimiter) and error signal (RXER, TXER).

MII Port Collision and Jam Generation

The FastMPR also monitors the input signals CRS0–10. If more than one carrier appears at the same time, the FastMPR will issue a jamming pattern to all its output ports, while reporting the collision status to the direct report pin XCOLRPT. After the collision has been detected, the FastMPR will immediately append the jamming pattern to all the connected ports until all network nodes stop transmitting data frames, only one node is active, or a power-on reset occurs. Figure 6 shows how the FastMPR enters and leaves the collision state.

Auto Partition/Reconnection

The FastMPR implements an auto partition/reconnection function to protect the network from failure caused by consecutive collisions from a specific port on the FastMPR. Each port on the FastMPR implements an independent auto partition/reconnection state function. The port will automatically partition itself when 64 or more consecutive collisions occur on the same port (the IEEE802.3 standard is greater than 60). A port will automatically recover to its active state after either successfully transmitting more than 512 bits of data continuously without collision on the same port (IEEE802.3 defines this figure to be between 450 and 560 bits) or after a power-on reset.

When a port is partitioned, the FastMPR does not allow any input messages to pass from the port, but can accept output messages from the hub internal to the partitioned port.

Collision and JAM Diagram

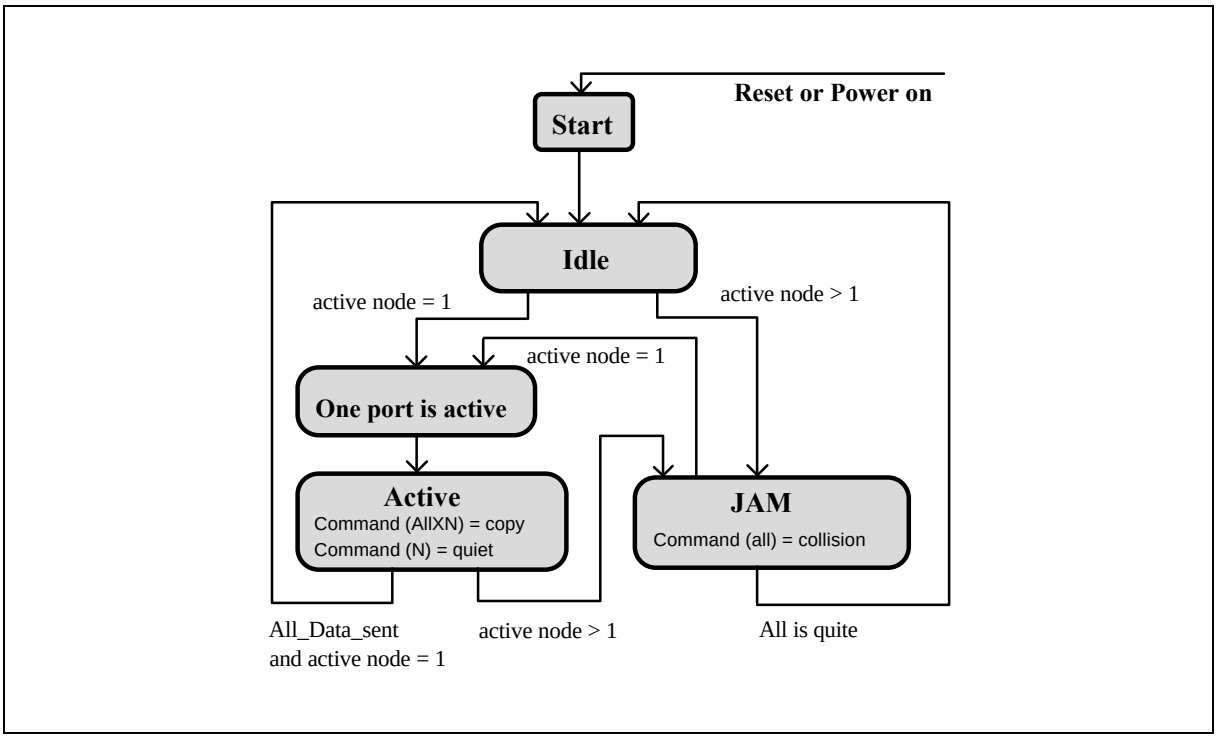


Figure 6

FastMPR Partition Diagram

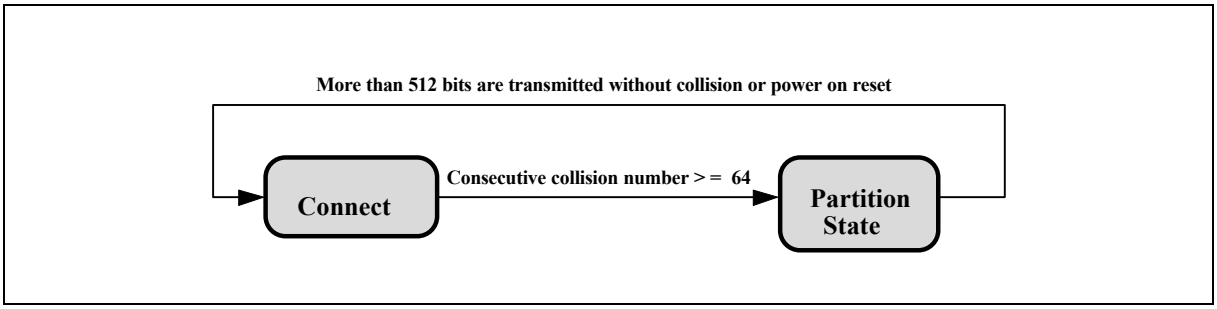


Figure 7

Jabber Protection

The jabber protection function prevents reception of illegally long packets, which would degrade network performance. When a FastMPR port receives a packet longer than 65536 bits, the jabber function cuts the data frame, and the receive/transmit path of the port is disabled. Then no data frame, regardless of whether it is from an input or output end, can pass through the port unless the carrier on the port is no longer detected or the FastMPR is reset (by being switched off and then on again). The jabber timer specification of Fast Ethernet is 40000–75000 bit times.

Carrier Integrity Monitor

The carrier integrity monitor function can be activated only in the 100BaseTX physical layer controller (PHY) and is neglected in T4 PHY. The FastMPR monitors this carrier activity and utilizes four types of timers to judge whether a carrier is distinguishable. The four timers are the false carrier timer (480 bits time), idle timer (33792 bits), Ipg timer (80 bits), and valid carrier timer (480 bits). The standard IEEE802.3u specifications for these items are the following:

False carrier timer: 450–500 bit-time

Idle timer: 33000 ±25% bit-time

Ipg timer: 64–86 bit-time

Valid carrier timer: 450–500 bit-time

The carrier integrity monitor state machine will force a port to enter the isolation state to prevent a malfunctioning port from disturbing the network segment. If the J and K patterns defined in 4B/5B coding table occur, so that the carrier in the start of preamble is combined with so much noise that it cannot be distinguished by the PHY controller, then PHY will put a false carrier packet on the MII bus. If two consecutive false carrier events occur on a FastMPR port or a false carrier event occurs and lasts for a time that exceeds the default value of the false timer register, the port will be forced into isolation mode and its transmit/receive path will be inhibited.

A port in the isolation state will return to operating state when the medium is idle for more than the summation of the set value of the idle timer and IPG timer or when both the carrier is absent and the valid carrier timer has timed out.

PCS CODE GROUP <4:0>	CODE NAME	MII (TXD/RXD) <3:0>	REMARK
11110	0	0000	Data 0
01001	1	0001	Data 1
10100	2	0010	Data 2
10101	3	0011	Data 3
01010	4	0100	Data 4
01011	5	0101	Data 5
01110	6	0110	Data 6
01111	7	0111	Data 7
10010	8	1000	Data 8
10011	9	1001	Data 9
10110	A	1010	Data A
10111	B	1011	Data B
11010	C	1100	Data C
11011	D	1101	Data D
11100	E	1110	Data E
11101	F	1111	

Continued

11111	I	Undefined	IDLE; used as interstream fill code
11000	J	0101	Start-of-stream Delimiter
10001	K	0101	Start-of-sream Delimiter
01101	T	Undefined	End-of-sream Delimiter
00111	R	Undefined	End-of-sream Delimiter

4B/5B Code Group

MII Management

The FastMPR provides a set of configuration registers, accessible through the MDC and MDIO pins on the MII serial management bus. The FastMPR can thus be managed through the MDC and MDIO pins. For the FastMPR to be configured by programming these registers or setting hardware jumpers, an external serial command generator is needed to generate an MII management frame format command (shown in the following table) to drive MDC with a minimum 400 nS clock period so that the data train is latched on the MDIO. The typical read and write timing of the serial interface is shown in the diagram below (Figure 8 and Figure 9).

	MII MANAGEMENT PROTOCOL							
	PRE	**ST**	**OP**	**PHYAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1... 1	01	10	AAAAA	RRRRR	Z0	16 bits	Z
Write	1... 1	01	01	AAAAA	RRRRR	10	16 bits	Z

Management Frame Format Table

Note:

PRE: Preample; ST: Start of Frame; OP: Operation code; PHYAD: PHY address; REGAD: register address.
TA: Turnaround.

Typical MDIO/MDC Read Cycle

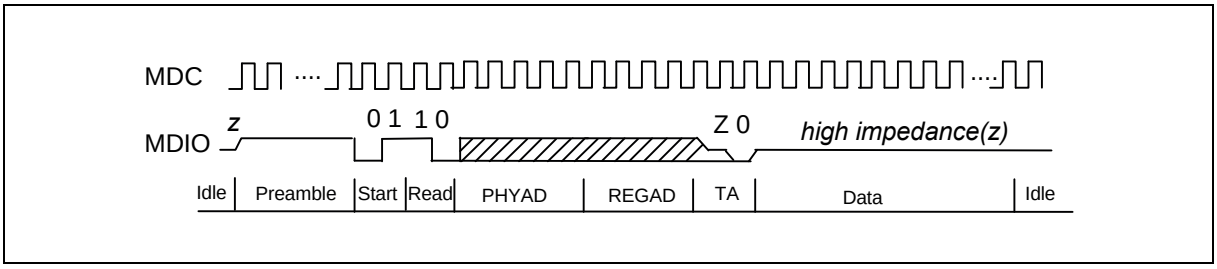


Figure 8

Typical MDIO/MDC Write Cycle

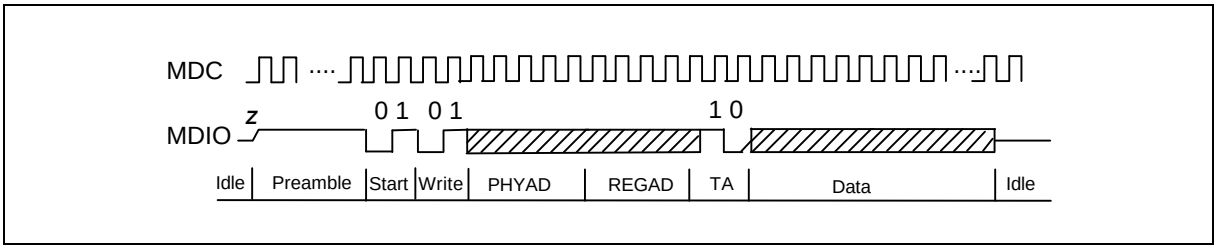


Figure 9

The FastMPR implements a total of 3 MII registers for users. Each function is described as follows:

NORMAL COMMAND REGISTERS				
REGISTER	**BIT**	**NAME**	**R/W**	**DESCRIPTION**
0	0–11	Port_Disable	R/W	TP0–10 and extension port are enabled when these bits are reset. TP0–10 and extension port are disabled when these bits are set.
0	12	SRAM_Select0	R/W	64K byte SRAM size is selected when this bit is reset. 128K byte SRAM size is selected when this bit is set.
0	13	SRAM_Select1	R/W	32 KB × 8 × 2 or 64 KB × 8 × 2 SRAM interfaceis selected when this bit is reset. 64 KB × 8 × 1 or 128 KB × 8 × 1 SRAM interface is selected when this bit is set.
0	14	Bridge_Disable	R/W	Extension port function is enabled when this bit is reset Extension port function is disabled when this bit is set.
0	15			Reserved.
1	0–11	Partition_status	R	Bit 0–11 show the partition status of TP0–10 ports and extension port. TP0–10 and extension port are connected when these bits are reset. TP0–10 and extension port are partitioned when these bits are set.
1	12–15			Reserved.
2	0–11	Jabber_status	R	Bit 0–11 show the jabber status of TP0–10 ports and extension port. TP0–10 and extension port are in jabber when these bits are set.
2	12–15			Reserved.

Notes:

1. The bit 11 of registers 1, 2 reports the partition, jabber. These status functions are reported only when the extension port is disabled.
2. "R" means read only, "W" means write only, "R/W" means read/write.

Port Status Direct Report

The port status direct report is the easiest way to obtain information on the network status. The FastMPR XCOLRPT output pin provides a collision status report. Four pins (M0–3) are used to select the type of status report and latching. Twelve pins, TP0–10RPT and BTPRPT, report the port status. Each pin can sequentially report four aspects of the port status: link/activity, partition, utilization, and jabber. The XCOLRPT report is asserted whenever a collision occurs in the FastMPR. Pins M0–3 determine the aspect of the network status reported on the twelve port status pins. The FastMPR reports the network status to a set of LEDs, which are driven through an external driver IC.

The timing chart for the status display pins M0–3 versus the port status data train is shown in the figure below.

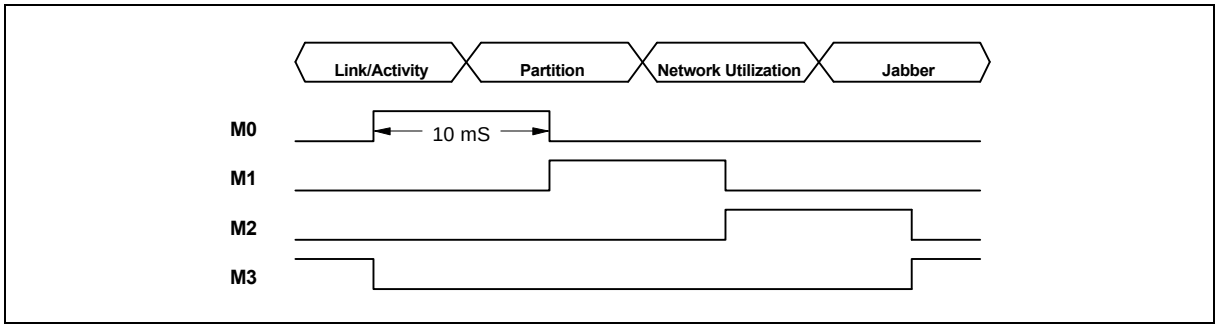


Figure 10

As the figure above shows, the LED report can be easily implemented. Each of the port status report pins outputs the port status and is sequentially latched by an external IC at the rising edge of the M0–3 pulse.

In the TP link/activity report section, a low output from TP0–10RPT and BTPRPT indicates that the TP ports and the extension port are in link good state. A high output indicates that the TP ports and extension port are not in link good state, and the LED is lit. If a data frame is passing through the port, a 10 Hz signal with a half duty cycle is output to flash the LEDs through a driving circuit to show that the TP port is receiving packets. Note that when the TP ports have incoming packets, the link/activity signal is still reported even if the ports are partitioned or disabled.

In the partition status report section, a high output from TP0–10RPT means the traffic on each FastMPR port connected to a network segment or a node is flowing smoothly. A low output on TP0–10RPT means the TP ports are in the partition state, and BTPRPT is undefined during this time. In this mode, the LED will be kept on when a port is partitioned.

In the network utilization report status section, TP0–9RPT will output the network utilization status, and the TP10RPTand BTPRPT pins are undefined. The Winbond FastMPR uses a proprietary technique to smoothly control the network utilization display, which is usually handled by the CPU. The FastMPR counts every bit, including preamble, runt packets, and so on, running over the media, so that it can display practical information on network utilization. It samples this counted value every 40 mS to determine which LEDs should be lit, so that the LED will be lit on or off in a smooth and ordering fashion. The relationship between utilization and the LEDs is described in the table below.

In the jabber status report section, a low output from the TPnRPT (n = 0, 1, ..., 10) pins indicates the TP ports are in the jabber state. A high output indicates the TP ports are not in the jabber state. At this time, BTPRPT has no function. When the extension port is disabled, the output behavior of BTPRPT will be the same as that of TP0–10RPT.

The pin/utilization report combinations are shown in the following table:

PIN/UTILIZATION REPORT	0%	10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
TP0RPT	1	0	0	0	0	0	0	0	0	0	0
TP1RPT	1	1	0	0	0	0	0	0	0	0	0
TP2RPT	1	1	1	0	0	0	0	0	0	0	0
TP3RPT	1	1	1	1	0	0	0	0	0	0	0
TP4RPT	1	1	1	1	1	0	0	0	0	0	0
TP5RPT	1	1	1	1	1	1	0	0	0	0	0

Continued

TP6RPT	1	1	1	1	1	1	1	0	0	0	0
TP7RPT	1	1	1	1	1	1	1	1	0	0	0
TP8RPT	1	1	1	1	1	1	1	1	1	0	0
TP9RPT	1	1	1	1	1	1	1	1	1	1	0

Network Utilization vs LED Status

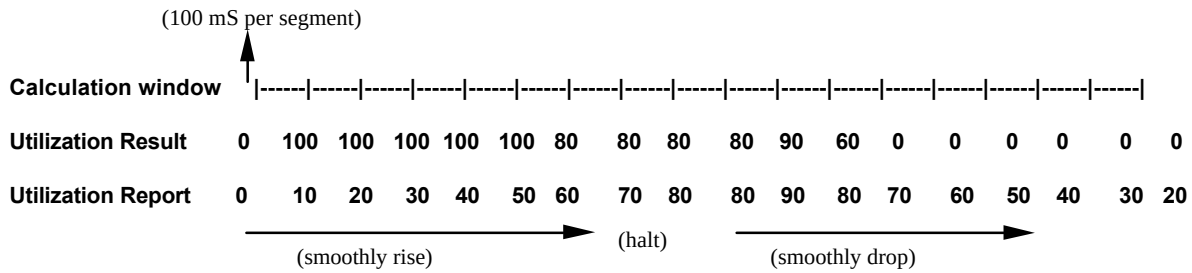


Figure 11

Note: "Halt" means that the utilization report cannot be larger than the real network utilization result.

Inter-FastMPR Interface

The FastMPR implements the inter-FastMPR interface for large scale repeater applications. Up to 6 FastMPRs can be put in to one repeater unit using the inter-FastMPR interface integrator. An extra integrator is needed to handle hub cascading. The inter-FastMPR interface is composed of IDAT<3:0>, $\overline{\text{ICRS}}$, $\overline{\text{IBEN}}$, $\overline{\text{ICOL}}$, IJAM, IERR, and IDCLK.

The inter-FastMPR interface adopts asynchronous operation, a frequency-phase-independent technique. Regardless of whether a single or multiple oscillator frequency source is used, the FastMPR cascades or stacks easily and each FastMPR connected to the inter-FastMPR interface integrator works well.

IDCLK is used to synchronize the data IDAT<3:0> transferred between FastMPRs. IERR is used to indicate that the repeated data contain errors. IERR also propagates this error message to other FastMPRs. $\overline{\text{ICRS}}$ is used to output the FastMPR carrier to the integrator.

When the FastMPR receives $\overline{\text{IBEN}}$ after $\overline{\text{ICRS}}$ is asserted, the FastMPR that asserted $\overline{\text{ICRS}}$ will put the transmitted data into IDAT<3:0> and propagates it to the inter-FastMPR interface integrator. If the FastMPR does not issue an $\overline{\text{ICRS}}$ assertion but receives $\overline{\text{IBEN}}$ from the integrator, the FastMPR is ready to receive data from the integrator. If the integrator receives more than one $\overline{\text{ICRS}}$ asserted from different FastMPRs, it will pull $\overline{\text{ICOL}}$ low so that all the FastMPRs connected to the integrator can detect that a collision event has occurred. At this time, the FastMPR that asserted $\overline{\text{ICRS}}$ will append IJAM to the inter-FastMPR interface integrator.

Extension Port Functions

The Fast Ethernet class 2 architecture has a limit of 205 meters. This means that the maximum length allowed between two 100BaseTX repeaters is only 5 meters. The W89C880F implements an extension port to overcome this limitation while maintaining a setup similar to 10Base-T Ethernet. The

extension port functions extend the distance between two 100BaseTX repeaters and partition the traffic and collisions among Fast Ethernet hubs. The extension port function is optional; the default setting is enabled. The extension port can also be disabled so that it functions as a normal port. To disable the extension port, place a 10K ohm pull-high resistor on the pin TP5RPT/DISBG, and power it on. When the extension port is disabled, the extension port MII interface acts as a normal MII port.

The extension port function is described below.

Frame Buffer Interface

The extension port provides three types of SRAM interfaces, 32K × 8, 64K × 8, and 128K × 8 SRAM, and two optional SRAM buffer sizes, 64K bytes and 128K bytes. The default SRAM buffer size is 64 KB, and the default SRAM interface is 32 KB × 8.

The SRAM buffer size and SRAM interface are programmable and are controlled by TP6RPT/SRAMsel0 and TP7RPT/SRAMsel1, respectively. If a 10K ohm pull-high resistor is connected to the pin TP6RPT/SRAMsel0, the SRAM buffer size will be 128 KB; otherwise, it is 64 KB. If a 10K ohm pull-high resistor is connected to the pin TP7RPT/SRAMsel1, the SRAM buffer interface will support one SRAM chip; otherwise, it will support two chips. The combinations permitted are listed in the table below.

	TP6RPT	TP6RPT +10KΩ	TP7RPT	TP7RPT +10KΩ
Buffer size	64 KB	128 KB		
Buffer interface			2s SRAM	1 SRAM

SRAM Configuration Table

Store and Forward

If enabled, the extension port will store packets in the buffer when the network segment on the other side of the extension port is busy. Once a complete packet is received and the opposing network segment is quiet, the packet will be forwarded. While the packet is being forwarded, any collision will abort the operation and force the FastMPR to enter a backoff period. When the backoff time has elapsed, the extension port reattempts to transmit the packet until the operation is successful or the backoff time is truncated. If the buffer is empty and the opposing network is quiet, the packet transmitted will pass directly through the port and will not be stored in the SRAM buffer.

Not all packets can be forwarded; forwarding depends on the contents of the address filtering table. If the destination node, which has registered its address to the extension port, is located on the same side as the source node, the packet will not be stored and forwarded.

Fragment-free Window

The extension port directly forwards a packet if the length of the received packet exceeds the value set in the fragment-free window and if the opposed network segment is quiet. Otherwise, the packet will be stored in the buffer.

The fragment-free function discards bad packets caused by a CRC error, alignment error, or receive error, long packets (longer than 1518 bytes), and runt packets caused by collision events.

Learning and Filtering

The extension port provides two internal hash tables with 128 address entries each for learning and filtering. One table is used for the source address, and the other for the destination address. After power on, the extension port resets the two address tables and starts to fill the address table by extracting the source address and the destination address from the received packet through a mapping function. About 40 minutes after power on, the FastMPR begins the address filter function.

At this time, a packet with a destination address that matches an address in the destination address table will pass through the extension port to the opposing network segment. Otherwise, the packet will not be stored and forwarded.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYM.	MINIMUM	MAXIMUM	UNIT
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_S	-55	150	°C
Supply Voltage	V_{DD}	-0.5	7.0	V
Input Voltage	V_{IN}	VSS -0.5	V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} -0.5	V_{DD} +0.5	V
Lead Temperature (soldering 10 seconds maximum)	T_I	-55	250	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Power Supply

(V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, T_A = 0° C to 70° C)

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Power Supply Current (idle)	I_{DDI}	-	150	mA
Power Supply Current	I_{DDL}	-	250	mA

DC CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0° C to 70° C)

Digital

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
Low Input Voltage	V_{IL}	V_{SS} -0.5	0.8	V
High Input Voltage	V_{IH}	3.85	V_{DD} +0.5	V
Low Output Voltage (V_{DD} = 4.5V)	V_{OL}		0.4	V
High Output Voltage (V_{DD} = 4.5V)	V_{OH}	2.4		V
Input Leakage Current (Note 1)	I_{IL1}		10	µA
Input Current (Note 2)	I_{IL2}		500	µA
Output Leakage Current (V_{DD} = 5.5V)	I_{OL}		10	µA

Notes:

1. All of the input pins except those stated in Note 2.

2: TEST, $\overline{\text{IBEN}}$, $\overline{\text{ICOL}}$ these pins had been pull low or pull high.

MII Interface

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT

Low Input Voltage	V_{IL}		0.8	V
High Input Voltage	V_{IH}	2		V
Low Output Voltage (at I_{OL} = 24 mA)	V_{OL}		0.4	V
High Output Voltage (at I_{OH} = -24 mA)	V_{OH}	2.4		V
Input High Current (V_I = 5.25V) (Note)	I_{IH1}		200	µA
MDC Input High Current (V_I = 5.25V)	I_{IH2}		20	µA
MDIO Input High Current (V_I = 5.25V)	I_{IH3}		3000	µA
Input Low Current (V_I = 0V) (Note)	I_{IL1}	-20		µA
MDC Input Low Current (V_I = 0V)	I_{IL2}	-20		µA
MDIO Input Low Current (V_I = 0V)	I_{IL3}	-180		µA
Output Leakage Current (V_{DD} = 5.5V)	I_{OL}		10	µA

Note:
All of the MII input pins except MDC, MDIO pins input low/high current.

SRAM Read

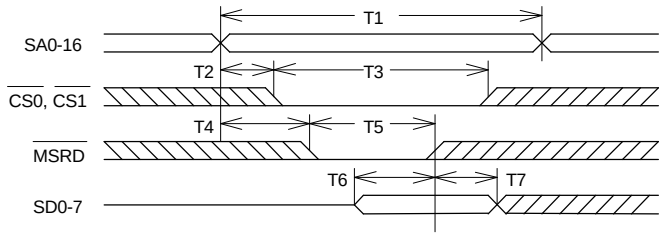


Figure 12

SYMBOL	DESCRIPTION	MIN	TYP.	MAX	UNIT
T1	Read cycle time	30			nS
T2	Address valid to chip select valid delay time			1	nS
T3	$\overline{CS0}$, $\overline{CS1}$ command width	30			nS
T4	Address valid to read command valid delay time			6	nS
T5	$\overline{MSRD}$ command width	15			nS
T6	SD0-7 setup time	3			nS
T7	SD0-7 hold time	3			nS

SRAM Write

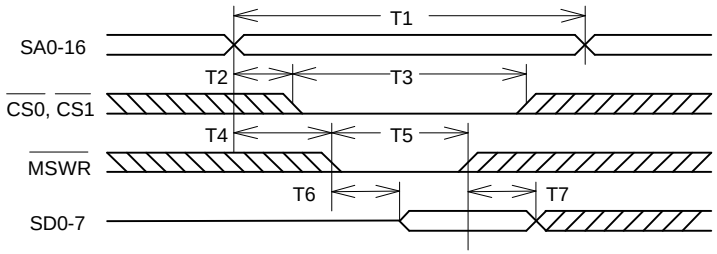


Figure 13

SYMBOL	DESCRIPTION	MIN	TYP.	MAX	UNIT
T1	Write cycle time	30			nS
T2	Address valid to chip select valid delay time			1	nS
T3	$\overline{CS0}$, $\overline{CS1}$ command width	30			nS
T4	Address valid to write command valid delay time			6	nS
T5	$\overline{MSWR}$ command width	15			nS
T6	$\overline{MSWR}$ active to SD0-7 valid delay time			2	nS
T7	$\overline{MSWR}$ inactive to SD0-7 inactive delay time	3			nS

AC CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0° C to 70° C)

MII Interface Input Timing

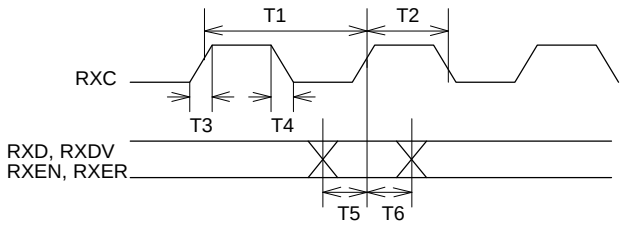


Figure 14

SYMBOL	DESCRIPTION	MIN	TYP.	MAX	UNIT
T1	RXC clock cycle	39.996	40	40.004	nS
T2	RXC clock high time	14	20	26	nS
T3	RXC rise time			4	nS
T4	RXC fall time			4	nS
T5	MII input setup time	10			nS
T6	MII input hold time	10			nS

MII Interface Output Timing

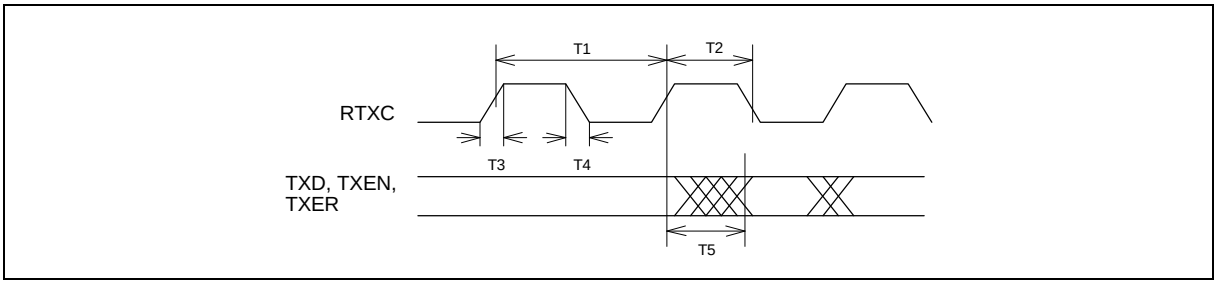


Figure 15

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T1	RTXC clock cycle	39.996	40	40.004	nS
T2	RTXC clock high time	14	20	26	nS
T3	RTXC rise time			4	nS
T4	RTXC fall time			4	nS
T5	RTXC to MII signal output delay time	0		25	nS

MII Management Output Timing

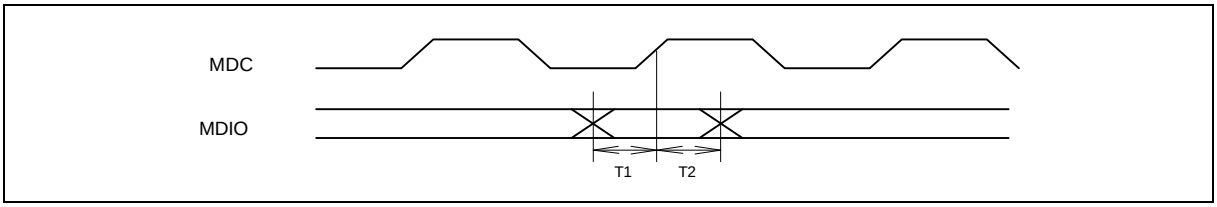


Figure 16

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T1	MII management output setup time	10			nS
T2	MII management output hold time	10			nS

MII Management Input Timing

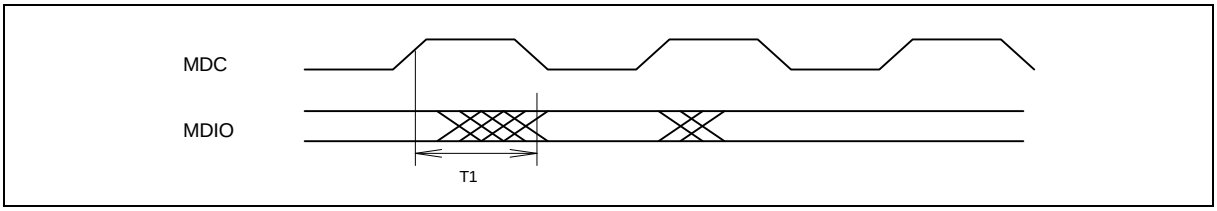


Figure 17

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T1	MII management input delay time	0		300	nS

MII Port Receive Timing

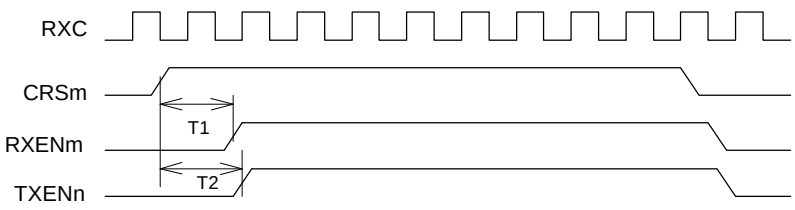


Figure 18

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T1	CRS input to RXEN output delay time		8	10	BT
T2	CRS in to TXEN out propagation delay		12		BT

MII Port Collision Propagation Delay Timing

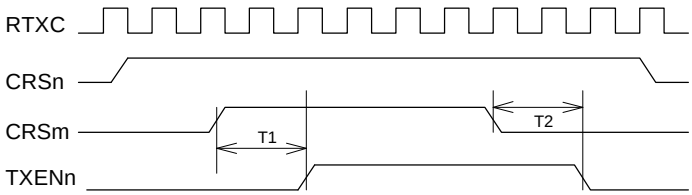


Figure 19

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T1	Second CRS input to TXEN (jam) output delay time		12		BT
T2	Second CRS end to TXEN (jam) end delay time		12		BT

MII Port Transmit Timing

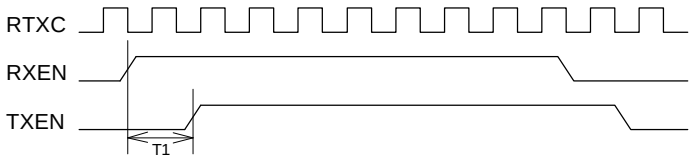


Figure 20

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T1	RXEN active to TXEN output delay		40		nS

Inter-FastMPR Interface Input Timing

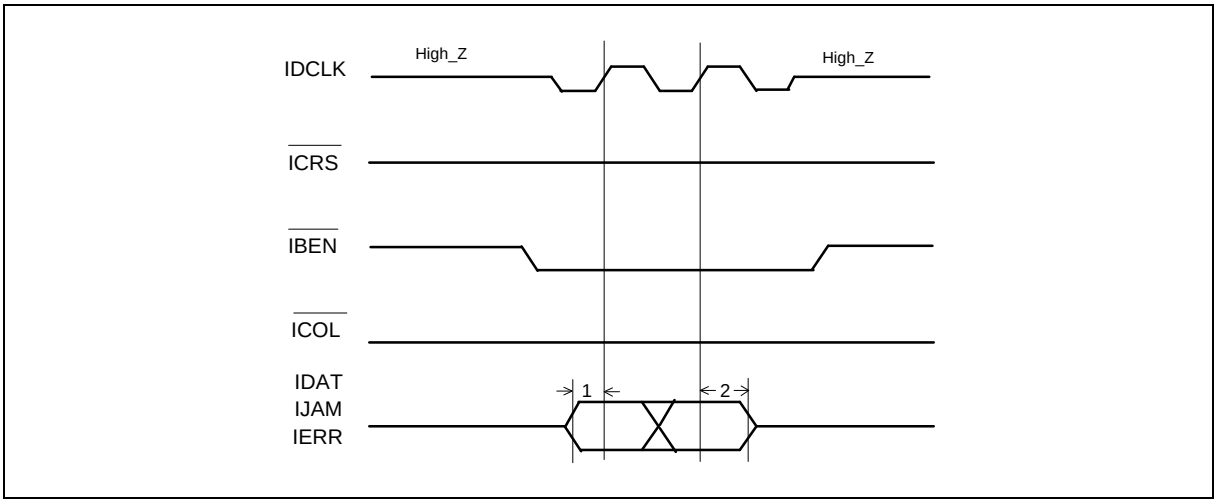


Figure 21

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
1	IDAT/IJAM/IERR to IDCLK setup time	5		35	nS
2	IDAT/IJAM/IERR to IDCLK hold time	5		35	nS

Inter-FastMPR Interface Output Timing

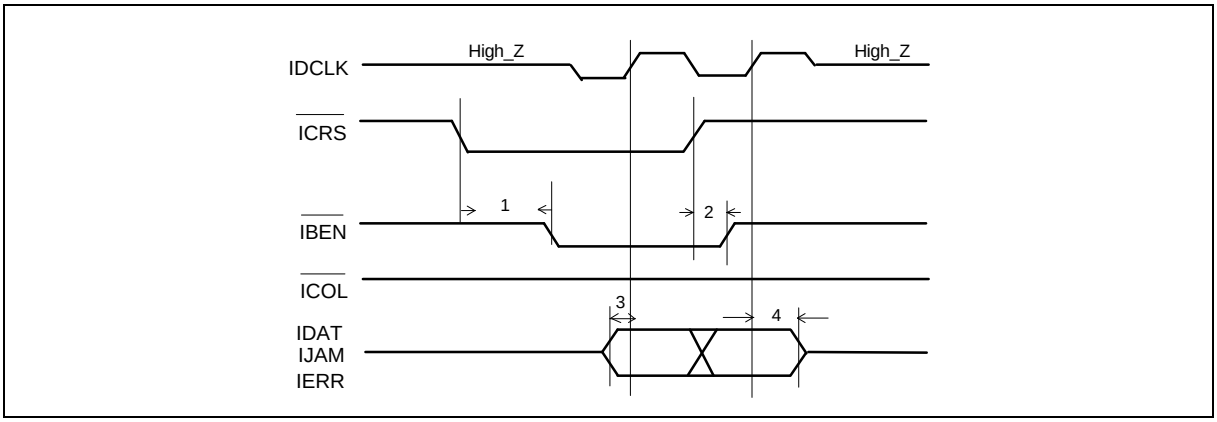


Figure 22

NO.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
1	$\overline{\text{ICRS}}$ asserted to $\overline{\text{IBEN}}$ asserted			20	nS
2	$\overline{\text{ICRS}}$ deasserted to $\overline{\text{IBEN}}$ deasserted			20	nS
3	Transmit-out IDAT/IJAM/IERR setup time to transmit-out IDCLK rising	13			nS
4	Transmit-out IDAT/IJAM/IERR hold time from transmit-out IDCLK rising	13			nS

Inter_FastMPR Interface Propagation Delay

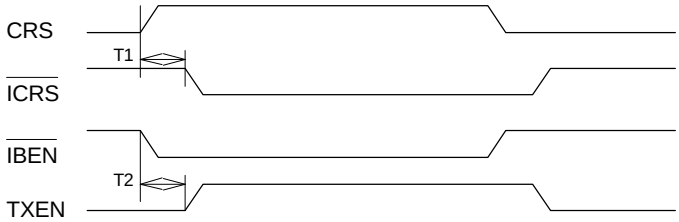


Figure 23

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T1	MII to Inter-FastMPR interface propagation delay		16		BT
T2	Inter-FastMPR interface to MII propagation delay		12		BT

Digital Output Switching Test Load

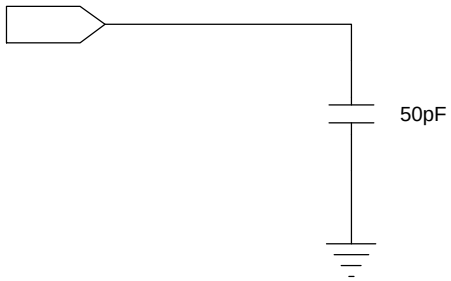


Figure 24

MII Output Switching Test Load

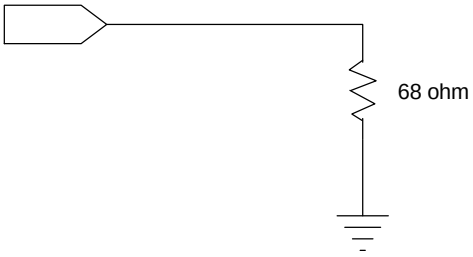
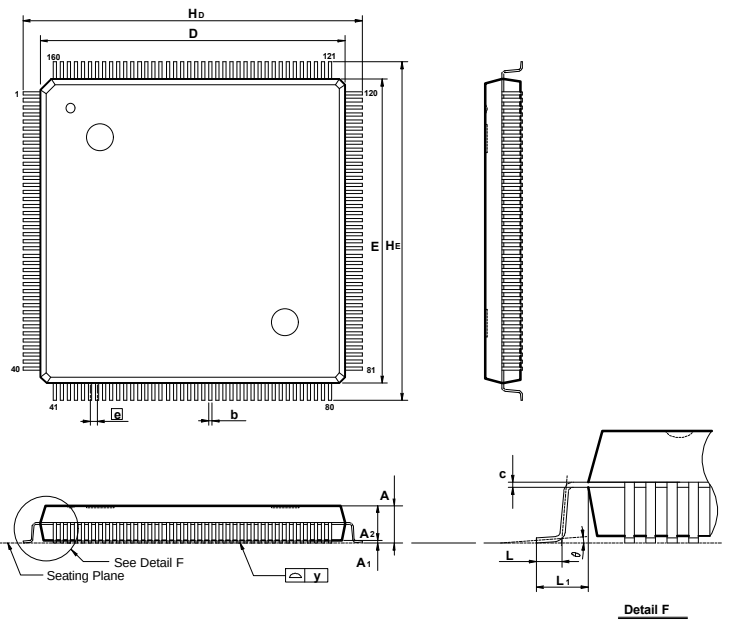


Figure 25

PACKAGE DIMENSIONS

160-pin PQFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.145	—	—	3.68
A_1	0.004	—	—	0.10	—	—
A_2	0.122	0.127	0.132	3.10	3.23	3.36
b	0.010	0.012	0.016	0.25	0.30	0.40
c	0.004	0.006	0.010	0.10	0.15	0.25
D	1.097	1.102	1.107	27.87	28.00	28.13
E	1.097	1.102	1.107	27.87	28.00	28.13
e	0.020	0.026	0.032	0.50	0.65	0.80
H_D	1.216	1.228	1.240	30.90	31.20	31.50
H_E	1.216	1.228	1.240	30.90	31.20	31.50
L	0.023	0.031	0.039	0.60	0.80	1.00
L_1	0.055	0.063	0.071	1.40	1.60	1.80
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

Figure 26

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