Designing RC Oscillator Circuits with Low Voltage Operational Amplifiers and Comparators for Precision Sensor Applications

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APPLICATION NOTE

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INTRODUCTION

The design of RC operational amplifier oscillators requires the use of a formal design procedure. In general, the design equations for these oscillators are not available; therefore, it is necessary to derive the design equations symbolically to select the RC components and to determine the influence of each component on the frequency of oscillation. A design procedure will be shown for two state variable oscillator circuits that can be used in precision capacitive sensor applications. These two oscillators have an output frequency proportional to the product of two capacitors (C_1*C_2) and the ratio of two capacitors (C_1/C_2).

The state variable oscillators have been built using ON Semiconductor's new family of sub–1 volt operational amplifiers and comparators. The MC33501, MC33503, and NCS2001 operational amplifiers, and the NCS2200 comparator are the industry's first and only commercially available analog components that are specified at a voltage of 0.9 volts. These components can be powered from a single NiCd, NiMH or alkaline battery cell. The wide operating temperature range of –40°C to +105°C makes these devices suitable for a wide range of applications.

ON Semiconductor's family of low voltage operational amplifiers and comparators help solve the analog limitations that have resulted from the industry's movement to low power supply voltages. The ON Semiconductor family of analog components provide a solution for the analog I/O interface circuits that are required for emerging low voltage DSP and microcontroller ICs.

There are a number of advantages that result from lowering the power supply voltage such as lower power consumption and the reduction of multiple power supplies. Low voltage analog design also results in new challenges for the designer and care must be taken to transfer existing higher voltage circuits to the lower voltage levels. For example, device parameters such as the bandwidth and slew rate decrease as the voltage is reduced and are modest in comparison to traditional devices operating at voltages such as ±10 V. Also, there is a limited voltage swing range available at low voltages; however, this problem is minimized by the rail–to–rail single voltage range of both the input and output signals of the ON Semiconductor devices.

The MC33501 and MC33503 are designed with a BiCMOS process, while the NCS2001 and NCS2200 are implemented with a full CMOS process. The main attributes of these devices are their low voltage operation and a full rail–to–rail input and output range. The rail–to–rail operation is provided by using a unique input stage that is formed by a folded cascade N–channel depletion mode differential amplifier. A simplified schematic of the MC33501 and MC33503 is shown in Figure 1.

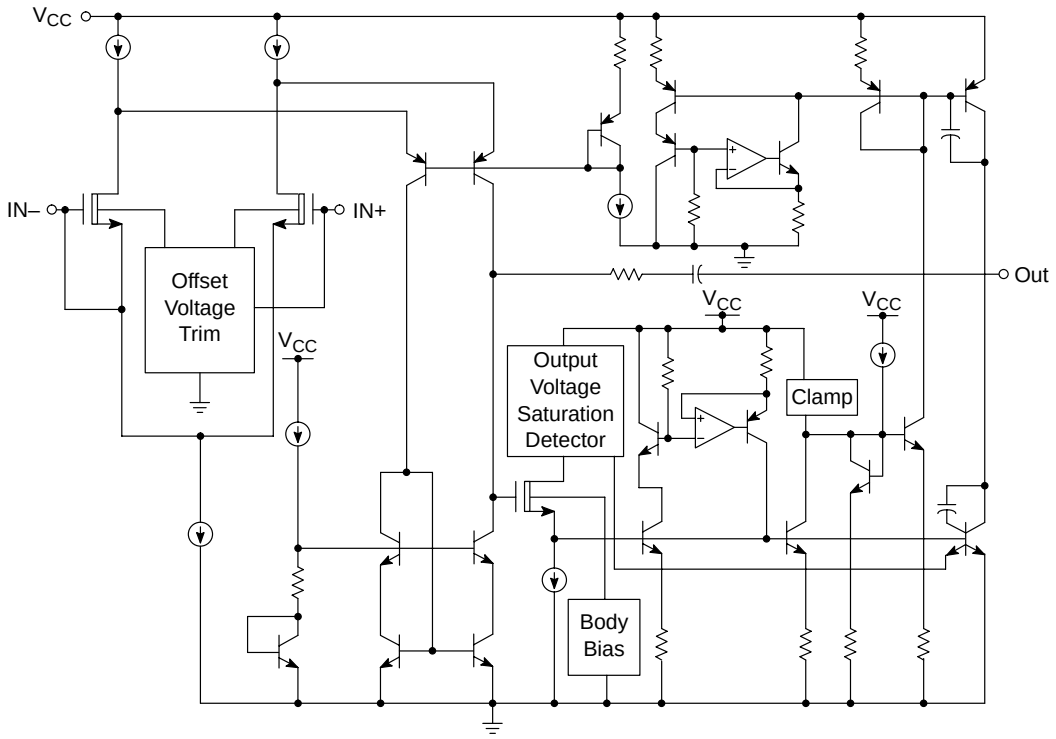


Figure 1. Simplified Schematic of the MC33501/MC33503

ON Semiconductor's Family of Low Voltage Operational Amplifiers and Comparators

Part Number	Component	Process	Features	Package	Availability
MC33501 MC33503	Operational Amplifier	BiCMOS	@ Single Supply Operation of 1.0 V ● Gain Bandwidth Product = 3 MHz (typ.) ● Open Loop Voltage Gain = 90 dB (typ.)	TSOP–5	Available NOW Production Release 4Q2000
NCS2001	Operational Amplifier	CMOS	@ Single Supply Operation of 0.9 V ● Gain Bandwidth Product = 1.1 MHz (typ.) ● Open Loop Voltage Gain = 90 dB (typ.)	TSOP–5	Available NOW Production Release 1Q2001
NCS2200	Comparator	CMOS	@ Single Supply Operation of 1.0 V ● Propagation Delay 1.1 μs (typ.) ● Complementary or Open Drain Output Configuration	TSOP–5	Product Preview Production Release 1Q2002

TRANSDUCER SYSTEM

A wide variety of different circuits can be used to accurately measure capacitive sensors. The design choices include switched capacitor circuits, analog multivibrators, AC bridges, digital logic ICs and RC operational amplifier oscillators. The requirements for a precision sensor circuit include high accuracy, reliable start–up, good long–term stability, low sensitivity to stray capacitance and a minimal component count. State variable RC operational amplifier oscillators meet all of the requirements listed above; thus, they form the basis for this study.

A block diagram of a capacitive sensor system is shown in Figure 2. The oscillation frequency is found by counting the number of clock pulses (i.e. MHz) in a time window that is formed by the square wave oscillator output (i.e. kHz) of a comparator circuit. The counter circuit can be implemented with a digital logic counter circuit or by using the Time Processing Unit (TPU) channel of a microprocessor. If necessary, temperature correction can be accomplished by implementing a curve fitting routine with data obtained by calibrating the sensor over the operating range. An analog IC sensor can be used to monitor the sensor temperature or for very precise applications a second oscillator could be built with a platinum resistive temperature device (RTD) sensor.

In addition, it is often important for the sensor system to compute the ratio of two capacitors. Calculating the ratio of the capacitors reduces the transducer's sensitivity to dielectric errors from factors such as temperature. In other cases, such as in an air data quartz ΔP pressure sensors, the desired measurement is equal to the ratio of two capacitances (C_{MEAS} / C_{REF}). Furthermore, dual sensors are typically designed to double the C_{MEAS} in capacitance, while C_{REF} may vary less than one percent. Thus, the transducer's accuracy is increased if a circuit such as the ratio state variable oscillator can directly detect the C_{MEAS} to C_{REF} ratio.

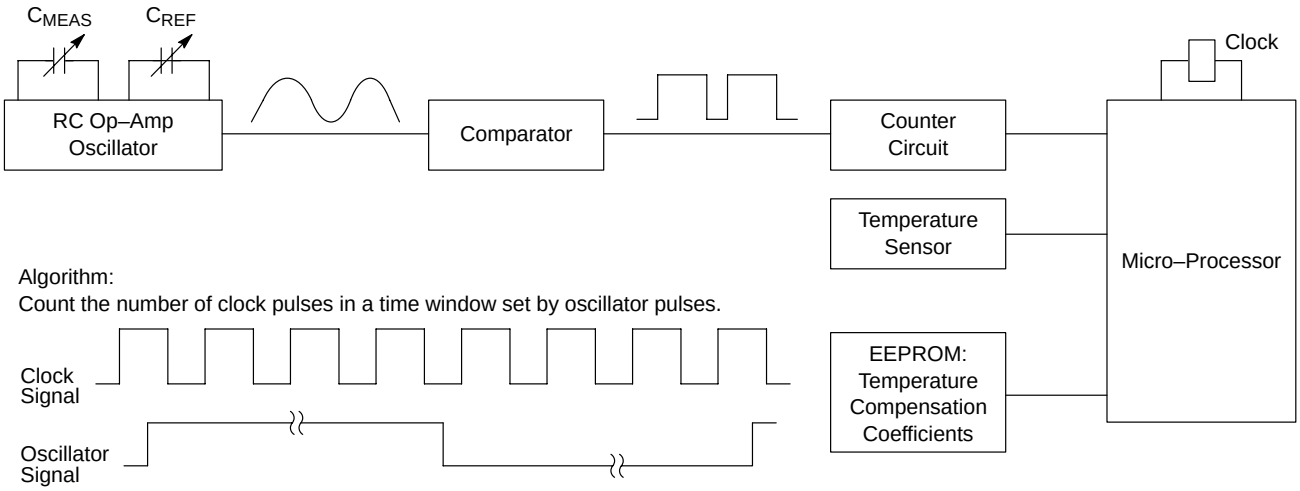
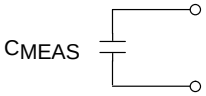
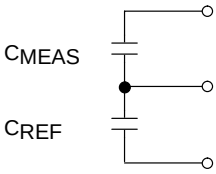
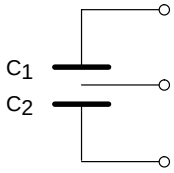


Figure 2. Block Diagram of Capacitive Sensor Application

SENSOR APPLICATIONS

RC operational amplifier oscillators can be used to accurately detect both resistive and capacitive sensors; however, this paper will only analyze capacitive applications. The three basic configurations of capacitive sensors and their attributes are shown in Table 1. The absolute and dual capacitive sensors will be used with the absolute and ratio oscillator circuits, respectively. Differential capacitive sensors typically are not used in precision applications; therefore, they will not be analyzed in this paper.

Table 1. Summary of Capacitive Sensors

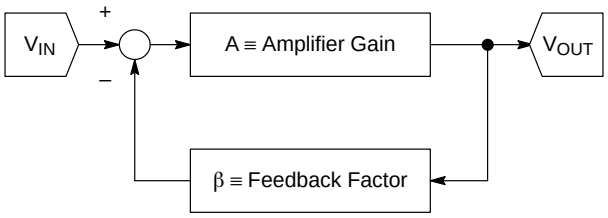
Sensor Configuration	Absolute	Dual	Differential
Schematic Representation			
Sensor Applications	• Absolute Pressure • Humidity	• Acceleration • Oil Level • Oil Quality • Differential Pressure	• Displacement • Proximity
Circuit	Absolute Oscillator	Ratio Oscillator	Typical Circuit – Multivibrator
Oscillation Frequency	freq. $\propto C_{MEAS}$	freq. $\propto \frac{C_{MEAS}}{C_{REF}}$	freq. $\propto C_1 - C_2$

OSCILLATOR THEORY

An oscillator is a positive feedback control system which does not have an external input signal, but will generate an output signal if certain conditions are met. In practice, a small input is applied to the feedback system from factors such as noise pick–up or power supply transients, and this initiates the feedback process to produce a sustained oscillation. A block diagram of an oscillator is shown in Figure 3.

The poles of the denominator of the transfer equation T(s), or equivalently the zeroes of the characteristic equation, determine the time domain behavior of the system. If T(s) has all of its poles located within the left plane, the system is stable because the corresponding terms are all exponentially decaying. In contrast, if T(s) has one pole that lies within the right half plane, the system is unstable because the corresponding term exponentially increases in amplitude. An oscillator is on the borderline between a stable and an unstable system and is formed when a pair of poles is on the imaginary axis, as shown in Figure 4.

If the magnitude of the loop gain is greater than one and the phase is zero, the amplitude of oscillation will increase exponentially until a factor in the system such as the supply voltage restricts the growth. In contrast, if the magnitude of the loop gain is less than one, the amplitude of oscillation will exponentially decrease to zero.



$$T(s) = \frac{V_{OUT}}{V_{IN}} = \frac{A}{1 - A\beta} = \frac{A}{1 - LG} = \frac{A}{\Delta s} = \frac{A}{\frac{N(s)}{D(s)}}$$

where $A \times \beta = LG \equiv$ loop gain

$\Delta s \equiv$ characteristic equation

If $V_{IN} = 0$, then $T(s) = \infty$ when $\Delta s = 0$

At the oscillation condition of $\Delta s = 0$, referred to as the Barkhausen stability criterion, $|LG| = 1$ (magnitude) and $\angle LG = 0$ (phase).

Figure 3. Block Diagram of an Oscillator

Figure 4. Pole Locations for a 2nd and 3rd Order Oscillator

CIRCUIT DESCRIPTIONS

Absolute State Variable Oscillator

The absolute state variable oscillator is used when the measurement is proportional to either one or two capacitors (i.e. freq. α C_1*C_2). The block diagram and schematic of the absolute circuit are shown in Figures 5 and 6. This circuit consists of two integrators and an inverter circuit. Each integrator has a phase shift of 90°, while the inverter adds an additional 180° phase shift; thus, a total phase shift of 360° is fed into the input of the first integrator to produce the oscillation. The first integrator stage consists of amplifier A_1, resistor R_1 and sensor capacitance C_1. The second integrator consists of amplifier A_2, resistor R_2 and sensor capacitance C_2. Resistor–capacitor combinations R_1 and C_1, and R_2 and C_2, set the gain of each integrator stage, in addition to setting the oscillation frequency. The inverter stage consists of amplifier A_3, resistors R_3 and R_4 and capacitor C_4. Capacitor C_4 is not essential for normal operation; however, it ensures oscillator startup under extreme ambient temperature conditions.

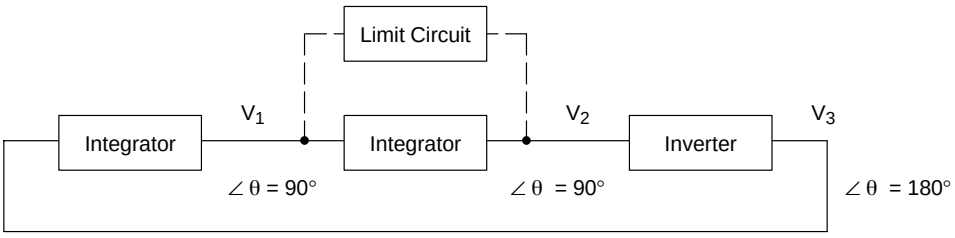
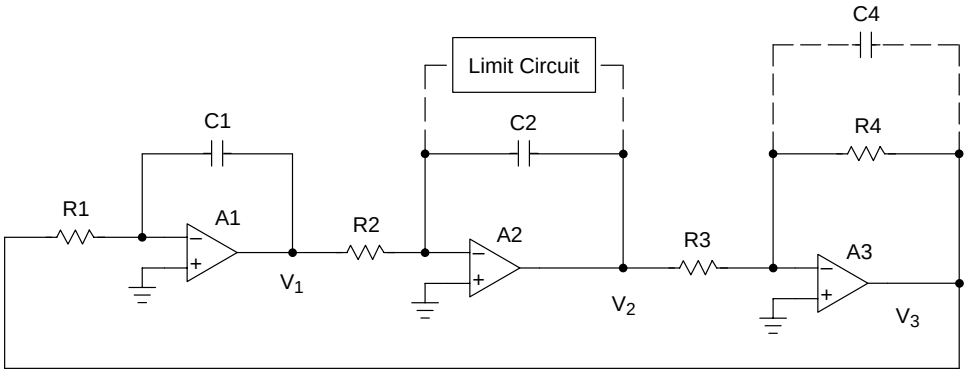


Figure 5. Absolute Oscillator Block Diagram



The absolute sensor capacitances C1 and C2 are used by the integration amplifiers.

Figure 6. Absolute Oscillator Schematic

Ratio State Variable Oscillator

The ratio state variable oscillator [6] is used for dual capacitive sensors when the oscillation frequency is proportional to the ratio of sensor capacitances C_3 and C_4 (i.e. freq. α C_3 / C_4). The block diagram and schematic of the ratio circuit are shown in Figures 7 and 8. This circuit consists of two integrators and a differentiator circuit. The integrators formed by amplifier A_1 and A_2 are identical to the integrators used in the absolute circuit. Amplifier A_3, resistors R_3, R_4 and R_5, and the sensor capacitors C_3 and C_4 form the differentiator stage which provides a 180° phase shift. The values of resistors R_3, R_4 and R_5 are selected to set the break frequencies of the differentiator stage, so that the gain of the stage is equal to $-C_3/C_4$. Resistor R_5 provides a DC current path through capacitor C_3 in order to initiate oscillation at power–up. Because R_5 is relatively large (MΩ), it can be replaced with a three resistor "Tee" network in order to use readily available resistors, as shown in Figure 9.

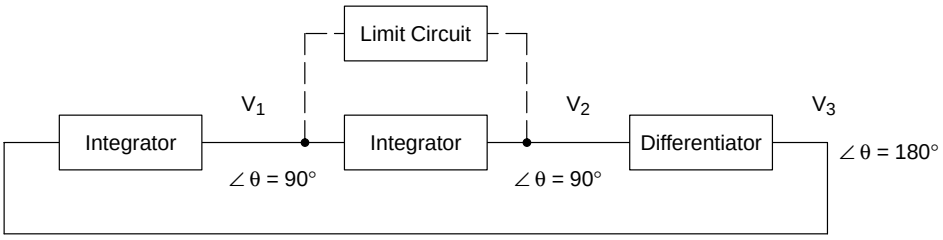
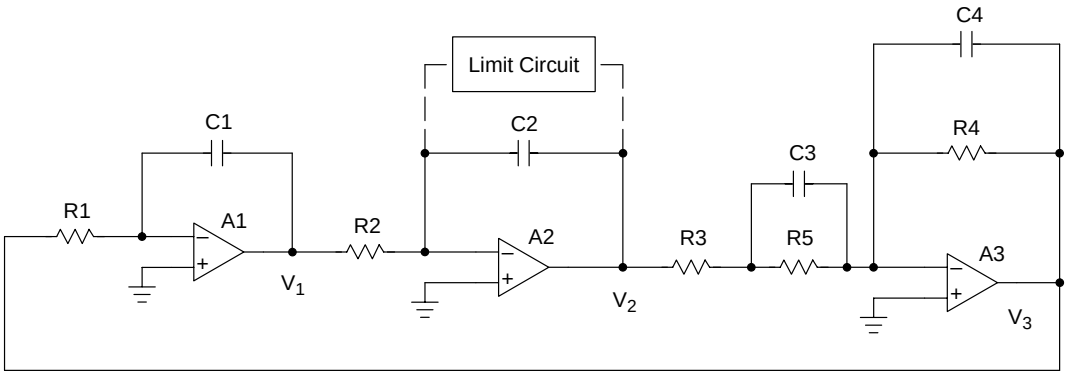
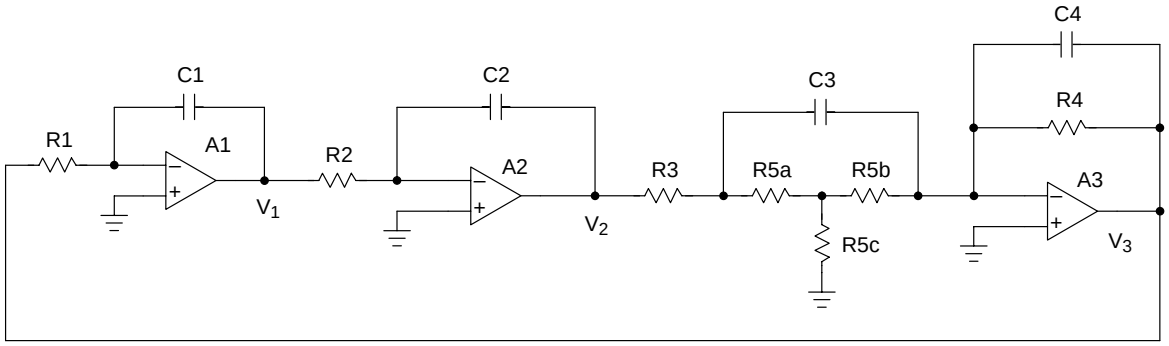


Figure 7. Ratio Oscillator Block Diagram

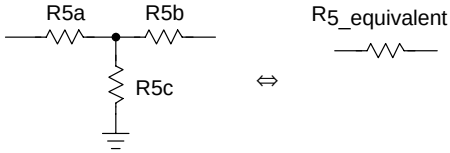


The differentiator amplifier is formed by the dual sensor capacitances C3 and C4.

Figure 8. Ratio Oscillator Schematic



A Tee network provides a method to replace a large resistor (i.e. MΩ) with three small resistors (i.e. kΩ).



$$R_{5\_equivalent} = R_{5a} + R_{5b} + \frac{R_{5a}R_{5b}}{R_{5c}}$$

Figure 9. Ratio Oscillator Schematic with R5 Tee Network

OSCILLATOR DESIGN PROCEDURE

Listed below is a procedure to design RC active oscillators:

Step 1: Find LG and Δs

Step 2: Solve Δs = 0 for s = jω$_o$ using methods I, II or III

Method I: Solve remainder of $\frac{N(s)}{s^2 + \omega_o^2} = 0$

Method II: Solve N(jω$_o$)$_{REAL}$ = N(jω$_o$)$_{IMAG}$ = 0

Method III: Routh's stability test

Step 3: Form sub–circuit design equations

Step 4: Verify LG ≥ 1

Step 1: Find LG and Δs

The oscillation frequency is determined by finding the poles of the denominator of the transfer equation T(s), or equivalently the zeroes of the numerator N(s) of the characteristic equation Δs. Mason's Reduction Theorem, shown in Appendix I, provides a method of determining the transfer equation from a signal flow diagram. Mason's Theorem, listed below, shows that it is not necessary to obtain the complete T(s) equation. The oscillation frequency can be determined by analyzing the numerator N(s) of the Δs. Δs is found by obtaining the open loop gain (LG) by breaking the feedback loop and applying a test voltage to the circuit.

$$T(s) = \frac{A}{1 - LG} = \frac{A}{\Delta(s)} = \frac{A}{\left(\frac{N(s)}{D(s)}\right)}$$

Step 2: Solve Δs

The second step in the procedure determines the zeroes of N(s). Several different control theory techniques such as the Bode or Nyquist stability tests can be used, or one of the three methods that are listed below. Examples of the application of the three different methods listed below will be provided.

Method I: $\frac{N(s)}{s^2 + \omega_o^2}$

An equation is established for the oscillation frequency ω$_o$ when N(s) is divided by $s^2 + \omega_o^2$ (i.e. $\frac{N(s)}{s^2 + \omega_o^2}$) and the remainder is solved to be equal to zero. Method I is easy to implement for second and third order systems, but with higher order systems the algebra can be tedious. Method I is described in [12] and is based on factoring the characteristic equation to have a $s^2 + \omega_o^2$ term. For example, when a third order system can be factored in the form $(s + \beta)(s^2 + \omega_o^2)$, the pole locations are at s = ± jω$_o$ and s = –β. Method I will be demonstrated by analyzing the absolute oscillator without the inverter capacitor C$_4$. Although the analysis of this second order system is trivial because N(s) is already in the form of $s^2 + \omega_o^2$, this method can be used for higher order circuits such as the 4th order ratio oscillator.

Method II: Solve N(jω$_o$)$_{REAL}$ = N(jω$_o$)$_{IMAGINARY}$ = 0

The oscillation equation sometimes can be determined directly from the characteristic equation by substituting s = jω$_o$ into N(s) and arranging N(jω$_o$) into its real and imaginary parts. This method is usually not feasible for fifth order and higher oscillators. This procedure is essentially a subset of the Routh test, because the first two rows of the Routh array will correspond to N(jω$_o$)$_{REAL}$ and N(jω$_o$)$_{IMAGINARY}$. If N(s) = jω$_o$ = 0, the poles of the characteristic equation will be on the imaginary axis at ±jω$_o$ with an oscillation frequency of ω$_o$. A summary of the oscillation equations for 2nd and 3rd order oscillators obtained using Method II [13] is shown in Appendix II. The application of Method II is shown for the 3rd order absolute oscillator with the inverter capacitor C$_4$.

Method III: Routh Stability Test

The Routh stability criterion [12] provides a method that determines the zeroes of the characteristic equation directly from the characteristic polynomial coefficients, without the necessity of factoring the equation. The Routh test, shown in Appendix III, is the preferred method to use for fourth order and higher order oscillators. The Routh test consists of forming a coefficient array. Next, the procedure substitutes s = jω$_o$ for s, and the summation of the row is set to zero. If the row equation produces a nontrivial solution for ω$_o$, the procedure is complete and the frequency of oscillation is equal to ω$_o$. If the row equation does not yield an equation that can be solved for ω$_o$, the procedure continues with the next row in the Routh array. Usually, it is necessary only to complete the first two or three rows of the Routh array to produce an equation that can be solved for ω$_o$. Method III will be demonstrated by analyzing the ratio oscillator.

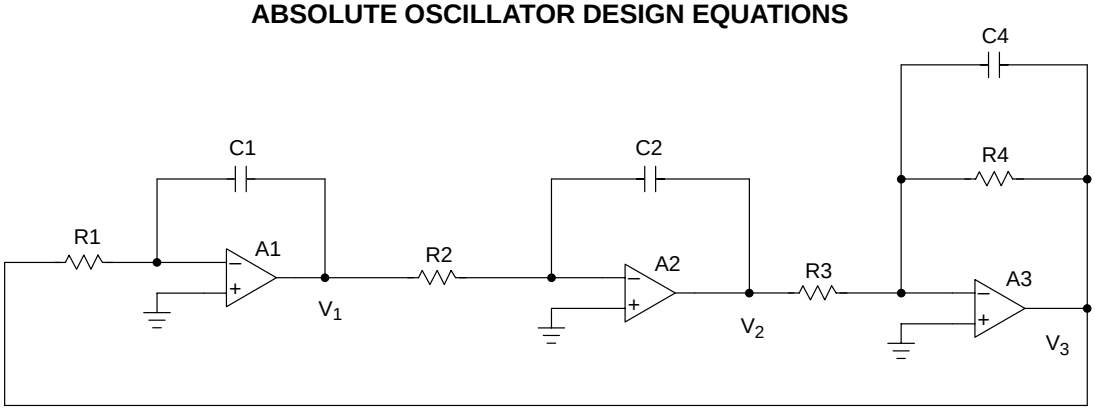
Step 3: Sub–circuit Design Equations

The third step in the design procedure is to form the design equations for the sub–circuits formed by each operational amplifier. The oscillation equation can be simplified by selecting the R's and C's with the assumptions shown in the "Design Equation" section. The amplifier gain and pole/zero locations for the absolute and ratio oscillator are also shown.

Step 4: Verify LG ≥ 1

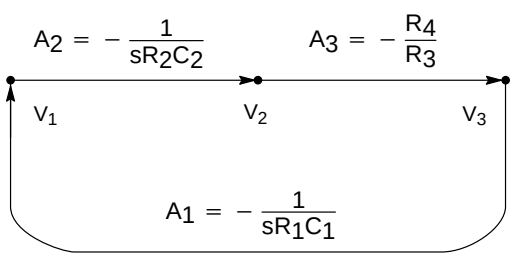
The final step in the procedure verifies that the loop gain is equal to or greater than one after the R's and C's component values have been chosen. This step is required to verify that the location and clamping voltage of the limit circuit will not result in a LG < 1, or that the operational amplifiers will reach their saturation voltage. The limit circuit can be located across any of the three amplifiers as long as the LG ≥ 1.

ABSOLUTE OSCILLATOR DESIGN EQUATIONS



Without C_4

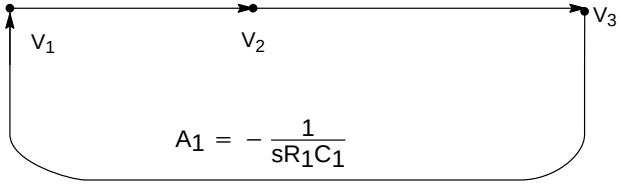
$$A_2 = -\frac{1}{sR_2C_2} \qquad A_3 = -\frac{R_4}{R_3}$$



$$A_1 = -\frac{1}{sR_1C_1}$$

With C_4

$$A_2 = -\frac{1}{sR_2C_2} \qquad A_3 = -\left[\left(\frac{R_4}{R_3}\right)\left(\frac{1}{sR_4C_4 + 1}\right)\right]$$



$$A_1 = -\frac{1}{sR_1C_1}$$

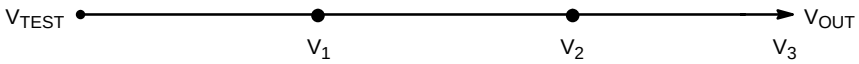
Figure 10. Absolute Oscillator Signal Flow Diagrams

Absolute Oscillator (without C_4)

Step 1: Find LG and Δs

The loop gain is found by breaking the loop and inserting a "test" voltage into the input.

$$A_1 = -\frac{1}{sR_1C_1} \qquad A_2 = -\frac{1}{sR_2C_2} \qquad A_3 = -\frac{R_4}{R_3}$$



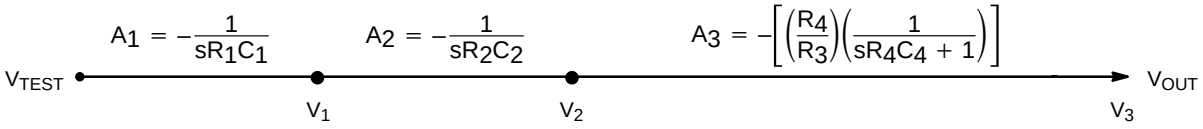
$$LG = \frac{V_{OUT}}{V_{TEST}} = A_1 \times A_2 \times A_3$$

$$\Delta s = \frac{N(s)}{D(s)} = 1 - LG = 1 - \left(-\frac{1}{sR_1C_1}\right)\left(-\frac{1}{sR_2C_2}\right)\left(-\frac{R_4}{R_3}\right) = 1 + \frac{R_4}{s^2R_1R_2R_3C_1C_2} = s^2 + \frac{R_4}{R_1R_2R_3C_1C_2}$$

$$= \frac{s^2R_1R_2R_3C_1C_2 + R_4}{s^2R_1R_2R_3C_1C_2}$$

$$N(s) = s^2R_1R_2R_3C_1C_2 + R_4$$

Absolute Oscillator (with C_4)
Step 1: Find LG and Δs
The loop gain is found by breaking the loop and inserting a "test" voltage into the input.



$$LG = \frac{V_{OUT}}{V_{TEST}} = A_1 \times A_2 \times A_3 \qquad A_3 = \frac{-Z_4}{Z_3} = \frac{R_4 \,||\, C_4}{R_3}$$

$$LG = \left(-\frac{1}{sR_1C_1}\right)\left(-\frac{1}{sR_2C_2}\right)\left[\left(-\frac{R_4}{R_3}\right)\left(\frac{1}{sR_4C_4 + 1}\right)\right] = -\frac{R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2}$$

$$\Delta s = \frac{N(s)}{D(s)} = 1 - LG = 1 + \frac{R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2}$$

$$= \frac{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2 + R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2}$$

$$N(s) = s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2 + R_4$$

Absolute Oscillator (without C_4)
Step 2: Solve N(s) using Method I

Solve Method I: Solve the remainder of: $\frac{N(s)}{s^2 + \omega_o^2}$

$$N(s) = s^2R_1R_2R_3C_1C_2 + R_4$$

$$s^2 + \omega_o^2 \;\sqrt{\begin{array}{r} R_1R_2R_3C_1C_2 \\ \hline R_1R_2R_3C_1C_2s^2 + R4 \\ -\,R_1R_2R_3C_1C_2s^2 + \omega_o^2R_1R_2R_3C_1C_2 \\ \hline R_4 - \omega_o^2R_1R_2R_3C_1C_2 \end{array}}$$

Set the remainder to equal zero and solve for ω_o: $R_4 - \omega_o^2R_1R_2R_3C_1C_2 = 0$ $\qquad \omega_o = \sqrt{\frac{R_4}{R_1R_2R_3C_1C_2}}$

Absolute Oscillator (with C_4)

Step 2: Solve N(s) using Method II shown in Appendix II: $\omega_o = \sqrt{\frac{a_3}{a_1}} = \sqrt{\frac{a_2}{a_0}}$

$$N(s) = a_0s^3 + a_1s^2 + a_2s + a_3 = s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2 + R_4$$

$$a_0 = R_1R_2R_3R_4C_1C_2C_4$$

$$a_1 = R_1R_2R_3C_1C_2$$

$$a_2 = 0$$

$$a_3 = R_4$$

$$\omega_o = \sqrt{\frac{a_3}{a_1}} = \sqrt{\frac{R_4}{R_1R_2R_3C_1C_2}}$$

Absolute Oscillator
Step 3a: Subcircuit Oscillation Design Equations

Absolute Oscillator	Without C_4	With C_4
N(s)	$R_1R_2R_3C_1C_2s^2 + R_4$	$R_1R_2R_3R_4C_1C_2C_4s^3 + R_1R_2R_3C_1C_2s^2 + R_4$
ω_o	$\sqrt{\frac{R_4}{R_1R_2R_3C_1C_2}}$	$\sqrt{\frac{R_4}{R_1R_2R_3C_1C_2}}$
Oscillation Period $P = \frac{2\pi}{\omega_o}$	$P \cong 2\pi R\sqrt{C_1C_2}$ If $R_1 = R_2 = R$ and $R_3 = R_4$	$P \cong 2\pi R\sqrt{C_1C_2}$ If $R_1 = R_2 = R$ and $R_3 = R_4$

Absolute Oscillator
Step 3b: Subcircuit Amplifier Design Equations

Absolute Oscillator	Without C_4	With C_4
Integrator A_1 Gain	$A_1 = \frac{V_1}{V_3} = -\frac{1}{sR_1C_1} = \frac{-1}{2\pi fR_1C_1}$	$A_1 = \frac{V_1}{V_3} = -\frac{1}{sR_1C_1} = \frac{-1}{2\pi fR_1C_1}$
Pole Location	$f_{p1} = \frac{1}{2\pi R_1C_1}$	$f_{p1} = \frac{1}{2\pi R_1C_1}$
Integrator A_2 Gain	$A_2 = \frac{V_2}{V_1} = -\frac{1}{sR_2C_2} = \frac{-1}{2\pi fR_2C_2}$	$A_2 = \frac{V_2}{V_1} = -\frac{1}{sR_2C_2} = \frac{-1}{2\pi fR_2C_2}$
Pole Location	$f_{p2} = \frac{1}{2\pi R_2C_2}$	$f_{p2} = \frac{1}{2\pi R_2C_2}$
Inverter A_3 Gain	$A_3 = \frac{V_3}{V_2} = -\frac{R_4}{R_3}$	$A_3 = \frac{V_3}{V_2} = -\frac{R_4}{R_3}\left(\frac{1}{sR_4C_4 + 1}\right)$
Pole Location	N/A	$f_{p3} = \frac{1}{2\pi R_4C_4}$
RC Sensitivities*	$* s^{\omega_o}_{R_1} = s^{\omega_o}_{R_2} = s^{\omega_o}_{R_3} = -s^{\omega_o}_{R_4} = s^{\omega_o}_{C_1} = s^{\omega_o}_{C_2} = -\frac{1}{2}$	$s^{\omega_o}_{R_1} = s^{\omega_o}_{R_2} = s^{\omega_o}_{R_3} = -s^{\omega_o}_{R_4} = s^{\omega_o}_{C_1} = s^{\omega_o}_{C_2} = -\frac{1}{2}$

*Sensitivity is defined as: $S^Y_X = \frac{\left(\frac{\Delta Y}{Y}\right)}{\left(\frac{\Delta X}{X}\right)} = \frac{d\ ln(Y)}{d\ ln(X)}$

Absolute Oscillator
Step 4: Verify LG ≥ 1

Step 4 will be demonstrating using the dual power supply limit circuit shown in Figure 25. The design equations are listed below.

Assume:

1.) $V_{Pos\_Limit} = V_{Neg\_Limit} = V_{Limit}$

2.) $V_2 = V_{Limit}$ (i.e. $|A_2| = V_{Limit}$)

3.) $|A_3| = R_4/R_3 = 1$

Check:

1.) Is $|LG| = A_1 \times A_2 \times A_3 \geq V_{Limit}$

$$= \left(\frac{1}{2\pi fR_1C_1}\right)(V_{Limit})\left(\frac{R_4}{R_3}\right) \geq V_{Limit}$$

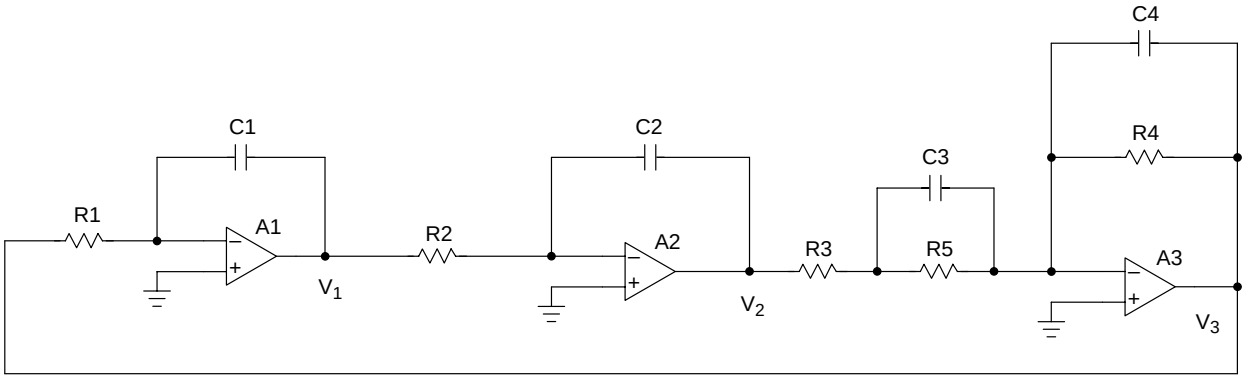
2.) Using the values shown in Figure 25,

$$\left(\frac{1}{2\pi(16.6\ kHz)(39\ K\ \Omega)\ (240\ pF)}\right)(V_{Limit})\ (1) \geq V_{Limit}$$

$$1.02\ V_{Limit} \geq V_{Limit}$$

thus the oscillation will be sustained.

RATIO OSCILLATOR DESIGN EQUATIONS



$$A_2 = -\frac{1}{sR_2C_2} \qquad A_3 = -\frac{R_4(sR_5C_3 + 1)}{(sR_3R_5C_3 + R_3 + R_5)(sR_4C_4 + 1)}$$

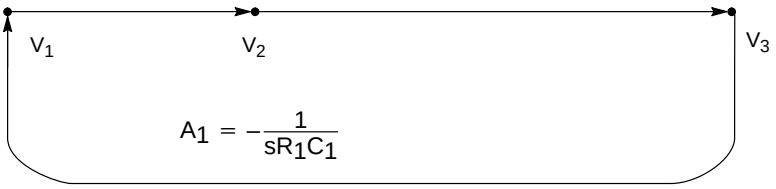


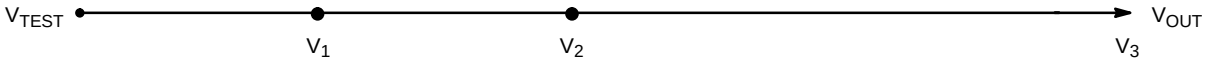
Figure 11. Ratio Oscillator Signal Flow Diagrams

Ratio Oscillator

Step 1: Find LG and Δs

The loop gain is found by breaking the loop and inserting a “test” voltage into the input.

$$A_1 = -\frac{1}{sR_1C_1} \qquad A_2 = -\frac{1}{sR_2C_2} \qquad A_3 = -\frac{R_4(sR_5C_3 + 1)}{(sR_3R_5C_3 + R_3 + R_5)(sR_4C_4 + 1)}$$



$$LG = \frac{V_{OUT}}{V_{TEST}} = A_1 \times A_2 \times A_3 \qquad A_3 = \frac{-Z4}{Z_3} = \frac{R_4 \parallel C_4}{R_3 + (C_3 \parallel R_5)}$$

$$LG = \left(-\frac{1}{sR_1C_1}\right)\left(-\frac{1}{sR_2C_2}\right)\left(-\frac{R_4(sR_5C_3 + 1)}{(sR_3R_5C_3 + R_3 + R_5)(sR_4C_4 + 1)}\right)$$

$$LG = -\frac{sR_4R_5C_3 + R_4}{s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] + s^2(R_3 + R_5)(R_1R_2C_1C_2)}$$

$$\Delta s = \frac{N(s)}{D(s)} = 1 - LG = \frac{\begin{array}{c}s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] \\ + s^2(R_3 + R_5)(R_1R_2C_1C_2) + sR_4R_5C_3 + R_4\end{array}}{\begin{array}{c}s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] \\ + s^2(R_3 + R_5)(R_1R_2C_1C_2)\end{array}}$$

$$N(s) = s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] + s^2(R_3 + R_5)(R_1R_2C_1C_2) + sR_4R_5C_3 + R_4$$

Ratio Oscillator
Step 2: Solve N(s) using Method III (Routh's Stability Test) shown in Appendix III

$$N(s) = s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] + s^2(R_3 + R_5)(R_1R_2C_1C_2) + sR_4R_5C_3 + R_4$$

$$\Delta s = a_0s^4 + a_1s^3 + a_2s^2 + a_3s + a_4$$

$a_0 = R_1R_2R_3R_4R_5C_1C_2C_3C_4$ $\quad a_1 = [(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2]$

$a_2 = (R_3 + R_5)(R_1R_2C_1C_2)$ $\quad a_3 = R_4R_5C_3$

$a_4 = R_4$

Routh's Stability Test Array

Row s^4	$a_0 + a_2 + a_4$	$\Leftrightarrow$	$R_1R_2R_3R_4R_5C_1C_2C_3C_4$	$(R_3 + R_5)R_1R_2C_1C_2$	R_4
Row s^3	$a_1 + a_3$	$\Leftrightarrow$	$(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2$	$R_4R_5C_3$	

Determine when the row s^3 equation is equal to zero. $\quad a_1s^3 + a_3s = s(a_1s^2 + a_3) = 0$

Let $s = j\omega_o$:

$$-j\omega_o^3a_1 + j\omega_oa_3 = -j\omega_o(a_1\omega_o^2 - a_3) = 0 \qquad \omega_o^2 = \frac{a_3}{a_1} = \frac{R_4R_5C_3}{(R_1R_2C_1C_2)(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)}$$

Ratio Oscillator
Step 3a: Subcircuit Oscillation Design Equations

N(s)	$s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3) + (R_3R_4C_4) + (R_4R_5C_4)](R_1R_2C_1C_2) + s^2(R_3 + R_5)(R_1R_2C_1C_2) + sR_4R_5C_3 + R_4$
ω_o	$\sqrt{\frac{R_4R_5C_3}{R_1R_2C_1C_2(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)}}$
Oscillation Period $P = \frac{2\pi}{\omega_o}$	If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ $\quad P = 2\pi RC\sqrt{\left(\frac{R_3C_4}{R_5C_3} + \frac{C_4}{C_3} + \frac{R_3}{R_4}\right)}$ If $R_5 \gg R_3$ and $R_4 \gg R_3$ then $\quad P \cong 2\pi RC\sqrt{\frac{C_4}{C_3}}$

Ratio Oscillator
Step 3b: Subcircuit Amplifier Design Equations

Integrator A_1 Gain/Pole Location	$A_1 = \frac{V_1}{V_3} = -\frac{1}{sR_1C_1} = \frac{-1}{2\pi fR_1C_1}$ $\quad f_{p1} = \frac{1}{2\pi R_1C_1}$
Integrator A_2 Gain/Pole Location	$A_2 = \frac{V_2}{V_1} = -\frac{1}{sR_2C_2} = \frac{-1}{2\pi fR_2C_2}$ $\quad f_{p2} = \frac{1}{2\pi R_2C_2}$
Differentiator A_3 Gain	$A_3 = \frac{R_4(sR_5C_3 + 1)}{(R_3 + R_5)(sR_3C_3 + 1)(sR_4C_4 + 1)}$ DC Gain $= \frac{-R_4}{R_3 + R_5}$ $\quad$ Gain at Oscillation $= \frac{-C_3}{C_4}$
Pole/Zero Locations	$f_{p1} = \frac{1}{2\pi R_4C_4}$ $\quad f_{p2} = \frac{1}{2\pi R_3C_3}$ $\quad f_{z1} = \frac{1}{2\pi R_5C_3}$
RC Sensitivities	$s_{R_1}^{\omega_o} = s_{R_2}^{\omega_o} = s_{C_1}^{\omega_o} = s_{C_2}^{\omega_o} = -s_{C_3}^{\omega_o} = s_{C_4}^{\omega_o} = \frac{-1}{2}$

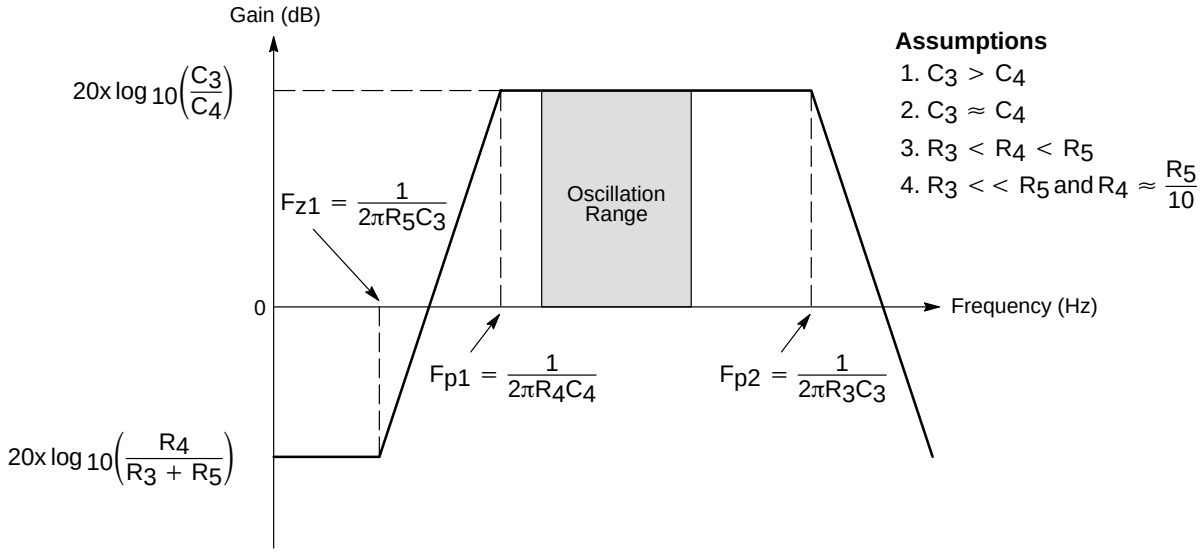


Figure 12. Bode Plot of Differentiator Amplifier A_3

Ratio Oscillator

Step 4: Verify LG ≥ 1

Step 4 will be demonstrating using the single power supply limit circuit shown in Figure 26.

The design equations are listed below.

Assume:

1.) $V_2 = V_{Max\_Limit}$ (i.e.$|A_2| = V_{Max\_Limit}$)

2.) $|A_3| = \frac{C_3}{C_4}$

Check:

1.) Is $|LG| = A_1 \times A_2 \times A_3 \geq V_{Max\_Limit}$

$$= \left(\frac{1}{2\pi f R_1 C_1}\right)(V_{Max\_Limit})\left(\frac{C_3}{C_4}\right) \geq V_{Max\_Limit}$$

2.) Using the values shown in Figure 26,

$$\left(\frac{1}{2\pi(16.5\ kHz)(39\ K\ \Omega)\ (240\ pF)}\right)(V_{Max\_Limit})\left(\frac{C_3}{C_4}\right) \geq V_{Max\_Limit}$$

$$(1.03)\ (V_{Max\_Limit})\left(\frac{C_3}{C_4}\right) \geq V_{Max\_Limit}$$

3.) Oscillation will be sustained if

$$\frac{C_3}{C_4} \geq \left(\frac{1}{1.03}\right)$$

COMPONENT SELECTION

Operation Amplifiers

The selection of an appropriate operational amplifier in a precision oscillator application is based on analyzing the errors caused by the amplifiers. Operational amplifier errors include input offset voltage (V_{IO}) and input bias current (I_B), open loop gain (A_o), and a finite bandwidth and slew rate (SR). The error contribution of the operational amplifier can be minimized if a low bias current, wide bandwidth amplifier is chosen. Also, selecting a low oscillation frequency minimizes the DC gain and bandwidth errors. In sensor applications, only the frequency of the signal is monitored; therefore, the DC amplifier errors of V_{OS}, I_B, and a finite gain will result in output signal distortion, but will not have a significant effect on the oscillation frequency. The open loop gain of almost all amplifiers will be several orders of magnitude larger than the closed loop gain of an oscillator, which typically is 1 to 2 at each amplifier. The AC amplifier errors resulting from a finite slew rate and bandwidth has a minimal effect if the oscillation frequency is relatively low (i.e. 10 kHz to 20 kHz).

Integrators

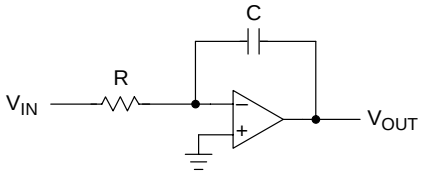


Figure 13. Ideal Integrator Amplifier

Listed below are the equations for the ideal integrator circuit formed by a single resistor and a capacitor as shown in Figure 13.

$$V_{OUT}(t) = -\frac{1}{RC}\int V_{IN}(t)dt$$

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = -\frac{1}{sRC}$$

The ideal integrator equations do not consider the effect of the amplifiers voltage offset and current bias offset errors. The effect of the offset errors is shown below [3][11].

$$V_{OUT}(t) = -\frac{1}{RC}\int V_{IN}(t)dt \pm \frac{1}{RC}\int V_{IO}dt + \frac{1}{C}\int I_B dt \pm V_{IO}$$

$$= \text{ideal} \pm \text{offset error} \pm \text{bias error}$$

Where V_{IO} and I_B are defined as:

$$V_{IO} = V_{IO} + \frac{\Delta V_{IO}}{\Delta T}\Delta T_{(Temp)} + \frac{\Delta V_{IO}}{\Delta V_S}\Delta V_{S(PowerSupply)} + \frac{\Delta V_{IO}}{\Delta t}\Delta t_{(Time)}$$

$$I_B = I_B + \frac{\Delta I_B}{\Delta T}\Delta T_{(Temp)} + \frac{\Delta I_B}{\Delta V_S}\Delta V_{S(PowerSupply)} + \frac{\Delta I_B}{\Delta t}\Delta t_{(Time)}$$

If the integrator offset and bias errors are referenced to the output, as shown below,

$$\frac{dV_{OUT}(t)}{dt} = \frac{V_{IO}}{RC} + \frac{I_B}{C}$$

the following observations can be made:

1. Use small R, large C.
2. $V_{OS} \propto 1 / RC$ and $I_B \propto 1 / C$.
3. Use a low leakage current capacitor.
4. I_B can be reduced if a resistor equal to the parallel combination of R and C is connected to the non–inverting input of the amplifier.

The error due to the operational amplifier's finite open loop gain and bandwidth, as shown below:

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \left[-\frac{1}{sRC}\right]\left[\frac{1}{1 + \left(\frac{1+T_{os}}{A_o}\right)\left(1 + \frac{1}{sR_pC}\right)}\right]$$

$$= \text{ideal} \times (\text{gain} + \text{bandwidth error})$$

where:

$$R_p = \frac{R_d R}{R_d + R}$$

$R_d \equiv$ open loop impedance
$T_o \equiv -3$ dB frequency
$\omega_1 \equiv$ the unity gain bandwidth $\approx A_o / T_o$

If $A_o >> 1$, the transfer equation can be simplified to:

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \left[-\frac{1}{sRC}\right]\left[\frac{1}{1 + \frac{1}{A_o} + \frac{T_o s}{A_o} + \frac{1}{A_o R_p C s} + \frac{T_o}{A_o R_p C}}\right]$$

$$\cong \left[-\frac{1}{sRC}\right]\left[\frac{1}{1 + \frac{s}{\omega_1} + \frac{1}{A_o R_p C s}}\right]$$

Also, there will be an error due to the amplifier slew rate and output current limitation. The slew rate error is defined as:

$$\frac{dV_{OUT}(t)}{dt}\Big|_{max} = 2\pi f_p E_o = SR$$

where: $f_P \equiv$ full power response
$E_o \equiv$ rated output voltage

The output current (I_o) of the amplifier charges the integrator feedback capacitor; thus, the integrator may have a slew rate that is less than the specified amplifier SR. The maximum rate of change of output voltage is equal to I_o/C.

Differentiator

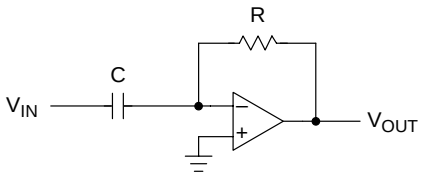


Figure 14. Ideal Differentiator

Listed below are the equations for the ideal differentiator circuit shown in Figure 14.

$$V_{OUT}(t) = -RC\frac{dV_{IN}(t)}{dt}$$

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = -sRC$$

However, the ideal differentiator does not consider the effect of the amplifier's voltage offset and current bias errors, as shown below [3].

$$V_{OUT}(t) = -RC\frac{V_{IN}(t)}{dt} \pm V_{IO} \pm I_B R$$

If the output offset and bias errors are referenced to the input, as shown below,

$$\frac{dV_{IN}(t)}{dt}_{error} = \pm\frac{V_{IO}}{RC} \pm \frac{I_B}{C}$$

the following observations can be made:

1. Use small R, large C.
2. $V_{IO} \propto 1 / RC$ and $I_B \propto 1 / C$.

A practical differentiator circuit is shown in Figure 15. For simplicity, this circuit will neglect the effect of resistor R_5. There will be an error due to the operational amplifier's finite open loop gain as shown below:

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{s\frac{A_0}{1-A_0}\frac{1}{R_3C_4}}{s^2 + s\left[\frac{1}{R_4C_4} + \frac{1}{R_3C_3}\right] + \frac{1}{R_3R_4C_3C_4}}$$

If $A_o >> 1$, the transfer equation can be simplified to:

$$\frac{V_{OUT}(s)}{V_{IN}(s)} \cong \frac{-s\left(\frac{1}{R_3C_4}\right)}{\left(s + \frac{1}{R_3C_3}\right)\left(s + \frac{1}{R_4C_4}\right)} \cong \frac{-sR_4C_3}{(sR_3C_3 + 1)(sR_4C_4 + 1)}$$

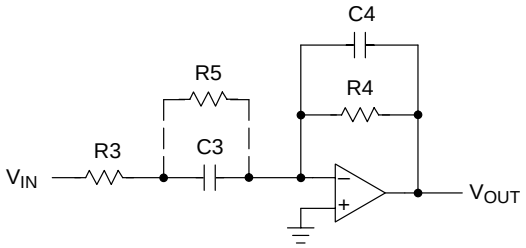


Figure 15. Practical Differentiator (Neglect R5)

The error due to the operational amplifier's finite open loop gain and bandwidth is shown graphically in Figure 16. The oscillator's amplifier error and bandwidth error terms are reduced if a higher gain and increased operational amplifier is selected. The oscillation error can be minimized by selecting an oscillation frequency that is as low as practical (i.e. $f_{oscillation} \cong 10$ KHz).

The Slew Rate (SR) error of a differentiator is identical to the equation listed for an integrator.

$$\frac{dV_{OUT}(t)}{dt}|_{max} = 2\pi f_p E_o = SR$$

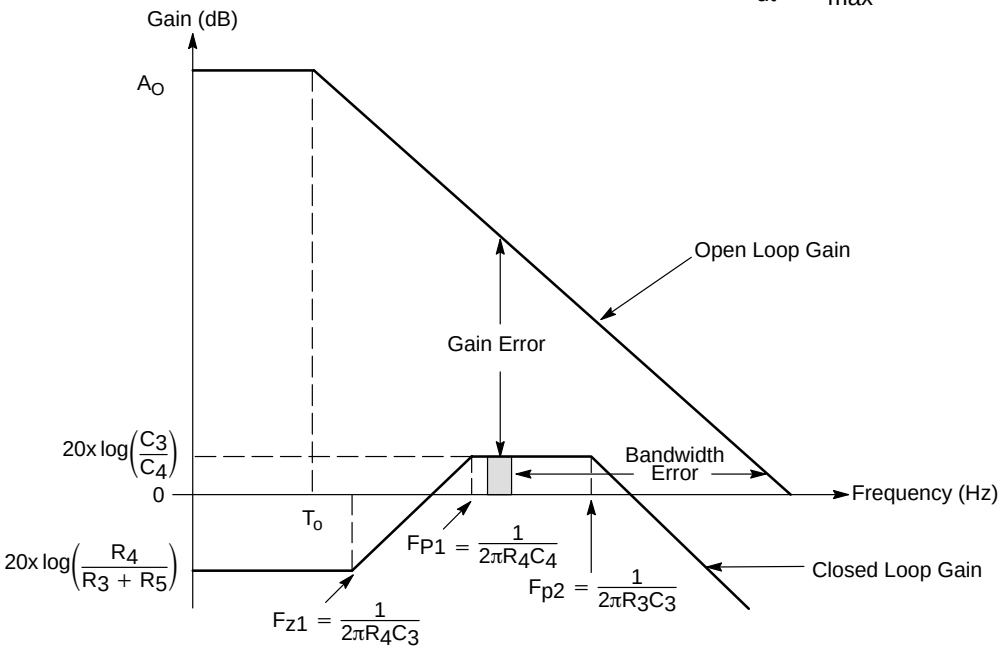


Figure 16. Graphical Error Analysis of Ideal Differentiator

Voltage Limit Circuits

Automatic Gain Control (AGC) circuits and voltage limit or bounding circuits are used in oscillators to prevent the operational amplifiers from saturating and to avoid amplifier slew rate limitations. Bipolar transistors are inherently slow in coming out of saturation; therefore, a limit circuit should be used to prevent a frequency error when using amplifiers such as the BiCMOS MC33501 or MC33503. FET transistors do not have the slow recovery time problem coming out of saturation; however, a limit circuit should also be used with CMOS operational amplifiers. The gain of the transistors in a CMOS operational amplifier such as the NCS2001 will change when the transistors saturate; thus, a limit circuit is necessary to prevent an oscillation error.

Limit circuits will also decrease the required time for the oscillation signal to stabilize at start–up. When an oscillator's poles are located exactly on the imaginary axis, the resulting waveform will be a perfect sinusoidal signal. To ensure oscillation startup the poles are adjusted to lie slightly in the right half s–plane causing the signal to grow exponentially until it is limited by some type of non–linearity, such as the saturation voltage of the amplifier.

AGC Circuits

Automatic Gain Control (AGC) circuits provide a linear control of the amplifier gain to produce a constant output voltage regardless of the level of the input signal. AGC circuits are usually used in applications where the level of signal distortion needs to be minimized. AGC circuits are more complex than limit circuits and usually consist of an operational amplifier and/or FET that are used as a variable resistor. An example of an AGC circuit is shown in Figure 17.

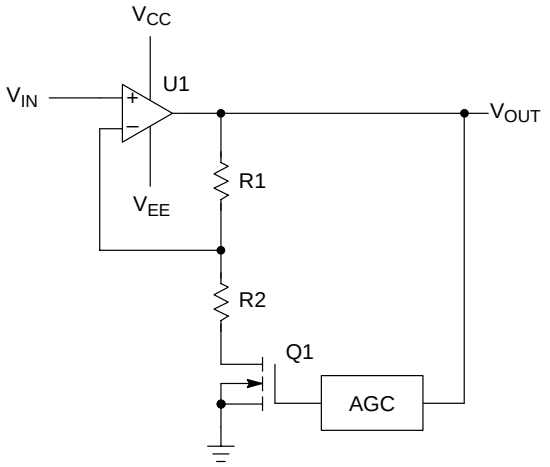


Figure 17. FET AGC Circuit

Limit Circuits

Limit circuits are nonlinear circuits, which clamp the amplitude to a voltage level that is less than the amplifier power supply voltage. This clamping function will produce distortion in the oscillator signal. The selection of the voltage limit circuits is based on the allowable signal distortion and the simplicity of the circuit. The distortion level for most sensor oscillator circuits is relatively unimportant because only the frequency of the signal is monitored. Also, limit circuits are preferable to AGC circuits because they require fewer components. Limit circuits typically consist of a combination of zener diodes, diodes, and transistors.

Dual Power Supply Limit Circuits

Figure 18 shows the clamping function of the limit circuit for a dual power supply application. A simple dual supply voltage limit circuit can be created by using two back–to–back zeners as shown in Figure 19. There are several performance limitations with this circuit that result from the relative large junction capacitance, leakage current and temperature coefficient of a zener diode. These limitations result in a distortion of the output signal and an error in the oscillation frequency. In addition, this circuit's low voltage operation is limited to the value of the zener diode's clamping voltage (V_{Zener}) plus the forward voltage drop (V_f) of the second zener diode. Zener diodes are available in voltages of about 1.8 volts, while their forward voltage drop is typically 0.7; therefore, this circuit is not useful for voltage limiting applications below 2.5 volts.

The minimum voltage range of the back–to–back zener diode limit circuit can be reduced by adding two resistors to the limit circuit as shown in Figure 20 [4]. The clamping value of this circuit is a function of the zener diode breakdown voltage multiplied by the ratio of the resistors. This circuit is solves the low voltage limitation of the back–to–back zener limit circuit; however, this circuit is not suitable for the integrator amplifiers of the oscillator when resistor R2 is replaced by a capacitor.

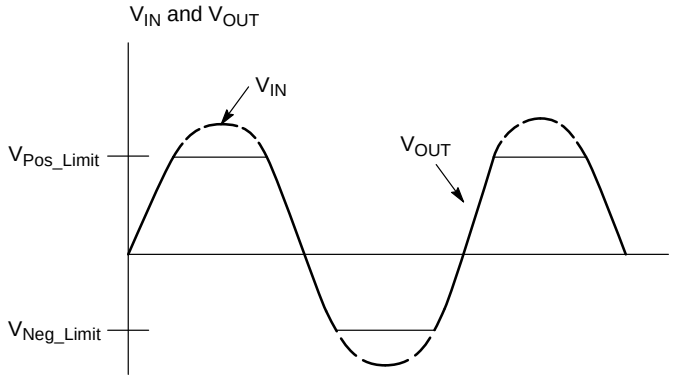
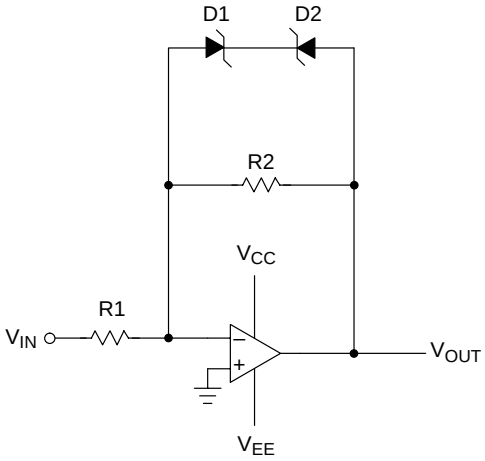
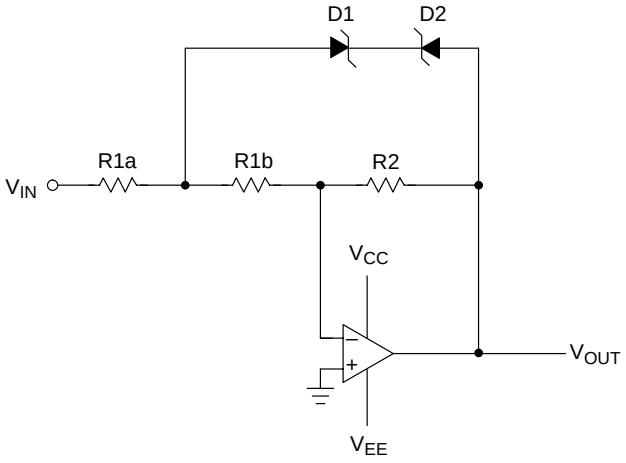


Figure 18. Dual Power Supply Clamping



$$V_{Limit} = \pm\ (V_{Zener} + V_f)$$

Figure 19. Back–to–Back Zener Diode Limit Circuit

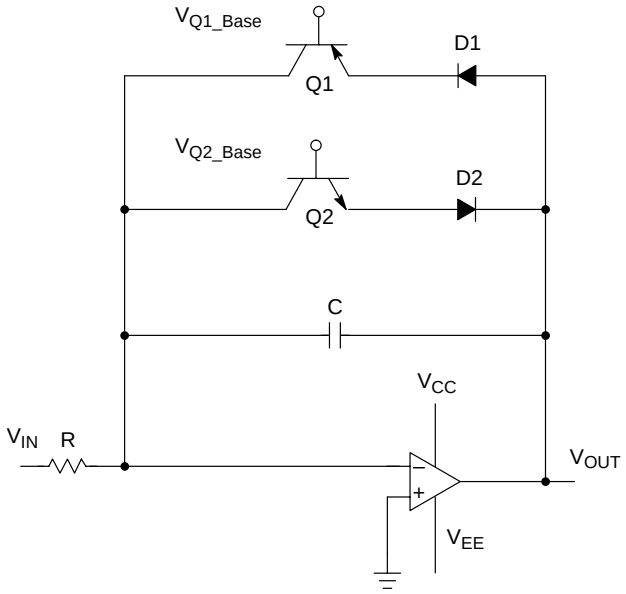


$$V_{Limit} \cong \pm\ (V_{Zener} + V_f) * \frac{R_2}{R_{1b} + R_2}$$

Figure 20. Back–to–Back Zener Diode Limit Circuit with Voltage Ratio Resistors

The voltage limit circuit shown in Figure 21 is useful in dual power supply designs when the integrator capacitance is relatively small. A combination of two transistors and two diodes are used to make up the circuit, which limits the signal at positive and negative voltages. The diodes are used to reduce the effective capacitance of the bipolar transistors and they can be removed for low voltage applications.

The operation of the limit circuits formed by the NPN and/or PNP transistors can be understood by using the Ebers–Moll transistor model, where a transistor is modeled as a base–to–emitter and a base–to–collector diode. The circuit functions by setting the fixed voltage at the base–to–collector junction to be less than the diode's turn–on voltage; therefore, this diode is always "OFF''. Next, the emitter of the transistor is connected to the sine wave output of the amplifier; thus, the base–to–emitter voltage (V_{BE}) can be either greater than or less than a diode's turn–on voltage. When the V_{BE} voltage is above the diode's turn–on voltage, the diode is "ON'' and the transistor is in the forward–active mode of operation and the circuit clamps at a level set by the base voltage. However, when the V_{BE} voltage is below the diode turn–on voltage, the junction is "OFF'' and the transistor is in the cut–off mode of operation and the clamping network is effectively an open circuit.



$V_{Q1\_Base} > 0$ V $\qquad$ $V_{Q2\_Base} < 0$ V

$$V_{Pos\_Limit} = V_{Q1\_base} + V_{Q1\_base–to–emitter} + V_f$$
$$\cong V_{Q1\_base} + (2 * 0.7) \cong V_{Q1\_base} + 1.4\ V$$
$$V_{Neg\_Limit} = V_{Q2\_base} - V_{Q2\_base–to–emitter} - V_f$$
$$\cong V_{Q2\_base} - (2 * 0.7) \cong V_{Q2\_base} - 1.4\ V$$

Figure 21. Dual Power Supply Limit Circuit

Single Power Supply Circuits

Figure 22 shows the clamping function of the limit circuit for a single power supply application [3] [4]. The limit circuit for low voltage single supply circuits can be formed by a single NPN or PNP transistor. The PNP circuit shown in Figure 23 is used to create the maximum voltage limit, while the NPN circuit shown in Figure 24 is used to form the minimum voltage limit. Note that in single supply applications it is not necessary to use both the PNP and NPN limit circuits. Only one of the limit circuits is required to prevent the amplifiers from saturating in the state variable oscillator.

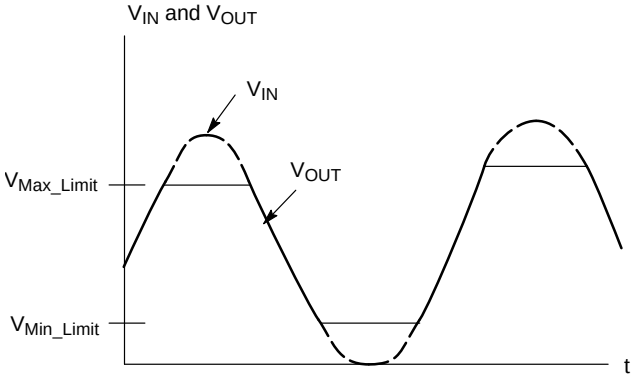
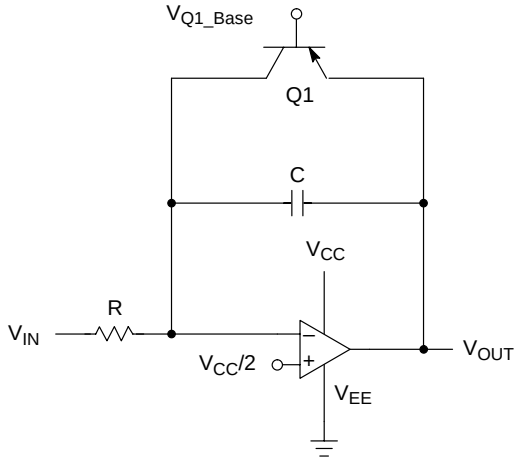
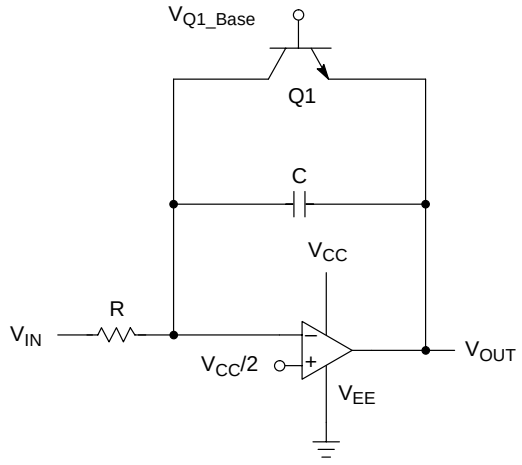


Figure 22. Single Power Supply Clamping



$$V_{Max\_Limit} = V_{Q1\_base} + V_{Q1\_base–to–emitter}$$
$$\cong V_{Q1\_base} + 0.7\ V$$

Figure 23. Single Supply Maximum Limit Circuit



$$V_{Min\_Limit} = V_{Q1\_base} - V_{Q1\_base–to–emitter}$$
$$\cong V_{Q1\_base} - 0.7\ V$$

Figure 24. Single Supply Minimum Limit Circuit

Resistors and Capacitors

It is critical that the oscillator circuits use precision resistors and capacitors with a small temperature coefficient (TC) and low drift rate to minimize temperature and aging errors. Long term stability is typically specified for resistors and capacitors by a life test of 2000 hours at the maximum rated power and ambient temperature. In general these components have an exponential change in value for the first 500 hours of the test and are essentially stable for the remainder of the test. Thus, a burn–in, or temperature cycling procedure will significantly lower the drift error of the resistors and capacitors.

Three types of precision resistors are available: metal film, wirewound, and foil. Metal film and wirewound resistors are available with a TC of ±10 to ±25 ppm/°C and a drift specification of approximately 0.1 to 0.5%. Foil resistors are available with a TC of ±0.3 ppm/°C and a drift specification of less than 20 ppm. Errors with resistors are caused by both environmental and manufacturing factors. The major environmental factors causing changes in resistance are the operating power and the ambient temperature. Other environmental factors such as humidity, the voltage coefficient (ΔR vs. voltage), the thermal EMF (due to the temperature difference between the leads and self heating), and storage will cause relatively small errors. Manufacturing induced errors from factors such as soldering can cause a small change in resistance; however, this error will not effect the component's long term stability.

Two of the leading technologies of stable capacitors are RF/Microwave multilayer porcelain and NPO (COG) ceramic capacitors. The TC of porcelain capacitors is specified at +90 ± 20 ppm/°C, while NPO ceramic capacitors are available with a TC of 0 ± 30 ppm/°C. The TC is specified over a temperature range of –55 to 125°C; however, the specification is skewed by the relatively large changes in capacitance at the extreme hot and cold temperatures. Both types of capacitors have a drift specification of 200 ppm or ± 0.02 pF, whichever is greater, for a 2000 hour life test at 200% WVDC and a temperature of 125°C. The major error term of capacitors is due to temperature hysteresis and is specified as the retrace error. Precision sensors use temperature compensation, thus a change of capacitance with temperature can be corrected; however, it is difficult to correct for hysteresis errors. Other error sources are a result of the piezoelectric effect (ΔC vs. voltage and pressure), the quality factor (Q), and the terminal resistance. These errors are relatively small because the capacitors are designed for microwave frequencies and are specified at a WVDC well beyond the normal operating voltage of an op–amp circuit.

APPLICATION ISSUES

Remote Sensing

Often, it is necessary to remotely locate the detection circuit from the sensor, and connect the sensor to the circuit with a shielded cable. For example, an oil level sensor for a gas turbine engine must operate at a temperature of 400°F, which is well beyond the operating capability of standard electronic components. In addition, a shielded cable is often required to limit the noise sensitivity of the measurement. The capacitance of shielded wire is typically 30 to 50 pF per foot, while the sensor capacitance is usually less than 100 pF. Thus, the electronic circuit must be insensitive to the cable capacitance which will be much larger than the sensor capacitance.

One approach to minimize the cable capacitance error is to use a shielded cable and the virtual ground feature of an operational amplifier when the non–inverting input is grounded. This feature is inherent in the integrator and inverter/differentiator circuits used in the state variable oscillator. Because an operational amplifier has a high open loop gain and input impedance, the differential voltage between the inverting and non–inverting inputs is essentially zero. Thus, the voltage potential at the inverting input is equal to the ground potential at the non–inverting terminal. The virtual ground approach forces a constant voltage to appear across the cable capacitance; therefore, the cable capacitance does not have to be charged or discharged by the circuit and the oscillation frequency is not effected. A constant DC level at the non–inverting input in the single power supply configuration is equivalent to a virtual ground because the AC level of the input terminals is equal to zero volts. The remote sensing ability of the state variable oscillator will be analyzed in detail in a future application note.

Reference Design

The reference design for the absolute oscillator is shown in Figure 25. The circuit uses the BiCMOS MC33501 operational amplifiers operated at a power supply of ± 2.5V. In addition the circuit uses the dual supply limit circuit. The operating voltage of the circuit could be lowered by removing diodes D_1 and D_2, and adjusting the base voltages of transistors Q_1 (V_{Pos_Limit}) and Q_2 (V_{Neg_Limit}). In the

typical application, capacitors C_1 and C_2 would be the sensor capacitances.

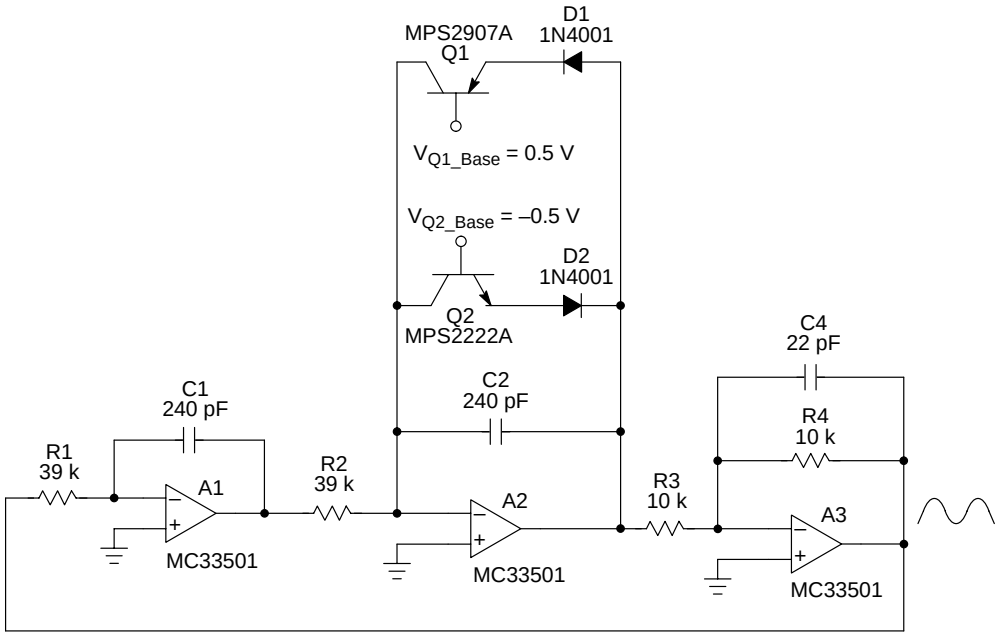
The reference design for the ratio circuit is shown in Figure 26. This circuit uses the CMOS NCS2001 operational amplifiers operated at the single power supply of 0.9V. In addition the circuit uses the single supply limit circuit. In the typical application, Capacitor C_3 functions as the C_{MEAS} sensor while C_4 serves as the C_{REF} sensor.

The single supply Vcc/2 reference voltage was obtained by using a resistor divider network. The values of the resistors R_9 and R_{10} were obtained by finding the input impedances of the integrator circuits formed at amplifiers A_1 ($R_1 \parallel C_1$) and A_2 ($R_2 \parallel C_2$). The input bias current of the CMOS amplifier is specified at only 10 pA; therefore, it is not necessary to balance the impedances at the non–inverting and inverting terminals of the amplifiers. In most applications, the non–inverting terminal can be connected directly to the reference voltage. Figure 27 shows a voltage follower circuit that could be used to provide a more stable reference voltage with the additional benefit of a low output impedance.

The NCS2200 comparator is used by the ratio oscillator design to convert the oscillator's sine wave output to a square ware digital signal. The NCS2200 is available in both a complementary and an open drain output configuration. The reference design used the open drain configuration to form a zero crossing detector.

Table 2 lists the calculated and measured oscillation frequency for the reference designs. The calculated frequency was obtained by measuring the R's and C's and using these values with the oscillation equations.

The measured frequency of the absolute and ratio oscillators was approximately ±1% different than the calculated frequency. This error between the measure and predicated oscillation frequency is probably due to the capacitance of the limit circuits, which is not included in the frequency equations. The reference designs used standard NPN, PNP transistors and diodes; selecting high frequency or RF devices would minimize the oscillation error of the limiting circuit.



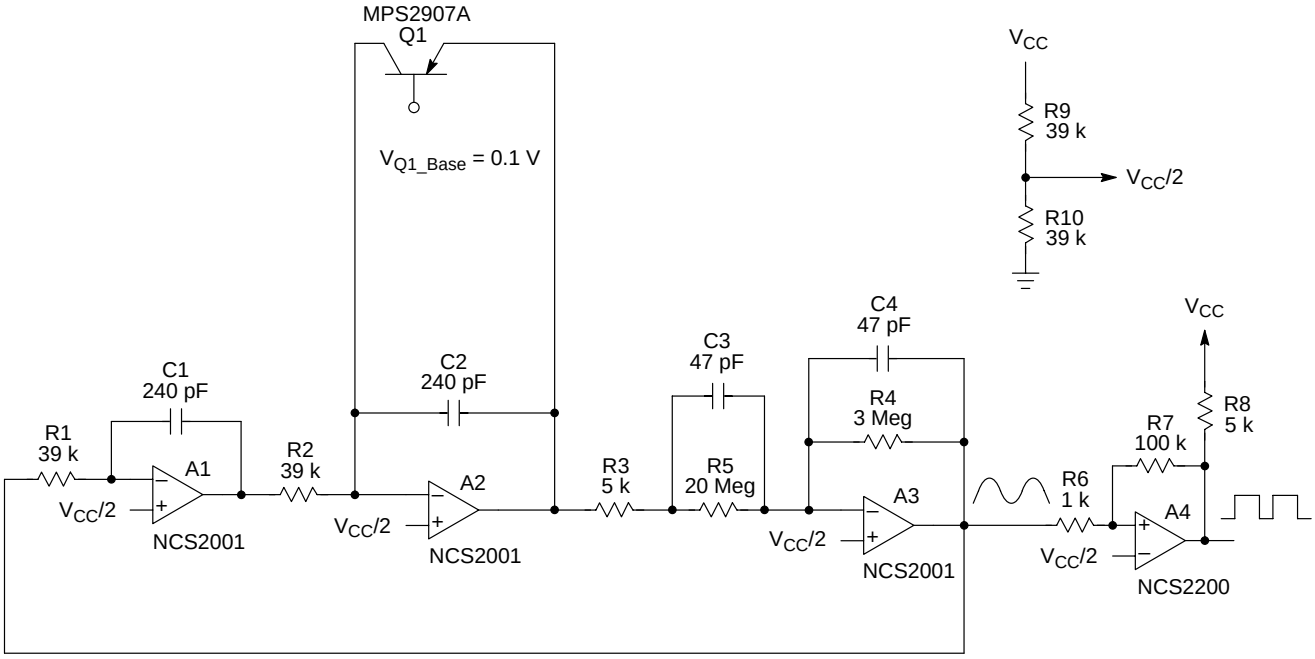
NOTES:

1. Power Supply Voltages for amplifiers A1, A2, and A3 are V_{CC} = 2.5 V, V_{EE} = 2.5 V
2. V_{Pos_Limit} = 1.9 V and V_{Neg_Limit} = –1.9 V

Figure 25. Reference Design – Absolute Circuit

Table 2. Reference Designs Oscillation Frequency

Circuit	Calculated Oscillation Frequency	Measured Oscillation Frequency
Absolute Oscillator	16.6 kHz	16.4 kHz
Ratio Oscillator	16.5 kHz	16.3 kHz



NOTES:

1. Power Supply Voltages for amplifiers A1, A2, A3, and A4 is V_{CC} = 0.9 V, V_{EE} = 0 V
2. Capacitors C3 and C4 are typically the sensor capacitance; however, for test purposes two 47 pF capacitors were used to verify the circuit.
3. V_{Max_Limit} = 0.8 V

Figure 26. Reference Design – Ratio Circuit

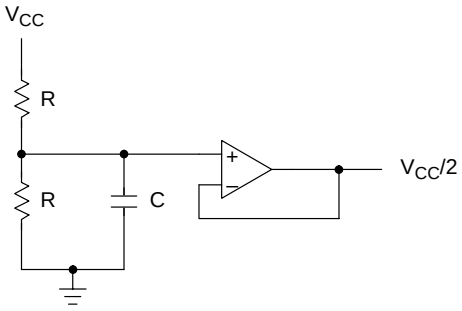


Figure 27. Low Output Impedance Reference Voltage

Appendix I: Mason's Reduction Theorem

The oscillation frequency is determined by finding the poles of the denominator of the transfer equation T(s) or equivalently the zeroes of the numerator N(s) of the characteristic equation Δ(s). Mason's theorem (12.) states that the transfer function from input X to output Y is

$$T(s) = \frac{Y}{X} = \frac{\sum_i P_i \Delta s_i}{\Delta s}$$

where the terms are defined as:

P_i is the direct transmittance or path form input X to output Y

Δs_i is the system determinant.

$\Delta s_i = 1$ if P_i touches all of the loops

$$\Delta s = 1 - \Sigma L_j + \Sigma' L_k L_l - \Sigma' L_m L_n L_n + \ldots$$

ΣL_j is the sum of all loops (i.e. loop gains)

$\Sigma L_k L_l$ is the sum of products of pairs of non–touching loops

$\Sigma L_m L_n L_o$ is the sum of products of gains of non–touching loops taken three at a time

Mason's Reduction Theorem should be used to determine the transfer equation if the oscillator has more than one feedback loop, such as the case for the circuit shown in Figure 28. Obtaining T(s) also provides the additional information required to complete a Bode plot of the oscillator. In contrast, Step 1 of the design procedure only provides the denominator of T(s) and will not provide the numerator of the transfer equation. Mason's equation can be rewritten in the form listed below:

$$T(s) = \frac{A}{1 - LG} = \frac{A}{\Delta(s)} = \frac{A}{\left(\frac{N(s)}{D(s)}\right)}$$

The absolute and ratio oscillators only have a single feedback loop, therefore, the calculation of

$$T(s) = \frac{V_3}{V_{11}}$$

is relatively easy because the path P_1 (equivalent to the amplifier gain A) is defined as the voltage gain from node V_{11} to V_3 and will be equal to the loop gain LG_1. In order to calculate the transfer equation, the intermediate voltage node of V_{11} is created by adding a "small" resistor R_{11} in series with resistor R_1 to the absolute and ratio circuits as shown in Figures 29 and 30. Adding R_{11} and V_{11} is not mathematically necessary; however, it greatly simplifies the algebra in the transfer equations. Note, the numerator of the transfer equation depends on the definition of the input and outputs; however, the denominator (i.e. the oscillation equation) is independent of the definition of T(s). If $R_1 >> R_{11}$, then the gain of amplifier A_1 is a function only of R_1 and C_1.

$$A_1 = \left(-\frac{1}{s(R_1 + R_{11})C_1}\right) \cong -\frac{1}{sR_1C_1}$$

Listed below are the calculation of T(s) for the absolute oscillator with and without capacitor C_4 and the ratio oscillator.

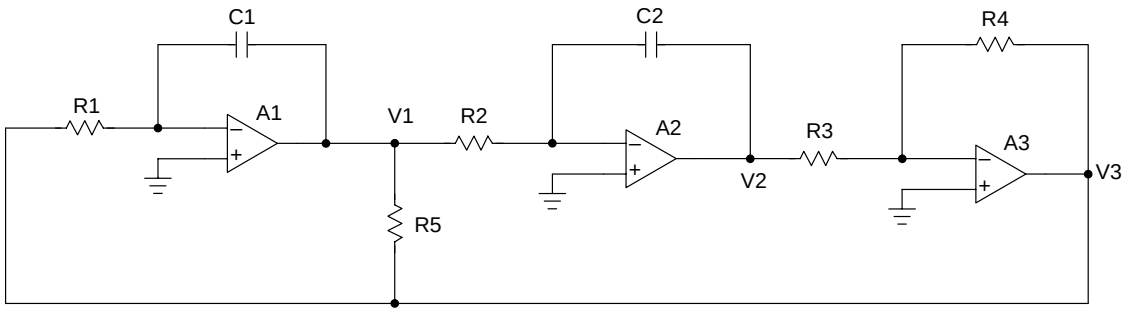


Figure 28. Mason's Theorem Provides a Method to Determine the Transfer Equation T(s) of an Oscillator when there are Multiple Feedback Loops, as with the Modified Absolute Circuit

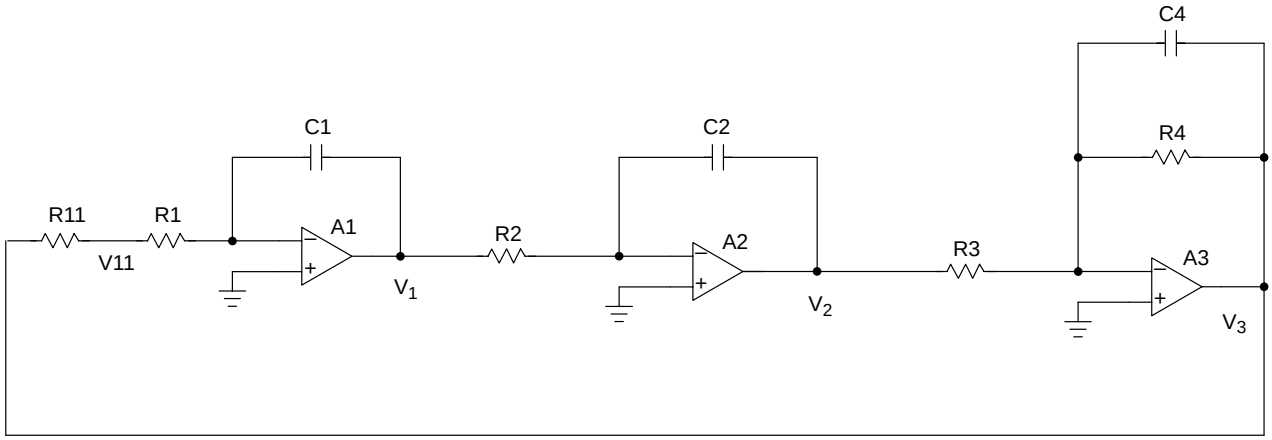


Figure 29. Schematic of the Absolute Oscillator with Rll that is Used to Obtain T(s), using Mason's Reduction Theorem

Absolute Oscillator (without C_4)

Assume $R_1 >> R_{11}$, then $R_1 + R_{11} \cong R_1$

$$P_1 = LG_1 = A_1 \times A_2 \times A_3 = \left(-\frac{1}{sR_1C_1}\right)\left(-\frac{1}{sR_2C_2}\right)\left(-\frac{R_4}{R_3}\right)$$

$$\Delta s = 1 - LG_1 = 1 - \left(-\frac{1}{sR_1C_1}\right)\left(-\frac{1}{sR_2C_2}\right)\left(-\frac{R_4}{R_3}\right) = 1 + \frac{R_4}{s^2R_1R_2R_3C_1C_2} = \frac{s^2R_1R_2R_3C_1C_2 + R_4}{s^2R_1R_2R_3C_1C_2}$$

$$T(s) = \frac{V_3}{V_{11}} = \frac{P_1}{\Delta s} = \frac{\left(\frac{R_4}{s^2R_1R_2R_3C_1C_2}\right)}{\left(\frac{s^2R_1R_2R_3C_1C_2 + R_4}{s^2R_1R_2R_3C_1C_2}\right)} = \frac{-R_4}{s^2R_1R_2R_3C_1C_2 + R_4}$$

Absolute Oscillator (with C_4)

Assume $R_1 >> R_{11}$, then $R_1 + R_{11} \cong R_1$

$$P_1 = LG = A_1 \times A_2 \times A_3$$

$$P_1 = LG = \left(-\frac{1}{sR_1C_1}\right)\left(-\frac{1}{sR_2C_2}\right)\left[\left(-\frac{R_4}{R_3}\right)\left(\frac{1}{sR_4C_4 + 1}\right)\right] = -\frac{-R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2}$$

$$\Delta s = 1 - LG = 1 + \frac{R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2} = \frac{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2 + R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2}$$

$$T(s) = \frac{P_1}{\Delta s} = \frac{\left(\frac{-R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2}\right)}{\left(\frac{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2 + R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2}\right)} = \frac{-R_4}{s^3R_1R_2R_3R_4C_1C_2C_4 + s^2R_1R_2R_3C_1C_2 + R_4}$$

Ratio Oscillator

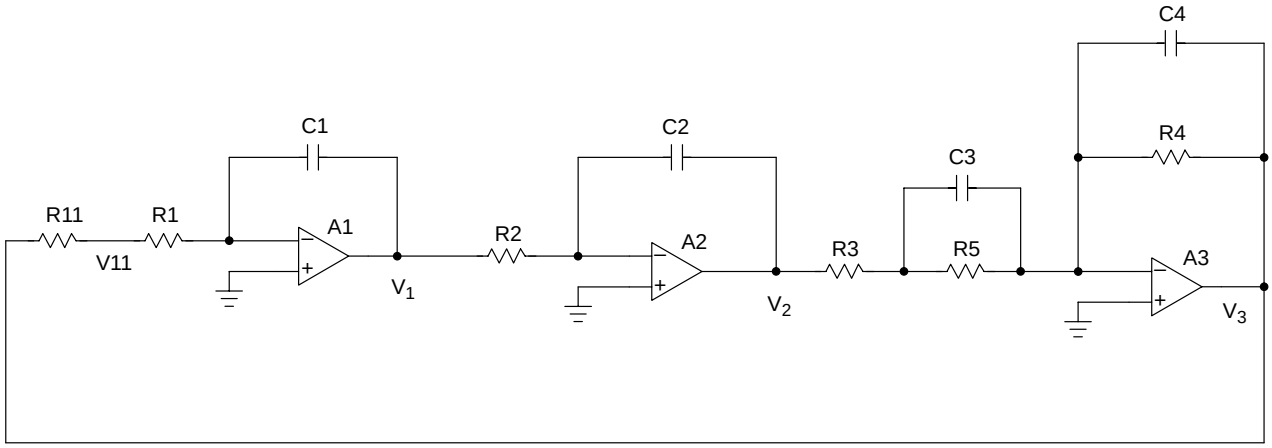


Figure 30. Schematic of the Ratio Oscillator with Rll that is Used to Obtain T(s), using Mason's Reduction Theorem.

Ratio Circuit

Assume $R_1 >> R_{11}$, then $R_1 + R_{11} \cong R_1$

$$P_1 = LG = A_1 \times A_2 \times A_3 = \left(-\frac{1}{sR_1C_1}\right)\left(-\frac{1}{sR_2C_2}\right)\left(-\frac{R_4(sR_5C_3 + 1)}{(sR_3R_5C_3 + R_3 + R_5)(sR_4C_4 + 1)}\right)$$

$$P_1 = LG_1 = \frac{-(sR_4R_5C_3 + R_4)}{s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] + s^2(R_3 + R_5)(R_1R_2C_1C_2)}$$

$$\Delta s = 1 - LG_1 = \frac{s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] + s^2(R_3 + R_5)(R_1R_2C_1C_2) + sR_4R_5C_3 + R_4}{s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] + s^2(R_3 + R_5)(R_1R_2C_1C_2)}$$

$$T(s) = \frac{V_3}{V_{11}} = \frac{P_1}{\Delta s} = \frac{\left(\frac{-(sR_4R_5C_3+R_4)}{s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4+s^3[(R_3R_5C_3+R_3R_4C_4+R_4R_5C_4)R_1R_2C_1C_2]+s^2(R_3+R_5)(R_1R_2C_1C_2)}\right)}{\left(\frac{s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4+s^3[(R_3R_5C_3+R_3R_4C_4+R_4R_5C_4)R_1R_2C_1C_2]+s^2(R_3+R_5)(R_1R_2C_1C_2)+sR_4R_5C_3+R_4}{s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4+s^3[(R_3R_5C_3+R_3R_4C_4+R_4R_5C_4)R_1R_2C_1C_2]+s^2(R_3+R_5)(R_1R_2C_1C_2)}\right)}$$

$$= \frac{-(sR_4R_5C_3 + R_4)}{s^4R_1R_2R_3R_4R_5C_1C_2C_3C_4 + s^3[(R_3R_5C_3 + R_3R_4C_4 + R_4R_5C_4)R_1R_2C_1C_2] + s^2(R_3 + R_5)(R_1R_2C_1C_2) + sR_4R_5C_3 + R_4}$$

Appendix II: Method II:
Solve $N(j\omega_o)_{REAL} = N(j\omega_o)_{IMAGINARY} = 0$

The oscillation equation sometimes can be determined directly from the characteristic equation by substituting $s = j\omega_o$ into Δs and arranging the $N(j\omega_o)$ into its real and imaginary parts. However, this method is usually not feasible for circuits which are fifth order and higher oscillators. This procedure is essentially a subset of the Routh test, because the first two rows of the Routh array will correspond to $N(j\omega_o)_{REAL}$ and $N(j\omega_o)_{IMAGINARY}$. If the characteristic equation $N(s) = j\omega_o = 0$, the poles of the characteristic equation will be on the imaginary axis at $\pm j\omega_o$ with an oscillation frequency of ω_o. The Method II procedure is shown below for second and third order oscillators [13].

Second–Order Circuits

$$N_{2(s)} = a_0s^2 + a_1s + a_2 = a_0\left(s^2 + \frac{a_1}{a_0}s + \frac{a_2}{a_0}\right)$$

Let $s = j\omega_o$ be the frequency at which $N_2(s) = 0$. The condition for oscillation is meet when the a_1 term is set to zero, and the s–term is removed. The frequency of oscillation is found from:

$$\omega_o = \sqrt{\frac{a_2}{a_0}}$$

Third Order Circuits

$$N_3(s) = a_0s^3 + a_1s^2 + a_2s + a_3$$

Let $s = j\omega_o$ be the frequency at which $N_3(s) = 0$, and arrange the equation into its real and imaginary parts:

$$N_3(j\omega_o) = (-a_1\omega_o^2 + a_3) + j\omega_o(-a_0\omega_o^2 + a_2) = 0$$

Thus, the real and imaginary parts equal zero when:

$$-a_1\omega_o^2 + a_3 = 0 \text{ and } -a_0\omega_o^2 + a_2 = 0$$

Solving the above equations for ω_o^2 gives:

$$\omega_o^2 = \frac{a_3}{a_1} = \frac{a_2}{a_0}$$

Summary of Method II Equations

Oscillator Order	N(s)	Oscillation Condition	ω_o
2nd	$N_2(s) = a_0s^2 + a_1s + a_2$	$a_1 = 0$	$\omega_o = \sqrt{\frac{a_2}{a_0}}$
3rd	$N_3(s) = a_0s^3 + a_1s^2 + a_2s + a_3$	$a_1a_2 = a_0a_3$	$\omega_o = \sqrt{\frac{a_3}{a_1}} = \sqrt{\frac{a_2}{a_0}}$

Appendix III: Routh's Stability Test

Routh's Stability Test [12] can be used to test the characteristic equation to determine whether any of roots lie on the imaginary axis. Routh's test consists of forming a coefficient array. Next, the procedure substitutes $s = j\omega_o$ for s, and the summation of the row is set to zero. If the row equation produces a nontrivial solution for ω_o, the procedure is complete and the frequency of oscillation is equal to ω_o. If the row equation does not yield an equation that can be solved for ω_o, the procedure continues with the next row in the Routh array. This technique arranges the numerator of the characteristic equation (i.e. denominator of the transfer equation) into the array listed below.

$$T(s) = \frac{A}{1 - LG} = \frac{A}{\Delta(s)} = \frac{A}{\left(\frac{N(\Delta s)}{D(\Delta s)}\right)}$$

$$N(\Delta s) = a_0 s^n + a_1 s^{n-1} + a_2 s^{n-2} + a_3 s^{n-3} + \ldots + a_{n-1} s + a_n$$

s^n	a_0	a_2	a_4	···	a_n
s^{n-1}	a_1	a_3	a_5	···	a_{n-1}
s^{n-2}	b_1	b_2	b_3	···	b_{n-2}
s^{n-3}	c_1	c_2	c_3	···	c_{n-3}
.	.	.	.		
.	.	.	.		
.	.	.			
s_0	f_1				

where the coefficients b_1, b_2, b_3, etc., are evaluated as follows:

$$b_1 = \frac{a_1 a_2 - a_0 a_3}{a_1} \quad b_2 = \frac{a_1 a_4 - a_0 a_5}{a_1}$$

$$b_3 = \frac{a_1 a_6 - a_0 a_7}{a_1}$$

The evaluation of the b's is continued until the remaining terms are equal to zero. The same pattern of cross multiplying the coefficients of the two previous rows is followed in evaluating the c's, d's, etc...

$$c_1 = \frac{b_1 a_3 - b_2 a_1}{b_1}$$

$$c_2 = \frac{b_1 a_5 - b_3 a_1}{b_1}$$

This process is continued until the *n*–th row has been completed. The Routh stability criterion states:

1. A necessary and sufficient condition for stability is that the first column of the array does not contain sign changes.
2. The number of sign changes in the entries of the first column of the array is equal to the number of roots in the right half s–plane.
3. If the first element in a row is zero, it is replaced by ε, and the sign changes when $\varepsilon \rightarrow 0$ are counted after completing the array.
4. The poles are located in the right half plane or on the imaginary axis if all the elements in a row are zero.

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