1.5GHz Band PLL IC for Mobile Communications

Description

The CXA1356N is a PLL frequency synthesizer IC developed for 0.1 to 1.5GHz mobile communication systems. Featuring low current consumption and small packaging, this IC is appropriate for portable systems such as cellular units, etc.

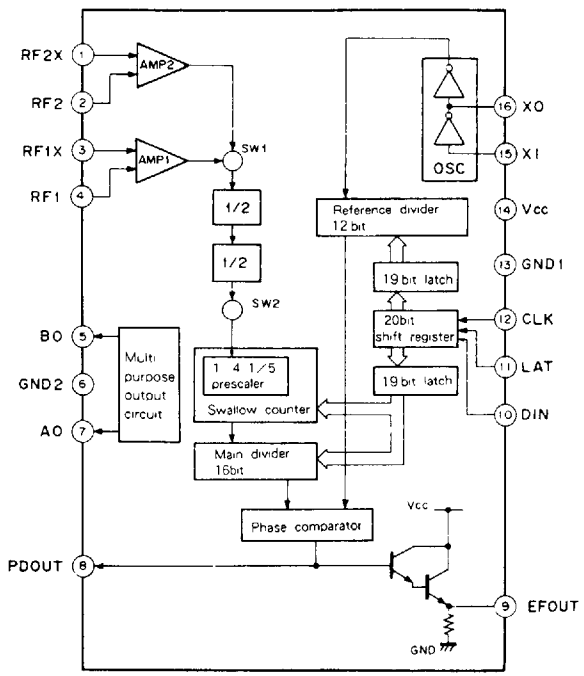
Features

- Low current consumption Icc=14mA (Vcc=5.0V)
- Guaranteed operating frequency 1.62GHz
- High input sensitivity
- Ultra-small 16-pin VSOP package

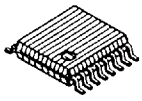
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	300	mW

Block Diagram and Pin Configuration



16 pin VSOP (Plastic)



Structure

Bipolar silicon monolithic IC

Applications

0.1 to 1.5GHz mobile communication equipment for cellular units, etc.

Operating Conditions

• Supply voltage	Vcc	4.5 to 5.5	V
• Operating temperature	Topr	−35 to +85	°C

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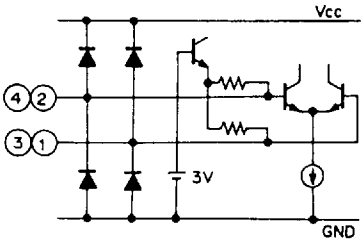
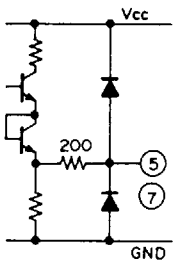
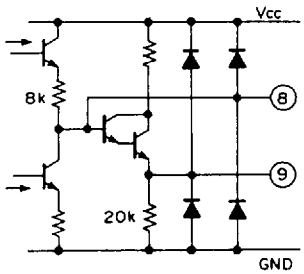
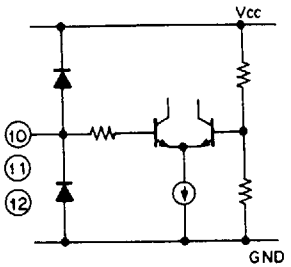
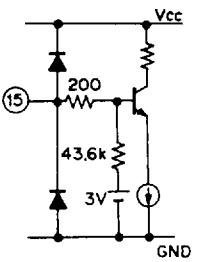
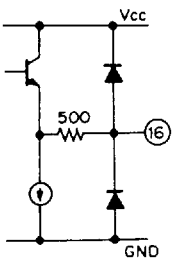
Pin Description

Pin No.	Symbol	Pin voltage Typ. (V)	Equivalent circuit	Description
1	RF2X	2.2		Input for VCO output signals.
2	RF2	2.2		
3	RF1X	2.2		
4	RF1	2.2		
5	AO	(T1=T2=L) H: 3.2 L: 0.5 (For the other data) H: 1.0 L: 0.6		Used for verifying internal operation of IC. Also, output for control systems when T1=T2=Low.
7	BO			
6	GND2	—		GND
8	PDOUT	—		Phase comparator output.
9	EFOUT	—		Used for constructing active filter with built-in transistor.

Pin No.	Symbol	Pin voltage Typ. (V)	Equivalent circuit	Description
10	DIN	—		Serial data input.
11	LAT			Latch signal input.
12	CLK			Clock input.
13	GND1	—		GND
14	Vcc	—		Vcc
15	XI	3.0		Reference divider input. Connect a crystal unit when generating reference signals from internal oscillator.
16	XO	4.1		OPEN when external clock is the reference signal. Connect a crystal unit when generating reference signals from internal oscillator.

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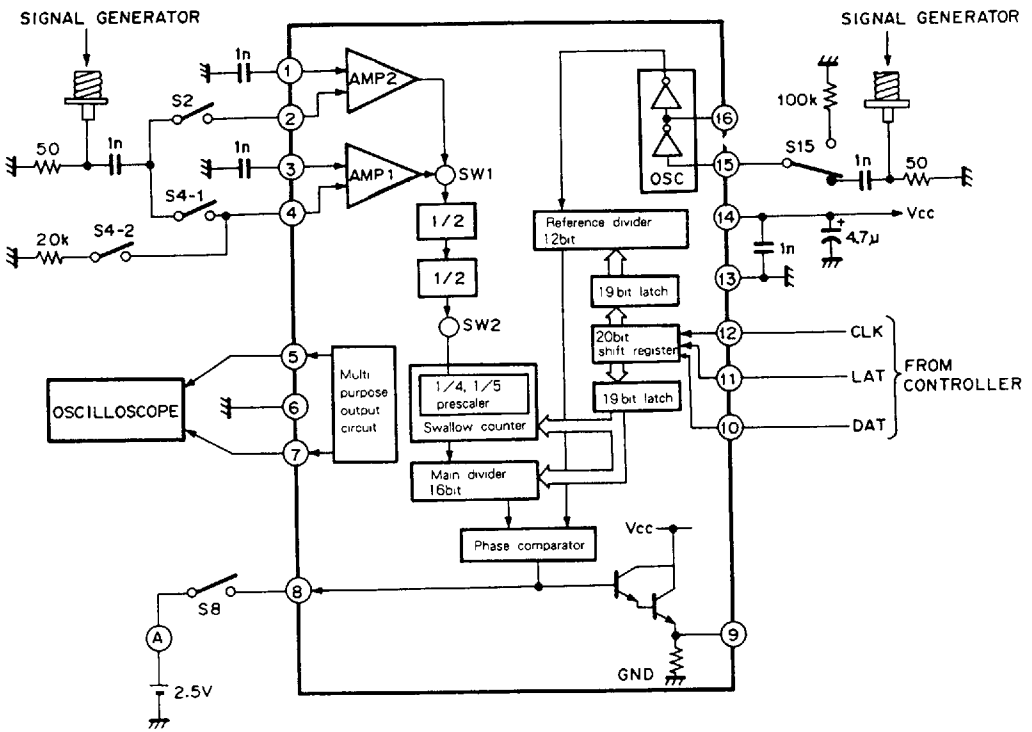
Electrical Characteristics

(Ta=–35 to +85°C, Vcc=4.5 to 5.5V, refer to Electrical Characteristics Test Circuit)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption		Icc	Ta=25°C, Vcc=5V f_{RF}=1600MHz, f_{XI}=12.8MHz S4-1 on	9	14	19	mA
Operating frequency		f_{RF}	S2 or S4-1 on, S15 on	80	—	1620	MHz
		f_{XI}	S4-2 on	1.5	—	20	MHz
Input voltage level		V_{fRF}	S2 or S4-1 on, S15 on	–10	—	6	dBm
		V_{fXI}	S4-2 on	0.5	—	2	Vp-p
DIN LAT CLK	"High" input voltage	V_{IH}		Vcc×0.7	—	—	V
	"Low" input voltage	V_{IL}		—	—	Vcc×0.3	V
	"High" input current	I_{IH}	V_{IH}=Vcc	–1	—	1	µA
	"Low" input current	I_{IL}	V_{IL}=GND	–1	—	1	µA
PDOUT	"High" output current	I_{OH}	V_{PDOUT}=2.5V Ta=25°C, Vcc=5V S8 on	–350	–220	–130	µA
	"Low" output current	I_{OL}		130	250	350	µA
	Leakage current in a state of high impedance	I_{OZ}		–0.3	—	0.3	µA
AO BO	"High" output voltage	V_{OH1}	I_L=–100 µA Ta=25°C, Vcc=5V T1=T2=Low	2.6	3.2	—	V
	"Low" output voltage	V_{OL1}	I_L=5 µA Ta=25°C, Vcc=5V T1=T2=Low	—	0.5	0.9	V
	"High" output voltage	V_{OH2}	Ta=25°C, Vcc=5V T1, T2; For the other than above data.	0.85	1.0	—	V
	"Low" output voltage	V_{OL2}		—	0.6	0.75	V

Electrical Characteristics Test Circuit



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Description of Operation

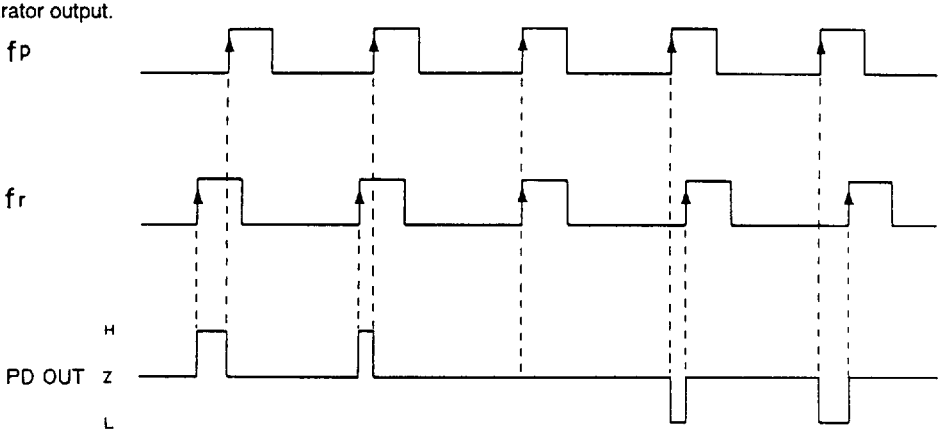
1. Signal Input from the Voltage Controlled Oscillator (VCO)

The CXA1356N has two independent high frequency input pins (RF1 and RF2).

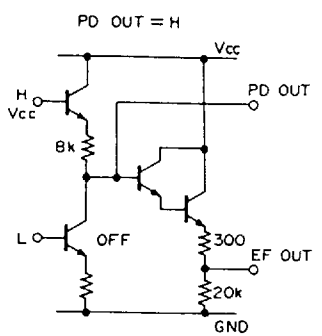
Each one of RF1 and RF2 is differential input circuits, each with a capacity to input signals from 80 to 1620MHz (refer to Pin Description). Balanced input usage is most appropriate, although single-end input is also enabled. For single-end input, the pin which signals will not be input connect GND with a capacitor.

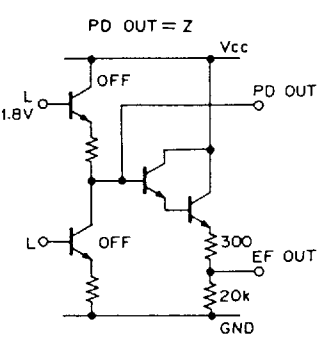
2. Phase Comparator Output

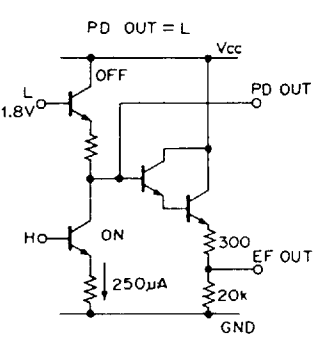
The phase comparator output consists of three levels: "High" level when the phase of the reference divider output leads that of the main divider output; "Low" level when the phase of the former follows that of the latter; and "High impedance" when both phases match. The diagram below illustrates the three levels of the phase comparator output.



fp: Main divider output
fr: Reference divider output







By utilizing Pin EFOUT, an active filter can be constructed with the built-in transistor, as shown in the Application Circuit. Also, independent use of Pin PDOUT is enabled, during which case no connections must be made to Pin EFOUT. Note that each constant of the low-pass filter is determined by the system needs.

3. Control Signal and Control Procedure

The CXA1356N is designed to work with a controller which consists of a general 4-bit/8-bit microprocessor. Three pins, CLK, LAT, and DIN, function as the control data input. As the output pins for control of the other systems, pins A0 and B0 are also available. By taking advantage of these pin usages, implementation of a simplified, multi-function system is enabled.

[1] Control signal input process

There are two signal input modes, DATA READ mode (normal mode) and DATA CHECK mode.

(a) DATA READ mode (normal mode)

To completely initialize this IC, two 20-bit data streams in this mode, totaling to 40 bits of data, must be input. First, set Pin LAT in "Low" state. When data is input to Pin DIN, the data is input into the shift register one bit at a time of the rising edge of the Pin CLK clock input. After 20 bits of data have been loaded into the shift register, the data is latched by setting Pin LAT to "High" while Pin CLK is in "High" state.

As explained in detail below, the data is input to either the main divider or reference divider, depending on the state of the final bit C. Upon actual usage of this IC, first input the 20-bit data which includes the frequency division number of the reference divider, input pin selection, and output data for Pins AO and BO, from the controller in the above sequence. At a time, the final bit C of the data should be "Low."

Next, input the following 20-bit data, which includes the data for the main divider setting, using the same method as before. At a time, the final bit C should be "High." The completion of this procedure will completely initialize the IC. After initiation, simply changing the latter 20-bit data will change the value of the main divider. (Bit C is also "High" for this procedure.)

(b) DATA CHECK mode

This mode is provided to verify whether if the data had been correctly loaded into the shift register by the controller. For data left in the shift register after latching the input data, inputting clock to Pin CLK will enable output of the data one bit at a time from Pin BO, during which time Pin CLK is maintained at "High" and Pin LAT at "Low." However, outputting shift register data from Pin BO is enabled only when data bits, T1 and T2 are "High" and "Low" respectively. Bits T1 and T2 are explained in the "Control data structure" section.

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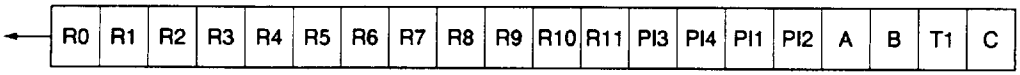
[2] Control data structure

Control data stream for the CXA1356N consists of 20 bits. The last of the data are identification code, which recognizes the purpose of the data stream. This code is also used in selecting the test mode for singular ICs. As explained below, the frequency division numbers for both main divider and reference divider consists of binary values starting with LSB.

(a) Control data for the reference divider (C=Low)

As this data is for initialization purposes, it is necessary to input this sequence upon power ON. The format of the input data is as assigned below:



R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	PI3	PI4	PI1	PI2	A	B	T1	C

- R0 to R11 : Reference divider frequency division number. (Binary values with R0 as LSB)
  There is an offset component between the actual frequency division number and the input data. Their relationship is as follows:
  (Actual frequency division number)=(Input data)+2

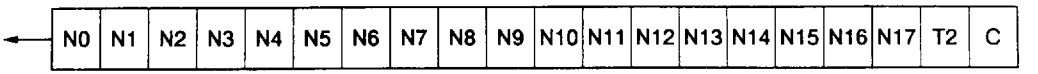
- PI1 to PI4 : Signal input pin selection.

PI1	PI2	PI3	PI4	
L	H	L	L	RF1 input (1/4 prescaler frequency division ratio)
H	H	L	L	RF2 input (1/4 prescaler frequency division ratio)

- A, B, T1 : Both Pins AO and BO have two functions, which depends on the value of T1. (T2=Low)
  When T1 is "Low, " A and B are output to Pins AO and BO respectively.
  When T1 is "High, " Pin AO outputs the signal for LOCK/UNLOCK state of the phase comparator.
  Pin AO: H : LOCK
  L : UNLOCK
  Pin BO outputs the shift register data by inputting clock to Pin CLK, as explained in section [1] (b) DATA CHECK mode. (Refer to Code Table of T1, T2, A, B; Page 9.)

- C : This code determines the latch direction of the input data. Input at "Low" for this case.

(b) Control data for the main divider (C=High)
This data determines the frequency division ratio of the main divider.



- N0 to N17 : Main divider frequency division number. (Binary values with N0 as LSB)
  Main divider has a 1/4 fixed divider circuit at the input, and the actual frequency division number is shown in the following relationship. (PI3=PI4=Low):

Range of Frequency Division Input Data N	Relationship between N and True Frequency Division Number ND	Range of True Frequency Division Number ND
4 to 262,143	4 • (N+8)	48 to 1,048,604

- T2 : Used to select test mode, this data should be "Low" for normal usage. When the main divider output and reference divider output are to be checked, set T2 and T1 at "High, " and A and B at "Low." Pins AO and BO will output the reference divider output and main divider output respectively.

- C : This code determines the latch direction of the input data. Input "High" for this case.

Input data				AO output	BO output
T1	T2	A	B		
L	L			A	B
H	L			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output

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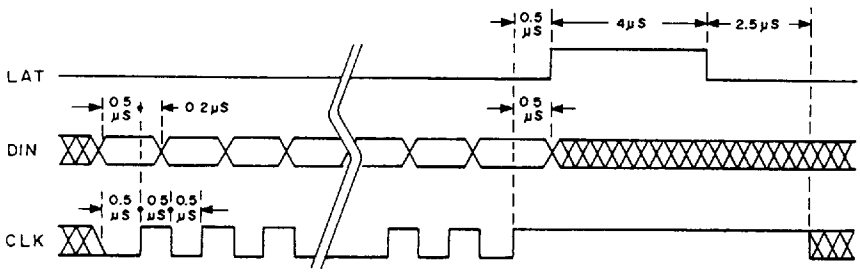
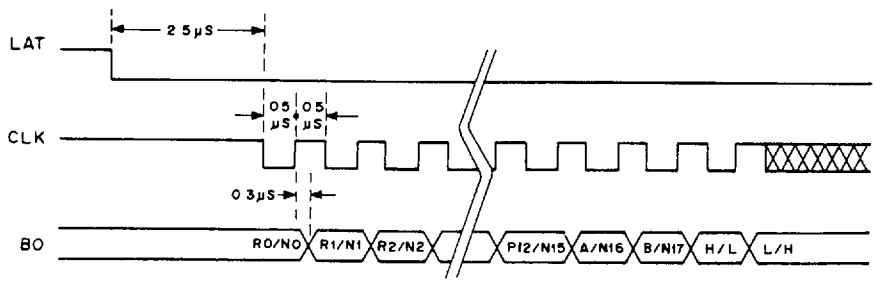
[3] Data input and control signal timing

(a) DATA READ mode (normal mode)



(b) DATA CHECK mode (shift register data check)

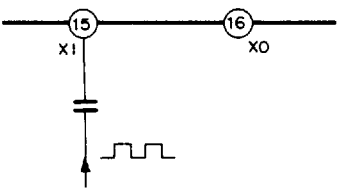


4. Reference Signal (Reference divider input signal)

Besides being able to use external clock as reference signal by inputting external signals to Pin XI, reference signal can also be generated by connecting a crystal unit to Pins XI and XO.

[1] Reference signal generation by external clock

When using the clock signals from external components, such as the controller, etc., input to Pin XI through a capacitor. The clock frequency range guarantees up to 20MHz, but for especially low frequencies, use signals with a slew rate of at least 2V/μs to prevent any operational errors.



[2] Reference signal generation by built-in oscillator

Connect a crystal unit to Pins XI and XO as shown in the figure below. For this procedure, use a crystal unit with a frequency of a few MHz, and check carefully the stability of the oscillation. Selection should be made so that the capacitance ratio of C_I and C_O is from 1:1 to 2:1, with the value set so that the serial capacitance of C_I and C_O is equivalent to the load capacitance of the crystal unit.

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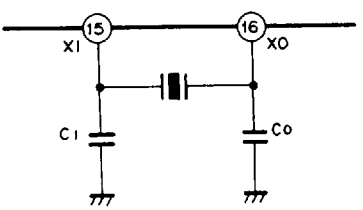
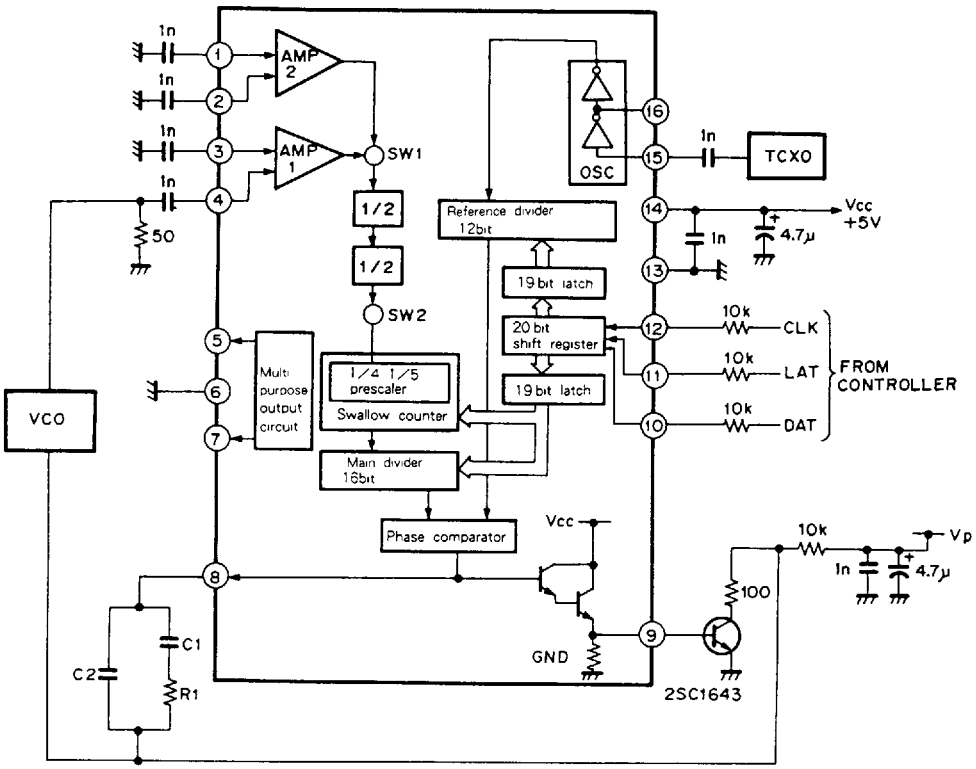


Notes on Operation

Take the following precautions upon usage of the CXA1356N:

- Ensure the shortest possible RF signal input path from VCO.
- Because Pins AO and BO, which check the internal operation of the IC, have low drive capacities due to low current operation, the lowest possible connection capacitance (2pF and below) should be used for this particular product design when evaluating the frequency division output. Otherwise, there stands the risk of the output oscillation becoming too small for measurement.
- In the CXA1356N, there is signals of frequency from a few kHz to over 1GHz. To suppress the interference of each signal, Vcc and GND1 should be connected through a ceramic capacitor at the shortest possible distance.

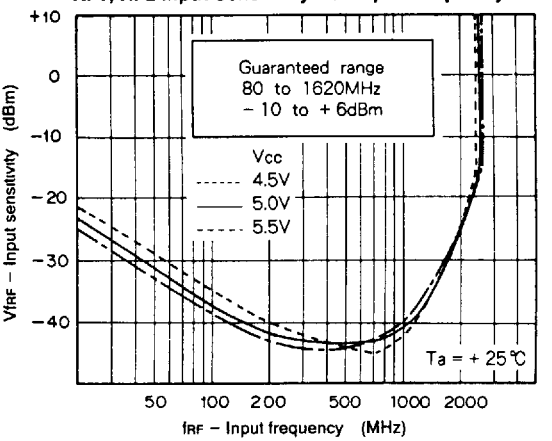
Application Circuit



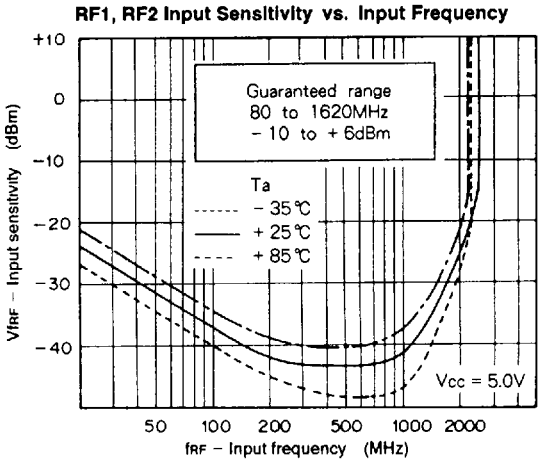
Application circuits shown are typical examples illustrating the operation of the devices Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

Example of Representative Characteristics

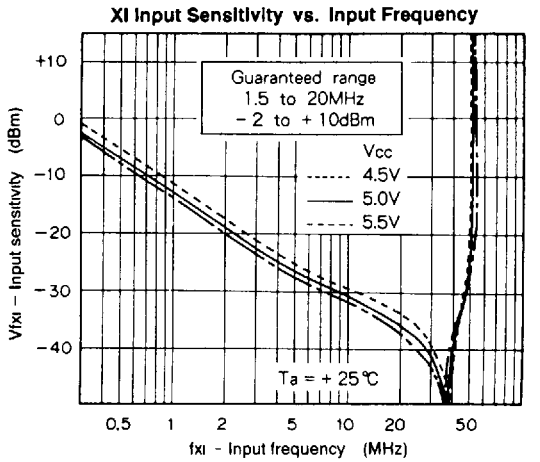
RF1, RF2 Input Sensitivity vs. Input Frequency



RF1, RF2 Input Sensitivity vs. Input Frequency



XI Input Sensitivity vs. Input Frequency



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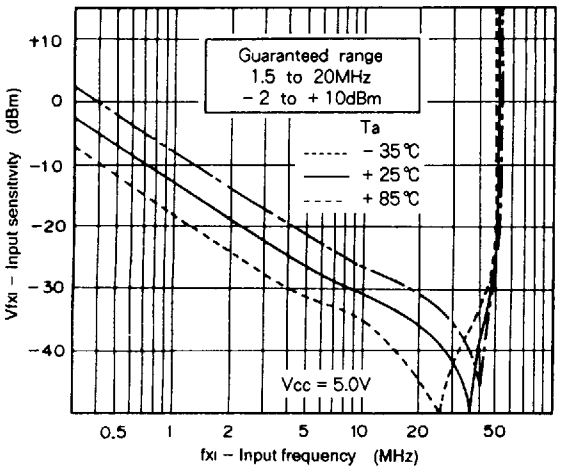
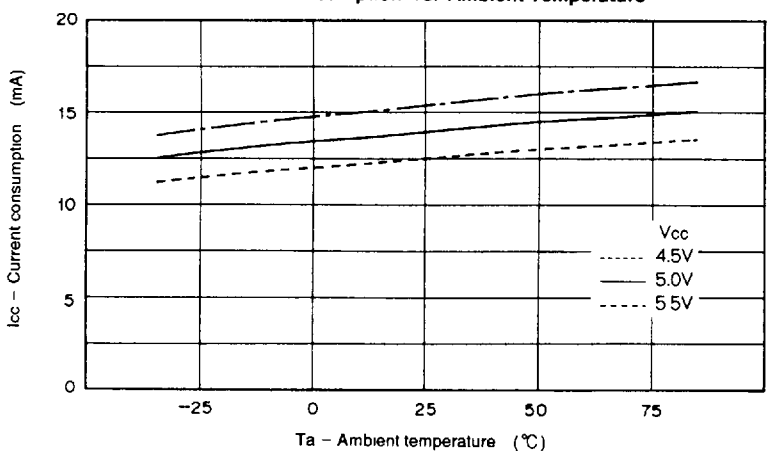
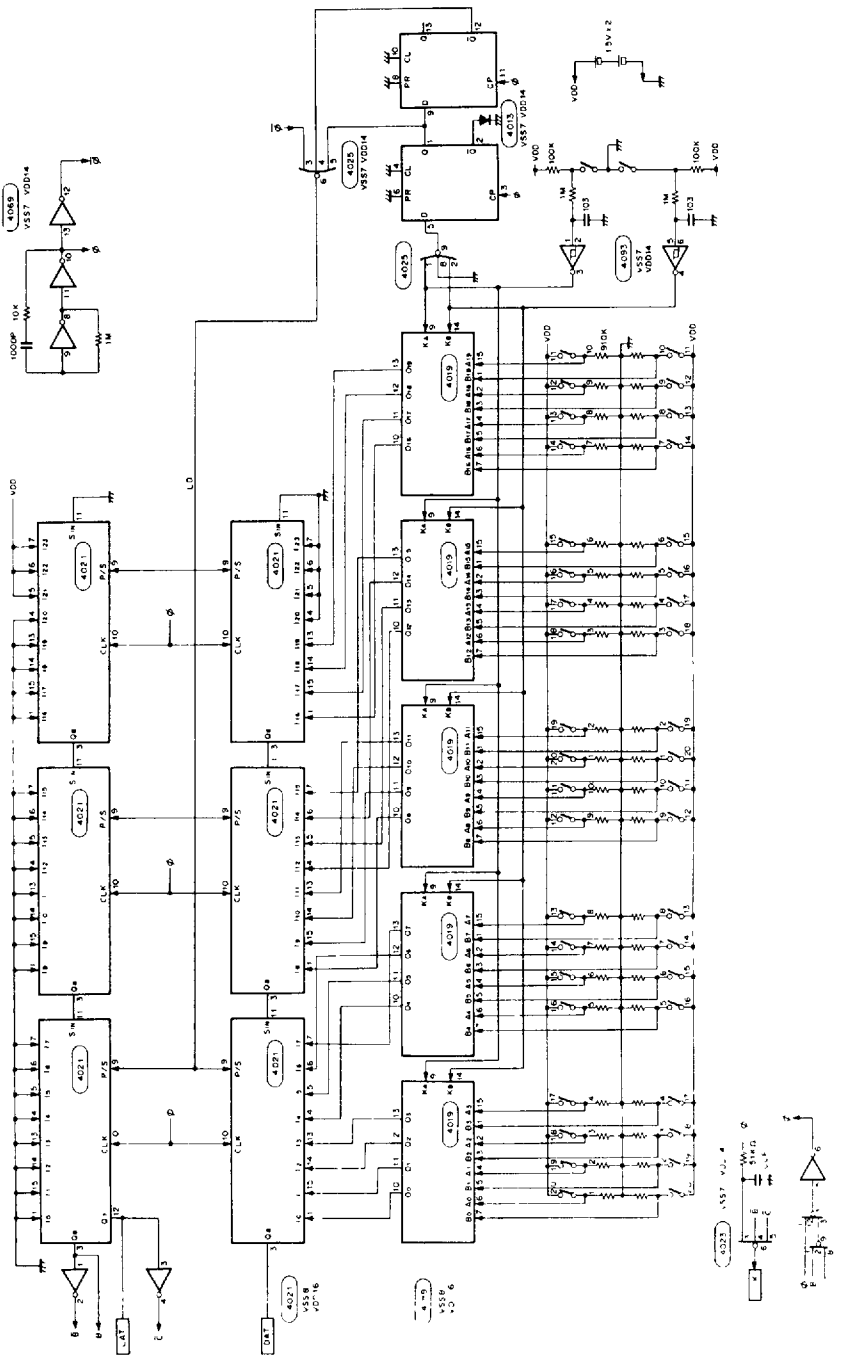
XI Input Sensitivity vs. Input Frequency



Current Consumption vs. Ambient Temperature



DATA, CLK, LATCH INPUT CIRCUIT



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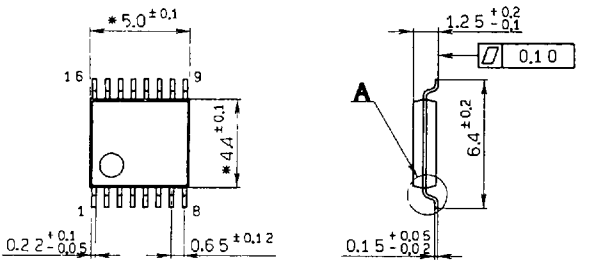
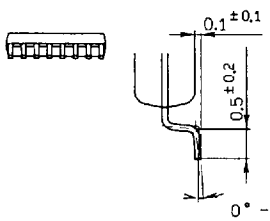
Package Outline Unit : mm

16pin VSOP (Plastic) 225mil





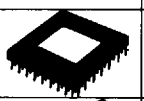
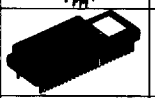
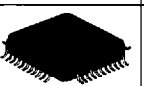
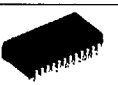
Detailed diagram of A

SONY NAME	VSOP-16P-L01
EIAJ NAME	SSOP016-P-0225- *
JEDEC CODE	———

* (Similar)

Note) Dimensions marked with * does not include resin residue

Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT L LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	QFJ	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		QFN	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P·····Plastic, C···Ceramic

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