



8Mx72 bits PC133 SDRAM Registered DIMM

with PLL, based on 8Mx8 SDRAM with LVTTL, 4 banks & 4K Refresh

HYM7V73AC801B H-Series

DESCRIPTION

The Hynix HYM7V73AC801B H-Series are 8Mx72bits ECC Synchronous DRAM Modules. The modules are composed of nine 8Mx8bits CMOS Synchronous DRAMs in 400mil 54pin TSOP-II package, two 18bits driver ICs in 56pin TSSOP package, one PLL clock driver in 24pin TSSOP package and one 2Kbits EEPROM in 8pin TSSOP package on a 168pin glass-epoxy printed circuit board. A 0.22uF and a 0.0022uF decoupling capacitors per each SDRAM are mounted on the PCB.

The HYM7V73AC801B H-Series are Dual In-line Memory Modules suitable for easy interchange and addition of 64Mbytes memory. The HYM7V73AC801B H-Series are offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. The DIMM /CAS latency in registered mode is one clock later than the device /CAS latency because of the register.

FEATURES

- PC133/100MHz support
- 168pin SDRAM Registered DIMM
- Serial Presence Detect with EEPROM
- 1.50" (38.10mm) Height PCB with Double Sided components
- Single 3.3 ± 0.3V power supply
- All devices pins are compatible with LVTTL interface
- Data mask function by DQM
- SDRAM internal banks : four banks
- Module bank : one physical bank
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
 - 1, 2, 4, 8, or Full Page for Sequential Burst
 - 1, 2, 4 or 8 for Interleave Burst
- Programmable /CAS Latency
 - Device /CAS Latency : 2, 3 clocks
 - DIMM /CAS Latency : 3, 4 clocks (registered mode)

ORDERING INFORMATION

PART NO.	MAX. FREQUENCY	INTERNAL BANK	REF.	POWER	SDRAM PACKAGE	PLATING
HYM7V73AC801BTHGC-75	133MHz	4 Banks	4K	Normal	TSOP-II	Gold

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PIN DESCRIPTION

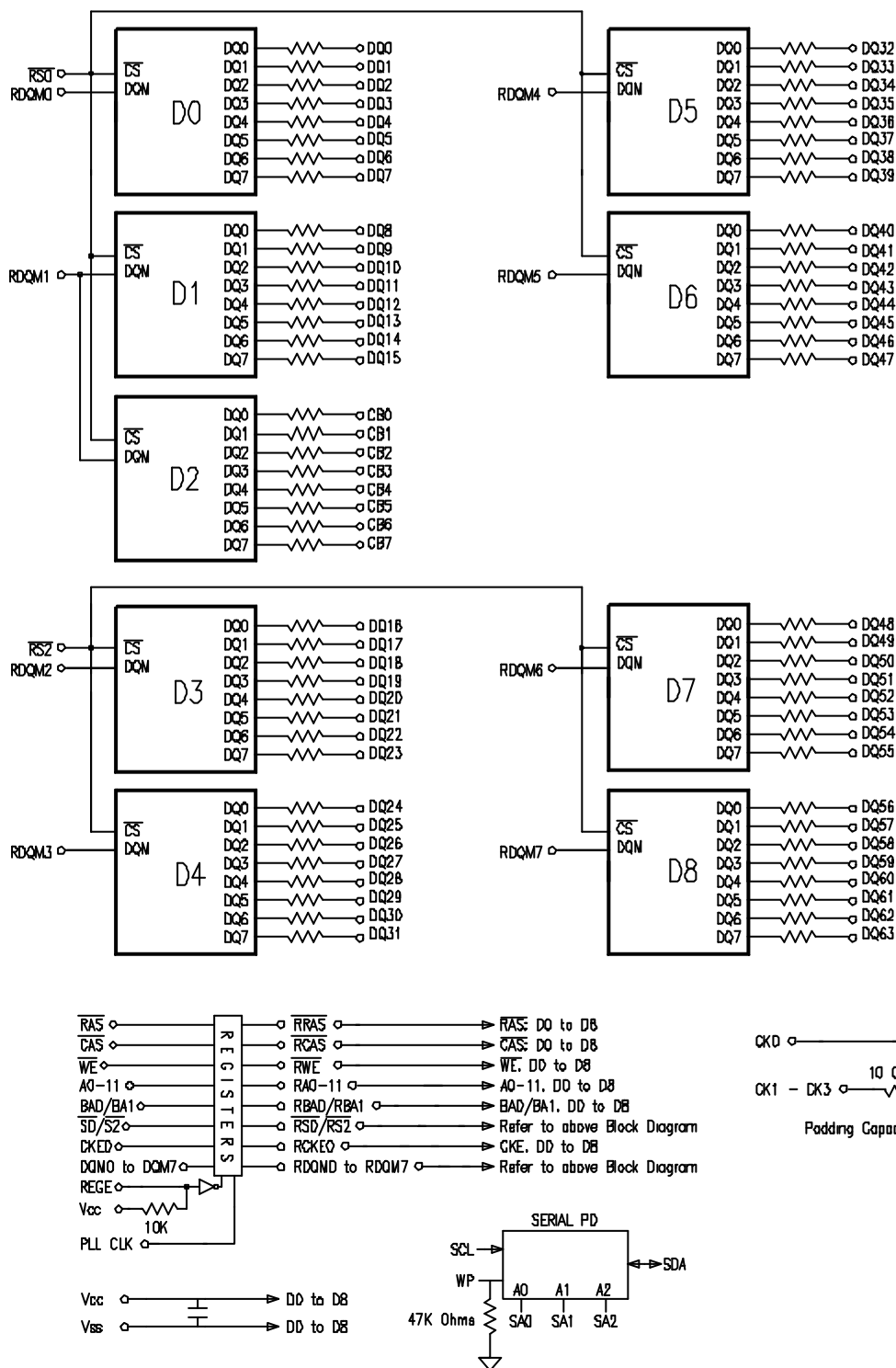
PIN NAME	DESCRIPTION	
CK0~CK3	Clock Inputs	The System Clock Input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE0	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.
/S0, /S2	Chip Select	Enables or disables all inputs except CK, CKE and DQM.
BA0, BA1	SDRAM Bank Address	Select bank to be activated during /RAS activity. Select bank to be read/written during /CAS activity
A0~A11	Address Inputs	Row address : RA0~RA11, Column address : CA0~CA8 Auto-precharge flag : A10
/RAS	Row Address Strobe	/RAS define the operation. Refer to the function truth table for details.
/CAS	Column Address Strobe	/CAS define the operation. Refer to the function truth table for details.
/WE	Write Enable	/WE define the operation. Refer to the function truth table for details.
REGE	Register Enable	Register Enable pin which permits the DIMM to operation in Buffered Mode when REGE input is Low, in Registered Mode when REGE input is High.
DQM0~DQM7	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode.
DQ0~DQ63	Data Input/Output	Multiplexed data input/output pins
CB0~CB7	ECC Data Input/Output	Error Checking and Correction Bits
VCC	Power Supply (3.3V)	Power supply for internal circuits and input/output buffers
VSS	Ground	Ground
SCL	SPD Clock Input	Serial Presence Detect Clock Input
SDA	SPD Data Input/Output	Serial Presence Detect Data input/output
SA0~SA2	SPD Address Input	Serial Presence Detect Address input
WP	Write Protect for SPD	Write Protect for Serial Presence Detect on DIMM
NC	No Connect	No Connect or Don't Use

PIN ASSIGNMENTS

FRONT SIDE		BACK SIDE		FRONT SIDE		BACK SIDE	
PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VSS	85	VSS	41	VCC	125	*CK1
2	DQ0	86	DQ32	42	CK0	126	NC
3	DQ1	87	DQ33	43	VSS	127	VSS
4	DQ2	88	DQ34	44	NC	128	CKE0
5	DQ3	89	DQ35	45	/S2	129	NC
6	VCC	90	VCC	46	DQM2	130	DQM6
7	DQ4	91	DQ36	47	DQM3	131	DQM7
8	DQ5	92	DQ37	48	NC	132	NC
9	DQ6	93	DQ38	49	VCC	133	VCC
10	DQ7	94	DQ39	50	NC	134	NC
Architecture Key				51	NC	135	NC
11	DQ8	95	DQ40	52	CB2	136	CB6
12	VSS	96	VSS	53	CB3	137	CB7
13	DQ9	97	DQ41	54	VSS	138	VSS
14	DQ10	98	DQ42	55	DQ16	139	DQ48
15	DQ11	99	DQ43	56	DQ17	140	DQ49
16	DQ12	100	DQ44	57	DQ18	141	DQ50
17	DQ13	101	DQ45	58	DQ19	142	DQ51
18	VCC	102	VCC	59	VCC	143	VCC
19	DQ14	103	DQ46	60	DQ20	144	DQ52
20	DQ15	104	DQ47	61	NC	145	NC
21	CB0	105	CB4	62	NC	146	NC
22	CB1	106	CB5	63	NC	147	REGE
23	VSS	107	VSS	64	VSS	148	VSS
24	NC	108	NC	65	DQ21	149	DQ53
25	NC	109	NC	66	DQ22	150	DQ54
26	VCC	110	VCC	67	DQ23	151	DQ55
27	/WE	111	/CAS	68	VSS	152	VSS
28	DQM0	112	DQM4	69	DQ24	153	DQ56
29	DQM1	113	DQM5	70	DQ25	154	DQ57
30	/S0	114	NC	71	DQ26	155	DQ58
31	NC	115	/RAS	72	DQ27	156	DQ59
32	VSS	116	VSS	73	VCC	157	VCC
33	A0	117	A1	74	DQ28	158	DQ60
34	A2	118	A3	75	DQ29	159	DQ61
35	A4	119	A5	76	DQ30	160	DQ62
36	A6	120	A7	77	DQ31	161	DQ63
37	A8	121	A9	78	VSS	162	VSS
38	A10/AP	122	BA0	79	*CK2	163	*CK3
39	BA1	123	A11	80	NC	164	NC
40	VCC	124	VCC	81	WP	165	SA0
Voltage Key				82	SDA	166	SA1
				83	SCL	167	SA2
				84	VCC	168	VCC

Note : *. CK1~CK3 are connected with termination R/C. (Refer to the Block Diagram.)

BLOCK DIAGRAM



Note : 1. The serial resistor values of DQs are 10 Ohms.
2. The padding capacitance of termination R/C for CK1-CK3 is 12pF.

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
		-75	-75	
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	12	0Ch	1
BYTE4	# of Column Addresses on This Assembly	9	09h	
BYTE5	# of Module Banks on This Assembly	1 Bank	01h	
BYTE6	Data Width of This Assembly	72 Bits	48h	
BYTE7	Data Width of This Assembly (Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTL	01h	
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	7.5ns	75h	9
BYTE10	Access Time from Clock @ /CAS Latency=3	5.4ns	54h	
BYTE11	DIMM Configuration Type	ECC	02h	
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported	80h	
BYTE13	Primary SDRAM Width	x8	08h	
BYTE14	Error Checking SDRAM Width	x8	08h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD = 1 CLK	01h	
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on Each SDRAM Device	4 Banks	04h	
BYTE18	SDRAM Device Attributes, CAS # Latency	/CAS Latency=2,3	06h	
BYTE19	SDRAM Device Attributes, CS # Latency	/CS Latency=0	01h	
BYTE20	SDRAM Device Attributes, Write Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes	Registered/Buffered Inputs, with PLL	1Fh	
BYTE22	SDRAM Device Attributes, General	+/-10% voltage tolerance, Burst Read Single bit Write, Precharge All, Auto Precharge, Early RAS Precharge	0Eh	
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	10ns	A0h	9
BYTE24	Access Time from Clock @ /CAS Latency=2	6ns	60h	
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	-	00h	
BYTE26	Access Time from Clock @ /CAS Latency=1	-	00h	
BYTE27	Minimum Row Precharge Time (tRP)	20ns	14h	
BYTE28	Minimum Row Active to Row Active Delay (tRRD)	15ns	0Fh	
BYTE29	Minimum /RAS to /CAS Delay (tRCD)	20ns	14h	
BYTE30	Minimum /RAS Pulse width (tRAS)	45ns	2Dh	
BYTE31	Module Bank Density	64MB	10h	
BYTE32	Command and Address Signal Input Setup Time	1.5ns	15h	
BYTE33	Command and Address Signal Input Hold Time	0.8ns	08h	
BYTE34	Data Signal Input Setup Time	1.5ns	15h	
BYTE35	Data Signal Input Hold Time	0.8ns	08h	
BYTE36 -61	Superset Information (may be used in future)	-	00h	
BYTE62	SPD Revision	Intel SPD 1.2	12h	3, 4
BYTE63	Checksum for Bytes 0-62	-	CFh	
BYTE64	Manufacturer JEDEC ID Code	Hynix JEDEC ID	ADh	
BYTE65 -71	Manufacturer JEDEC ID Code	Unused	FFh	
BYTE72	Manufacturing Location	Hynix (Korea Area) HSA (United States Area) HSU (Europe Area) HSJ (Japan Area) Asia Area	0*h 1*h 2*h 3*h 4*h	10

Continued

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
		-75	-75	
BYTE73	Manufacturer's Part Number (Component)	7 (SDRAM)	37h	5, 6
BYTE74	Manufacturer's Part Number (Voltage Interface)	V (3.3V, LVTTTL)	56h	5, 6
BYTE75	Manufacturer's Part Number (Data Width)	7	37h	5, 6
BYTE76	Manufacturer's Part Number (Data Width)	3	33h	5, 6
BYTE77	Manufacturer's Part Number (ECC)	A	41h	5, 6
BYTE78	Manufacturer's Part Number (Reg. DIMM Type)	C (RCC Registered with PLL)	43h	5, 6
BYTE79	Manufacturer's Part Number (Memory Depth)	8	38h	5, 6
BYTE80	Manufacturer's Part Number (Refresh)	0 (4K Refresh)	30h	5, 6
BYTE81	Manufacturer's Part Number (Internal Banks)	1 (4 Banks)	31h	5, 6
BYTE82	Manufacturer's Part Number (Generation)	B	42h	5, 6
BYTE83	Manufacturer's Part Number (Package Type)	T (TSOPII)	54h	5, 6
BYTE84	Manufacturer's Part Number (Module Type)	H (x8 based Registered DIMM)	48h	5, 6
BYTE85	Manufacturer's Part Number (Plating Type)	G (Gold)	47h	5, 6
BYTE86	Manufacturer's Part Number (Hyphen)	- (Hyphen)	2Dh	5, 6
BYTE87	Manufacturer's Part Number (Min. Cycle Time)	7	37h	5, 6
BYTE88	Manufacturer's Part Number (Min. Cycle Time)	5	35h	5, 6
BYTE89 ~90	Manufacturer's Part Number	Blank	20h	5, 6
BYTE91	Revision Code (for Component)	Process Code	-	5, 7
BYTE92	Revision Code (for PCB)	Process Code	-	5, 7
BYTE93	Manufacturing Date	Work Week	-	3, 7
BYTE94	Manufacturing Date	Year	-	3, 7
BYTE95 ~98	Assembly Serial Number	Serial Number	-	7
BYTE99 ~125	Manufacturer Specific Data (may be used in future)	None	00h	
BYTE126	Reserved	Refer to Note8	64h	4, 8
BYTE127	Intel specification details for 100MHZ support	Refer to Note8	87h	4, 8
BYTE128 ~256	Unused Storage Locations	-	00h	

- Note:** 1. The bank address is excluded.
2. 1,2,4,8 for Interleave Burst Type
3. BCD adopted.
4. Refer to the most recent version of the Intel and JEDEC SPD Specification.
5. ASCII adopted.
6. Basically Hynix writes Part No. except for `HYM` in Byte 73-90 to use the limited 18 bytes from byte 73 to 90 efficiently.
7. Not fixed but dependent.
8. These values apply to PC100 applications only, per Intel PC SDRAM SPD specification
9. In a registered DIMM, data is delayed an additional clock cycle due to the register (that is, Device CL + 1 = DIMM CL)
10. Refer to Hynix Web Site.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	MA
Power Dissipation	PD	9	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum can adversely affect device reliability.

DC OPERATING CONDITION

(TA = 0 to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Power Supply Voltage	VCC	3.0	3.3	3.6	V	1
Input High Voltage	VIH	2.0	3.0	VCC + 2.0	V	1, 2
Input Low Voltage	VIL	VSS – 2.0	0	0.8	V	1, 3

Note : 1. All voltage are referenced to VSS = 0V.
 2. VIH (max) is acceptable 5.6V AC pulse width with ≤ 3ns of duration.
 3. VIL (min) is acceptable –2.0V AC pulse width with ≤ 3ns of duration.

AC OPERATING CONDITION

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V, VSS = 0V)

PARAMETER	SYMBOL	VALUE	UNIT
AC Input High / Low Level Voltage	VIH / VIL	2.4 / 0.4	V
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V
Input Rise / Fall Time	tR / tF	1	ns
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V
Output Load Capacitance for Access Time Measurement	CL	*Note	pF

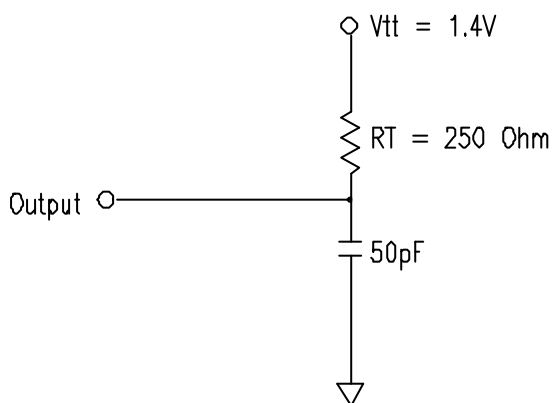
Note : *. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF).
 For details, refer to AC/DC output circuit.

CAPACITANCE

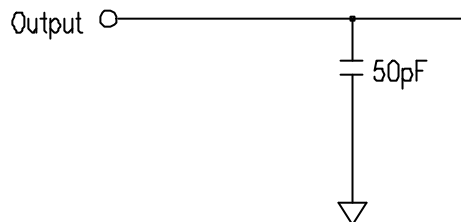
(TA = 25°C, f = 1MHz)

PARAMETER	PIN	SYMBOL	MIN	MAX	TYP.	UNIT
Input Capacitance	CK0	CIN1	-	32	-	pF
	CKE0	CIN2	-	16	-	pF
	/S0, /S1	CIN3	-	16	-	pF
	A0~A11, BA0, BA1	CIN4	-	16	-	pF
	/RAS, /CAS, /WE	CIN5	-	16	-	pF
	DQM0~DQM7	CIN6	-	16	-	pF
Data Input/Output Capacitance	DQ0~DQ63, CB0~CB7	CI/O	-	17	-	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit



AC Output Load Circuit

DC CHARACTERISTICS I

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V)

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Input Leakage Current	ILI	-10	10	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

Note : 1. VIN = 0 to 3.6V. All other pins are not tested under VIN = 0V.
2. DOUT is disabled. VOUT = 0 to 3.6V.

DC CHARACTERISTICS II

(TA = 0 to 70°C, VDD = 3.3 ± 0.3V, VSS = 0V)

PARAMETER	SYMBOL	TEST CONDITION	SPEED	UNIT	NOTE
			-75		
Operating Current	IDD1	Burst Length = 1, One bank active tRC ≥ tRC(min), IOL = 0mA	1130	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = min	338	mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	108	mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD - 0.2V or ≤ 0.2V	535	mA	
	IDD2NS	CKE ≥ VIH(max), tCK = ∞ Input signals are stable.	225	mA	
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = min	365	mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞	135	mA	
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD - 0.2V or ≤ 0.2V	670	mA	
	IDD3NS	CKE ≥ VIH(max), tCK = ∞ Input signals are stable.	360	mA	
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL = 0mA All banks active	CL = 3	mA	1
			CL = 2		
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active	2000	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V	tCK = min	mA	
			tCK = ∞	mA	

Note : 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRRC (Refresh /RAS cycle time) is shown at AC CHARACTERISTICS II.
3. All values are measured with Registers and PLL.

AC CHARACTERISTICS I

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	-75		UNIT	NOTE
			MIN	MAX		
System Clock Cycle Time	/CAS Latency = 3	tCK3	7.5	1000	ns	1
	/CAS Latency = 2	tCK2	10			
Clock High Pulse Width		tCHW	2.5	-	ns	2
Clock Low Pulse Width		tCLW	2.5	-	ns	2
Access Time from Clock	/CAS Latency = 3	tAC3	-	5.4	ns	3
	/CAS Latency = 2	tAC2	-	6		
Data-Out Hold Time		tOH	2.7	-	ns	
Data-Input Setup Time		tDS	1.5	-	ns	2
Data-Input Hold Time		tDH	0.8	-	ns	2
Address Setup Time		tDS	1.5	-	ns	2
Address Hold Time		tDH	0.8	-	ns	2
CKE Setup Time		tDS	1.5	-	ns	2
CKE Hold Time		tDH	0.8	-	ns	2
Command Setup Time		tDS	1.5	-	ns	2
Command Hold Time		tDH	0.8	-	ns	2
CLK to Data Output in Low-Z time		tOLZ	1	-	ns	
CLK to Data Output in High-Z time	/CAS Latency = 3	tOHZ3	2.7	5.4	ns	
	/CAS Latency = 2	tOHZ2	3	6		

Note : 1. In a registered DIMM, data is delayed an additional clock cycle due to the register (that is, Device CL + 1 = DIMM CL).
 2. Assume tR / tF (input rise and fall time) is 1ns.
 3. Access times to be measured with input signals of 1v/ns edge rate.

AC CHARACTERISTICS II

PARAMETER		SYMBOL	-75		UNIT	NOTE
			MIN	MAX		
/RAS Cycle Time	Operation	tRC	65	-	ns	
	Auto Refresh	tRRC	65			
/RAS to /CAS Delay		tRCD	20	-	ns	
/RAS Active Time		tRAS	45	100K	ns	
/RAS Precharge Time		tRP	20	-	ns	
/RAS to /RAS Bank Active Delay		tRRD	15	-	ns	
/CAS to /CAS Delay		tCCD	1	-	CLK	
Write Command to Data-in Delay		tWTL	1	-	CLK	1
Data-in to Precharge Command		tDPL	0	-	CLK	1
Data-in to Active Command		tDAL	3	-	CLK	1
DQM to Data-out Hi-Z		tDQZ	3	-	CLK	1
DQM to Data-in Mask		tDQM	0	-	CLK	
MRS to New Command		tMRD	2	-	CLK	
Precharge to Data Output Hi-Z	/CAS Latency = 3	tPROZ3	4	-	CLK	1
	/CAS Latency = 2	tPROZ2	3	-		
Power Down Exit Time		tPDE	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	CLK	2
Refresh Time		tREF	-	64	ms	

Note : 1. Timing delay due to the register is considered in a registered DIMM.
2. A new command can be given tRRC after self refresh exit.

OPERATING OPTION TABLE

	/CAS LATENCY	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz (7.5ns)	3CLKS	3CLKS	6CLKS	9CLKS	3CLKS	5.4ns	2.7ns
125MHz (8.0ns)	3CLKS	3CLKS	6CLKS	9CLKS	3CLKS	6ns	3ns
100MHz (10.0ns)	2CLKS	2CLKS	5CLKS	7CLKS	2CLKS	6ns	3ns

Note : DIMM /CAS Latency = Device CL + 1 (Registered mode)

COMMAND TRUTH TABLE

		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/ AP	BA	NOTE
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge Selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Self Refresh	Entry	H	L	L	L	L	H	X	X			1
	Exit	L	H	H	X	X	X	X				
Precharge Power Down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note : 1. Existing Self Refresh occurs by asynchronously bringing CKE from low to high.

2. X = Don't care, H = Logic High, L = logic Low, BA = Bank Address, CA = Column Address, OP code = Operand code, NOP = No operation

PACKAGE DIMENSIONS

