REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to table I, figure 3, figure 7, and editorial changes throughout.	1988 NOV 16	M. A. Frye
B	Remove vendor CAGE number 50364 as a source of supply for device types 09 through 11. Changes to table I and figure 8. Editorial changes throughout.	1989 OCT 30	M. A. Frye

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV	B	B	B	B	B		A	A	B	B			B			A	B		B	B			
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20			

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: James E. Johnson

CHECKED BY: Charles Reusing

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 17 DECEMBER 1987

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, BIPOLAR, FIRST-IN FIRST-OUT (FIFO), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87791

SHEET 1 OF 1

DESC FORM 193
SEP 87

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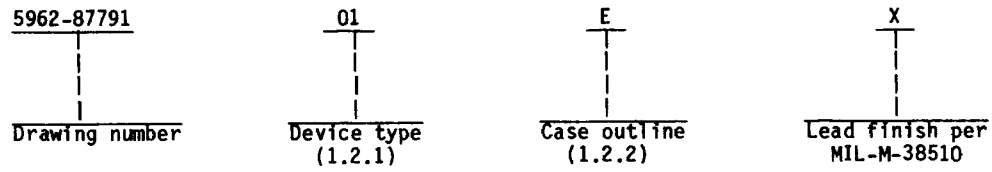
5962-E1386

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	57401	7 MHz 64x4 stand-alone first-in first-out memory
02	57402	7 MHz 64x5 stand-alone first-in first-out memory
03	57401A	10 MHz 64x4 stand-alone first-in first-out memory
04	57402A	10 MHz 64x5 stand-alone first-in first-out memory
05	C57401	7 MHz 64x4 cascadable first-in first-out memory
06	C57402	7 MHz 64x5 cascadable first-in first-out memory
07	C57401A	10 MHz 64x4 cascadable first-in first-out memory
08	C57402A	10 MHz 64x5 cascadable first-in first-out memory
09	57L401D	12 MHz 64x4 stand-alone first-in first-out memory
10	57L402D	12 MHz 64x5 stand-alone first-in first-out memory
11	57L4013D	12 MHz 64x4 stand-alone three-state first-in first-out memory

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
V	D-6 (18-lead, .960" x .310" x .200"), dual-in-line package
2	C-2 (20-lead, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7 V dc
Input voltage range	-1.5 V dc to +7 V dc
Storage temperature range	-65°C to +150°C
Lead temperature:	
Soldering, 5 seconds, E and V outline	+300°C
Soldering, 10 seconds, 2 outline	+260°C
Thermal resistance, junction-to-case (θ_{JC}) 1/	See MIL-M-38510, appendix C
Output voltage applied range	-0.5 V dc to +5.5 V dc
Output sink current	100 mA

1/ Heat sinking is recommended to reduce the junction temperature.

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Maximum power dissipation (P_D) 2/:	
Device types 01 and 05	880 mW
Device types 02, 03, 06, and 07	990 mW
Device types 04 and 08	1.1 W
Device types 09, 10, and 11	660 mW
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Case operating temperature range (T_C)	-55°C to +125°C
Static low level input voltage (V_{IL1})	0.8 V maximum 3/
Static high level input voltage (V_{IH1})	2.0 V minimum 3/
AC low level input voltage (V_{IL2})	0 V maximum 3/
AC high level input voltage (V_{IH2})	3.0 V minimum 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
3/ These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagrams. The logic diagrams shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA	1, 2, 3	All		-1.5	V
Low level input current	I_{IL1}	V_{CC} = 5.5 V, V_I = 0.45 V D_O-D_n, $\overline{MR}$	1, 2, 3	01-08		-0.8	mA
	I_{IL2}	V_{CC} = 5.5 V, V_I = 0.45 V SI, SO	1, 2, 3	01-08		-1.6	mA
	I_{IL}	V_{CC} = 5.5 V, V_I = 0.45 V	1, 2, 3	09,10, 11		-250	µA
High level input current	I_{IH}	V_{CC} = 5.5 V, V_I = 2.4 V	1, 2, 3	All		50	µA
Maximum input current	I_I	V_{CC} = 5.5 V, V_I = 5.5 V	1, 2, 3	All		1	mA
Low level output current	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	01-08		0.5	V
		V_{CC} = 4.5 V, I_{OL} = 12 mA O_O-O_n V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	09,10, 11		0.5	V
		V_{IL} = 0.8 V, V_{IH} = 2.0 V V_{CC} = 4.5 V, I_{OL} = 8 mA IR, OR	1, 2, 3	09,10, 11		0.5	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -0.9 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	01-08	2.4		V
		V_{IL} = 0.8 V, V_{IH} = 2.0 V V_{CC} = 4.5 V, I_{OH} = -3.0 mA O_O-O_n	1, 2, 3	09,10, 11	2.4		V
		V_{IL} = 0.8 V, V_{IH} = 2.0 V V_{CC} = 4.5 V, I_{OH} = -0.9 mA IR, OR	1, 2, 3	09,10, 11	2.4		V
Output short-circuit current 1/	I_{OS}	V_{CC} = 5.5 V, V_O = 0 V V_{CC} = 6.0 V, V_O = 0.5 V	1, 2, 3	09,10, 11 01-08	-20	-90	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Off-state output current	I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V	1, 2, 3	11		-50	µA
Off-state output current	I_{OZH}	V_{CC} = 5.5 V, V_O = 2.4 V	1, 2, 3	11		50	µA
Supply current	I_{CC}	V_{CC} = 5.5 V, Inputs low, outputs open	1, 2, 3	01,05		160	mA
				02,03, 06,07		180	mA
				04,08		200	mA
				09,10, 11		120	mA
Shift out high to output ready low	t_{ORL}	See figure 3	9, 10, 11	01-08		65	ns
				09,10, 11		55	ns
Shift out low to output ready high	t_{ORH}			01,02, 05,06		70	ns
				03,04, 07,08		65	ns
				09,10, 11		55	ns
Shift out rate 2/	f_{OUT}			01,02, 05,06		7	MHz
				03,04, 07,08		10	MHz
				09,10, 11		12	MHz
Output data hold	t_{ODH}			All	10		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output data shift	t_{ODS}	See figure 3	9, 10, 11	01,02, 05,06		65	ns
				03,04, 07,08		60	ns
				09,10, 11		50	ns
Output ready high to data valid	t_{ORD}			09,10, 11		0	ns
Shift out high time 2/	t_{SOH}			01,02, 05,06	45		ns
				03,04, 07,08	35		
				09,10, 11	28		
Shift out low time 2/	t_{SOL}			01,02, 05,06	45		ns
				03,04, 07,08	35		
				09,10, 11	18		
Shift in rate 2/	f_{IN}	See figure 4	9, 10, 11	01,02, 05,06		7	MHz
				03,04, 07,08		10	MHz
				09,10, 11		12	MHz
Shift in high to input ready low	t_{IRL}			01,02, 05,06		60	ns
				03,04, 07-11		50	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Shift in low to input ready high	t_{IRH}	See figure 4	9, 10, 11	01,02, 05,06		60	ns
				03,04, 07,08		50	ns
				09,10, 11		30	ns
Shift in high time 2/	t_{SIH}			01,02, 05,06	45		ns
				03,04, 07,08	35		
				09,10, 11	30		
Shift in low time 2/	t_{SIL}			01,02, 05,06	45		ns
				03,04, 07,08	35		
				09,10, 11	15		
Input data setup to SI 2/	t_{IDS}			01,02	10		ns
				03,04	5		
				05,06, 07,08, 09,10, 11	0		
Input data hold time to SI 2/	t_{IDH}			01,02, 05,06	55		ns
				03,04, 07,08	45		
				09,10, 11	35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data throughput	t_{PT}	See figures 5 and 6	9, 10, 11	01,02, 05,06		4	µs
				03,04, 07,08		2.2	µs
				09,10, 11		2	µs
Output ready pulse high 3/	t_{OPH}	See figure 5	9, 10, 11	01-04, 09,10, 11	20		ns
				05-08	30		ns
Input ready pulse high 3/	t_{IPH}	See figure 6	9, 10, 11	01-04	20		ns
				05-08	30		ns
				09,10, 11	15		ns
Input data setup to IR 2/	t_{RIDS}	See figure 6	9, 10, 11	09,10, 11	0		ns
Input data hold time to IR 2/	t_{RIDH}		9, 10, 11	09,10, 11	35		ns
Master reset pulse 2/	t_{MRW}	See figure 7	9, 10, 11	01,02, 05,06	30		ns
				03,04, 07-11	40		
Master reset to SI 3/	t_{MRS}			All	45		ns
Master reset low to output ready low	t_{MRORL}			All		65	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Master reset high to input ready high	t_{MRIRH}	See figure 7	9, 10, 11		01-08	65	ns
				09,10, 11		35	ns
Master reset low to input ready low	t_{MRIRL}			09,10, 11		55	ns
Master reset low to output low	t_{MRO}			09,10, 11		75	ns
Output disable delay high	t_{PHZ}	See figures 8 and 9	9, 10, 11	11		35	ns
Output disable delay low	t_{PLZ}			11		35	ns
Output enable delay low	t_{PZL}			11		35	ns
Output enable delay high	t_{PZH}			11		45	ns

1/ No more than one output should be shorted at a time and duration of the short-circuit should not exceed 1 second.
2/ These are input conditions whose minimum values when applied shall result in the part meeting all the requirements of table I.
3/ For device types 01-08, t_{IPH} and t_{OPH} are tested initially and after any design change.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

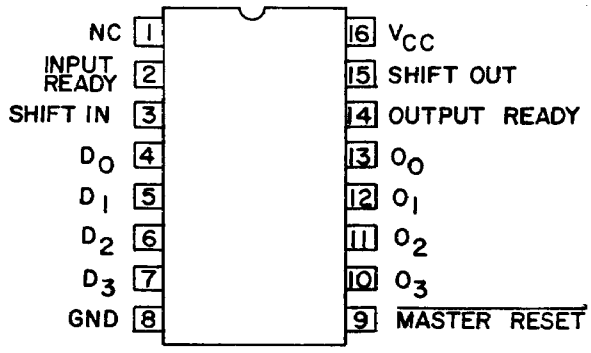
a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

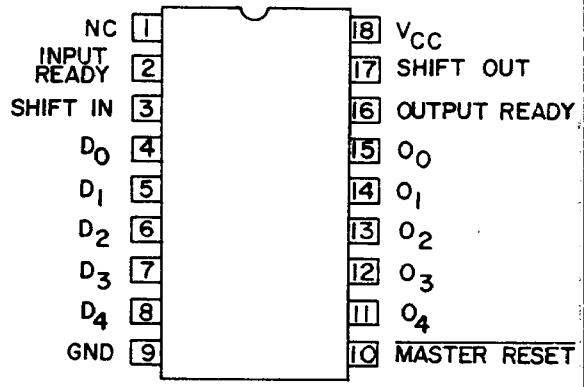
(2) $T_A = +125°C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

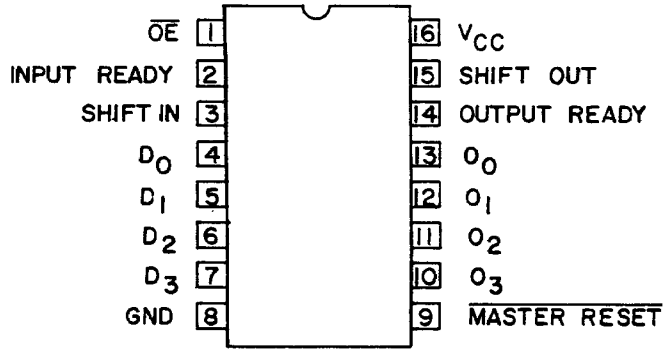
Device types 01, 03, 05, 07, and 09



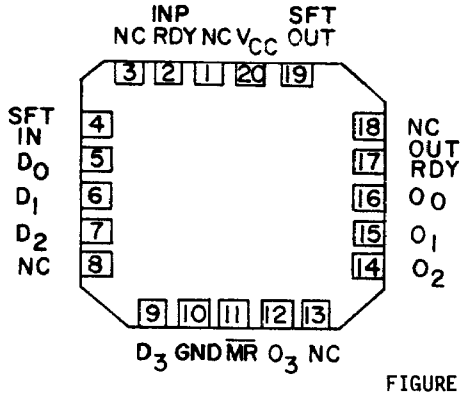
Device types 02, 04, 06, 08, and 10



Device type 11



Device types 01, 03, 05, and 07



Device types 02, 04, 06, and 08

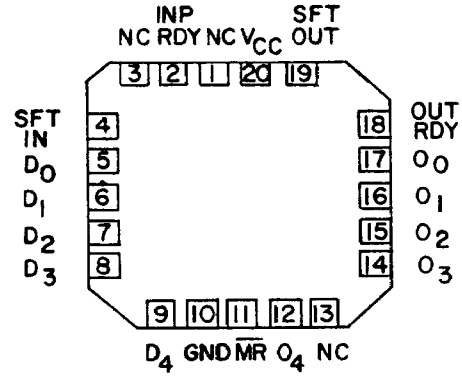


FIGURE 1. Terminal connections.

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		REVISION LEVEL	SHEET 11

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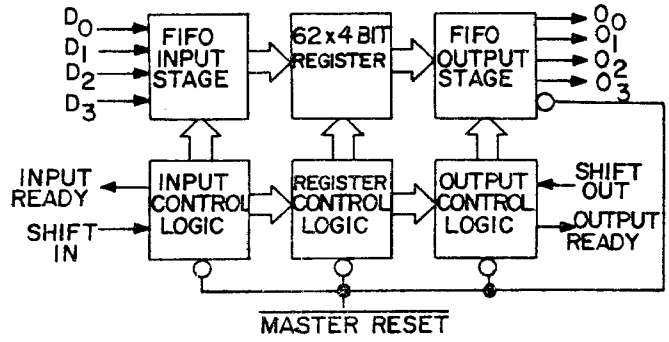
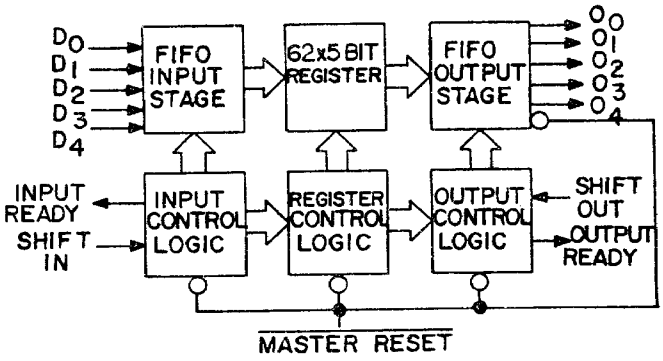
Device types 01, 03, 05, 07, and 09



Device types 02, 04, 06, 08, and 10



Device type 11

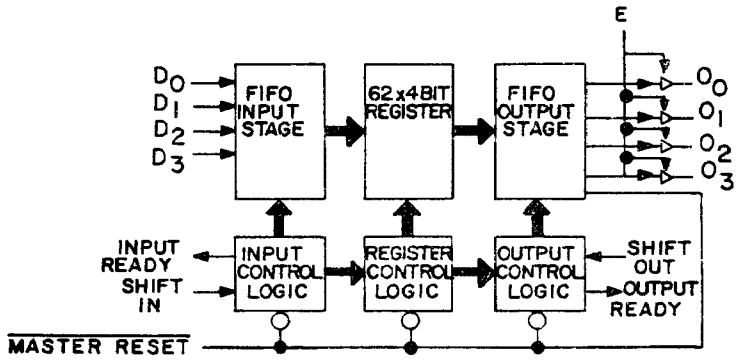
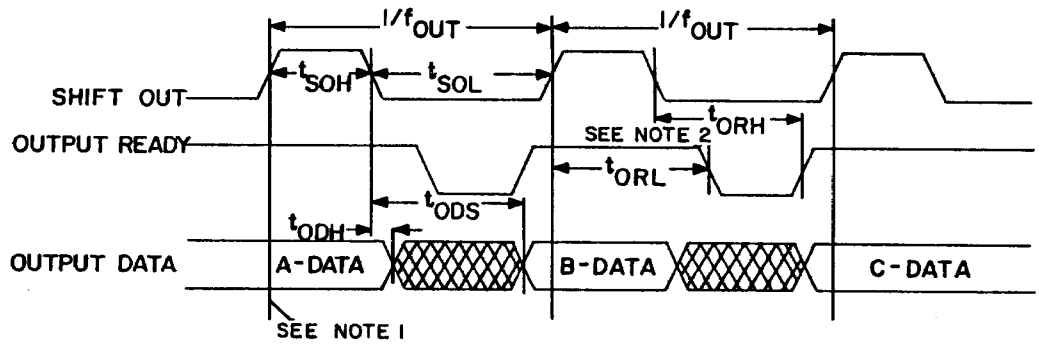


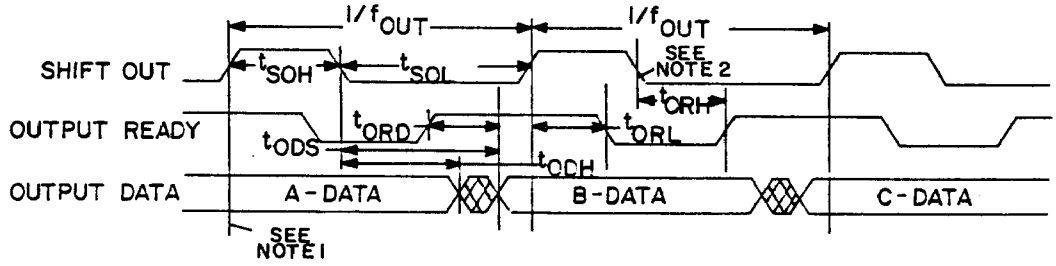
FIGURE 2. Logic diagrams.

Device types 01 - 08



NOTES:
1. The diagram assumes that at this time words 63, 62, and 61 are loaded with A, B, and C data respectively.
2. Data is shifted out when shift out makes a high to low transition.

Device types 09, 10, and 11



NOTES:
1. The diagram assumes that at this time words 63, 62, and 61 are loaded with A, B, and C data respectively.
2. Output data changes on the falling edge of SO after a valid shift-out sequence, i.e., OR and SO are both high together.

FIGURE 3. Output timing diagrams.

Device types 01 - 11

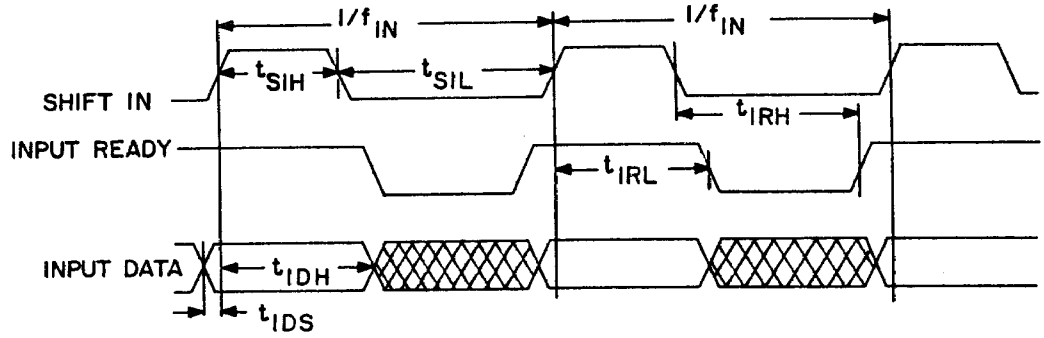
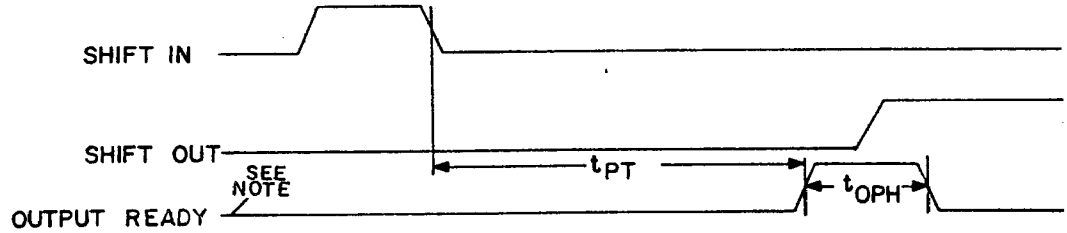


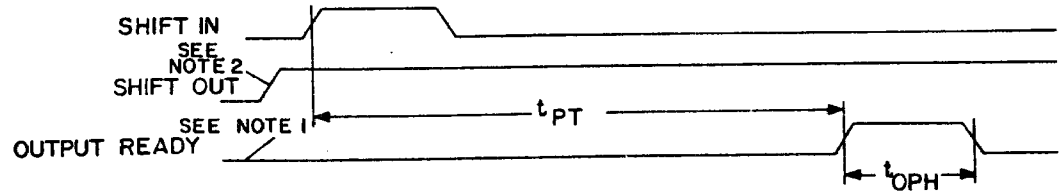
FIGURE 4. Input timing diagram.

Device types 01 - 08



NOTE: FIFO initially empty.

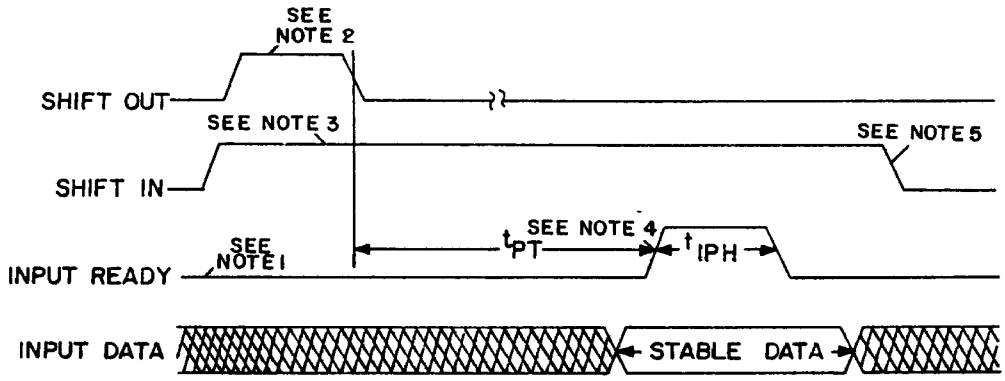
Device types 09, 10, 11



NOTES:
1. FIFO initially empty.
2. Shift out held high.

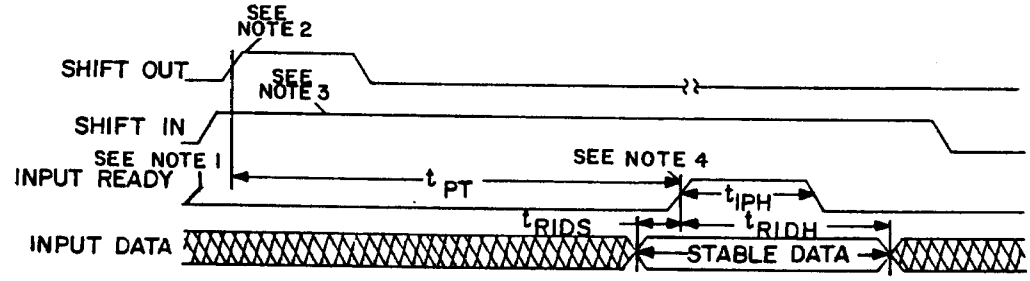
FIGURE 5. t_{PT} and t_{OPH} specifications.

Device types 01 - 08



NOTES:
1. FIFO is initially full.
2. Shift out pulse is applied. An empty location starts "bubbling" to the front.
3. Shift in is held high.
4. As soon as input ready becomes high, the input data is loaded into the first word.
5. The data from the first word is released for "fall through" to second word.

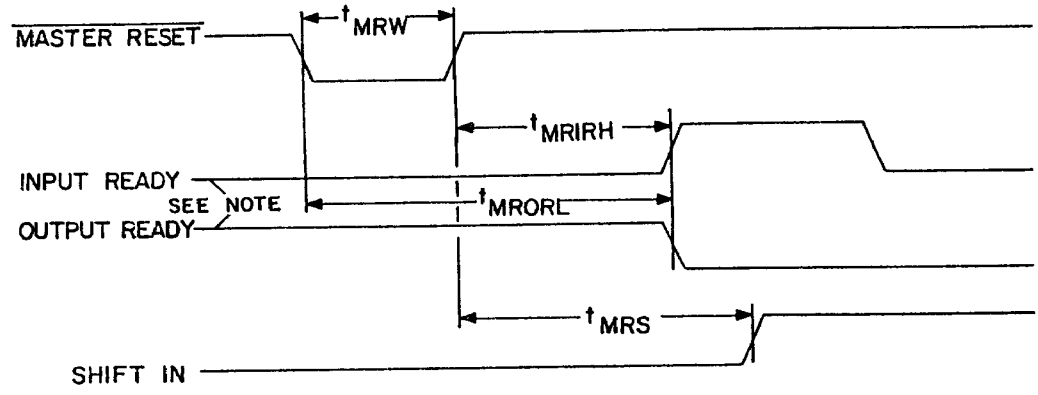
Device types 09, 10, and 11



NOTES:
1. FIFO is initially full.
2. Shift out pulse is applied. An empty location starts "bubbling" to the front.
3. Shift in is held high.
4. As soon as input ready becomes high, the input data is loaded into the first word.

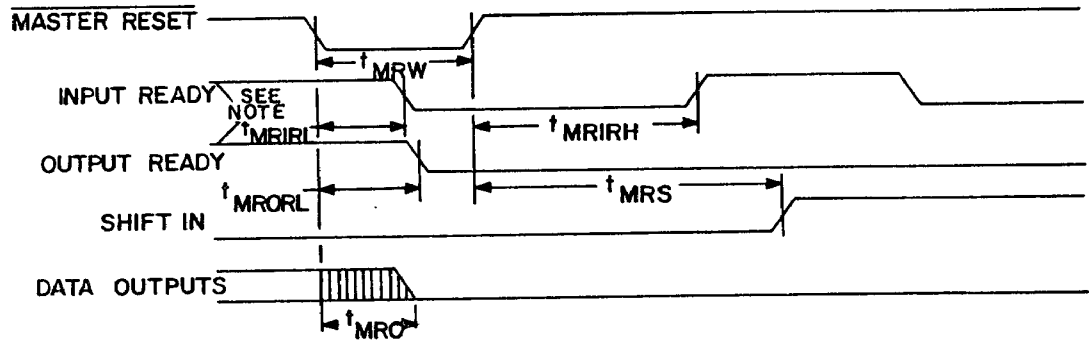
FIGURE 6. t_{PT} and t_{IPH} specifications.

Device types 01 - 08



NOTE: FIFO initially full.

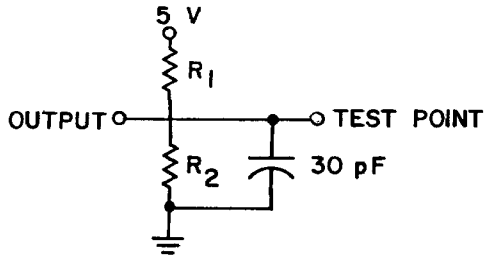
Device types 09, 10, and 11



NOTE: FIFO initially partially full.

FIGURE 7. Master reset timing.

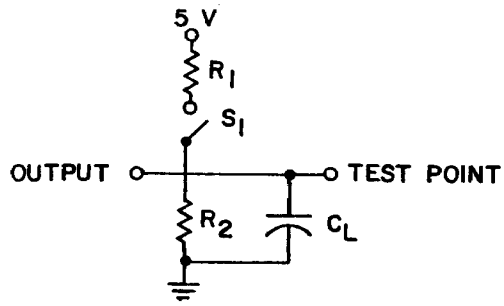
Device types 01 - 10



Device	I_{OL}	R_1	R_2
01 - 08	8 mA	560	1.1 k
09, 10	12 mA	390	760
	8 mA	600	1.2 k

Device type 11

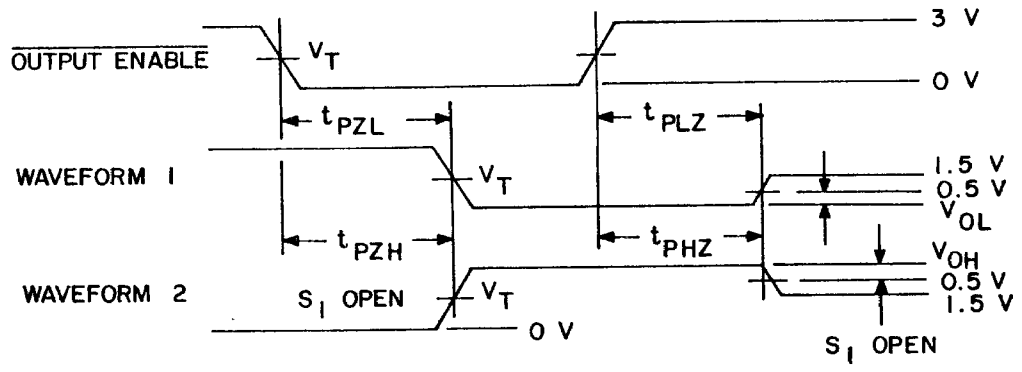
Device	I_{OL}	R_1	R_2
11	12 mA	390	760
	8 mA	600	1.2 k



EQUIVALENT TEST CIRCUIT

NOTES:
1. t_{PZL} and t_{PZH} measured at 1.5 V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.
2. t_{PHZ} and t_{PLZ} are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test measured at V_{OH} -0.5 V output level; S_1 is closed for "0" test to high impedance test measured at V_{OL} +0.5 V output level.
3. Input pulse amplitude 0 to 3 V.
4. Input rise and fall time (10 percent to 90 percent) = 5 ns.
5. Measurements made at 1.5 V.

FIGURE 8. Test loads.



NOTES:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 9. Enable and disable (device type 11 only).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8

*PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8779101EX	50364	57401J/883B	
5962-87791012X	50364	57401L/883B	
5962-8779102VX	50364	57402J/883B	
5962-87791022X	50364	57402L/883B	
5962-8779103EX	50364	57401AJ/883B	
5962-87791032X	50364	57401AL/883B	
5962-8779104VX	50364	57402AJ/883B	
5962-87791042X	50364	57402AL/883B	
5962-8779105EX	50364	C57401J/883B	
5962-87791052X	50364	C57401L/883B	
5962-8779106VX	50364	C57402J/883B	
5962-87791062X	50364	C57402L/883B	
5962-8779107EX	50364	C57401AJ/883B	
5962-87791072X	50364	C57401AL/883B	
5962-8779108VX	50364	C57402AJ/883B	
5962-87791082X	50364	C57402AL/883B	
5962-8779109EX	2/	57L401DJ/883B	
5962-8779110VX	2/	57L402DJ/883B	
5962-8779111EX	2/	57L4013DJ/883B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
50364	Monolithic Memories, Incorporated 2175 Mission College Boulevard Santa Clara, CA 95054-1592

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