REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline 3. Change conditions for Supply Current test I_{EE}. Editorial changes throughout.	92/01/17	M. A. Frye

REV																			
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SHEET																			

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
88/08/30

REVISION LEVEL A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 12-BIT VOLTAGE OUTPUT D/A CONVERTER, MICROPROCESSOR COMPATIBLE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88659
A	67268	

SHEET 1

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5962-E1625

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD667	12-bit voltage output D/A converter, microprocessor compatible

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

V_{CC} to power ground range	0 V dc to +18 V dc
V_{EE} to power ground range	0 V dc to -18 V dc
Digital inputs (pins 11-15, 17-28) to power ground range	-1.0 V dc to 7.0 V dc
Reference in to reference ground	±12 V dc
Bipolar offset to reference ground	±12 V dc
10 V span R to reference ground	±12 V dc
20 V span R to reference ground	±24 V dc
Reference out, V_{OUT} (pins 6 and 9)	Continuous short to power ground, momentary short to V_{CC}
Power dissipation (P_D)	1,000 mW 1/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case outline X	60°C/W
Case outline 3	125°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+11.4 V dc to +16.5 V dc
Supply voltage range (V_{EE})	-11.4 V dc to -16.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 4.

3.2.5 Test circuit for 20 V FSR. The test circuit for 20 V FSR shall be as specified on figure 5.

3.2.6 Test circuit for 10 V FSR. The test circuit for 10 V FSR shall be as specified on figure 6.

3.2.7 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ (unless otherwise specified)	Group A sub-groups	Limits		Unit
				Min	Max	
Resolution	RES			12		Bits
Integral linearity error	LE	2/	1	-0.5	+0.5	LSB
			2, 3	-0.75	+0.75	
Differential linearity error	DLE	3/	1	-0.75	+0.75	
			2, 3	-1	+1	
Gain error	A_E	All bits high	1	-0.2	+0.2	% of FSR
Gain drift 4/	$\Delta A_E/\Delta T$		2, 3	-30	+30	ppm of FSR/°C
Unipolar offset error	V_{OS}	All bits low	1	-2	+2	LSB
Unipolar offset drift 4/	$\Delta V_{OS}/\Delta T$		2, 3	-3	+3	ppm of FSR/°C
Bipolar zero error 5/	B_{PZE}	MSB high, all other bits low	1	-0.1	+0.1	% of FSR
Bipolar zero drift 4/ 5/	$\Delta B_{PZE}/\Delta T$		2, 3	-10	+10	ppm of FSR/°C
Reference voltage	V_{REF}	V_{CC} = +11.4 V, V_{EE} = -11.4 V 6/	1, 2, 3	9.9	10.1	V
Latch functionality	$V_{OS\Delta}$	7/	1, 2, 3	-1	+1	LSB
	$A_{E\Delta}$	7/ 8/	1, 2, 3	-1	+1	
Output current	I_{OUT}	T_A = +25°C 9/	1	-5	+5	mA
Output short circuit current	I_{OS}	T_A = +25°C 9/	1		40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ (unless otherwise specified)		Group A subgroups	Limits Min	Limits Max	Unit
Power supply rejection ratio	PSSR+	$+11.4\ V \le V_{CC} \le +16.5\ V$, All bits high, $T_A = +25°C$		1	-10	+10	ppm of FS/%
	PSSR-	$-16.5\ V \le V_{EE} \le -11.4\ V$, All bits high, $T_A = +25°C$		1	-10	+10	
Power supply current	I_{CC}	$V_{CC} = +16.5\ V$, $V_{EE} = -16.5\ V$, $T_A = +25°C$	All bits high	1		12	mA
	I_{EE}		All bits low		-25		
Digital input high voltage	V_{IH}	$T_A = +25°C$		1	2.0		V
Digital input low voltage	V_{IL}			1		0.8	
				2, 3		0.7	
Digital input high current	I_{IH}	$T_A = +25°C$, $V_{IH} = 5.5\ V$		1		10	µA
Digital input low current	I_{IL}	$T_A = +25°C$, $V_{IL} = 0\ V$				5	
Functional tests		See 4.3.1c		7, 8			
Output voltage settling time	t_{SL}	See figure 4, $T_A = +25°C$ 9/, $R_L = 2\ k\Omega$, $C_L = 500\ pF$	See figure 5, 20 V FSR	9		4	µs
			See figure 6, 10 V FSR			3	
$\overline{CS}$ pulse width	t_{CP}	See figure 4, $T_A = +25°C$ 9/			100		ns
Data setup time	t_{DC}				50		
Data hold time	t_{DH}				0		
Address valid to end of $\overline{CS}$	t_{AC}				100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ V_{CC} = +15 V dc, V_{EE} = -15 V dc, $\overline{CS}$, A0, A1, A2, A3 = LOGIC "0", V_{IH} = 2.0 V, V_{IL} = 0.8 V, 50Ω resistor pin 6 to pin 7. Unipolar configuration (pins 1 and 2 to pin 9, pin 4 to pin 5, unless otherwise specified).

2/ All bits with positive errors on. All bits with negative errors on.

3/ Major carry transitions.

4/ $\Delta V_{OS}/\Delta t$, $\Delta A_E/\Delta t$, $\Delta B_{PZE}/\Delta t$ are determined for measurements made at +125°C, +25°C, and -55°C for V_{OS}, A_E, and B_{PZE} respectively. Drift is specified from +25°C to +125°C and from +25°C to -55°C.

5/ Bipolar configuration (pins 1 to 9, 50Ω resistor pin 4 to pin 6).

6/ In subgroup 1, the reference output is loaded with 0.5 mA nominal reference current, 1.0 mA bipolar offset current and 0.1 mA additional current. In subgroups 2 and 3, only the 0.5 mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperatures.

7/ All bits low, A0, A1, A2, A3 are logic "0"; A0, A1, A2, A3 are initialized to logic "1", each 4-bit register set to logic "1", and A0, A1, A2 are set sequentially to logic "0" and back to logic "1" to latch data into first rank.

8/ A3 is set to logic "0" and back to logic "1" to latch full scale output into second rank.

9/ Guaranteed, if not tested, to the limits specified.

Case outline X

Case outline X

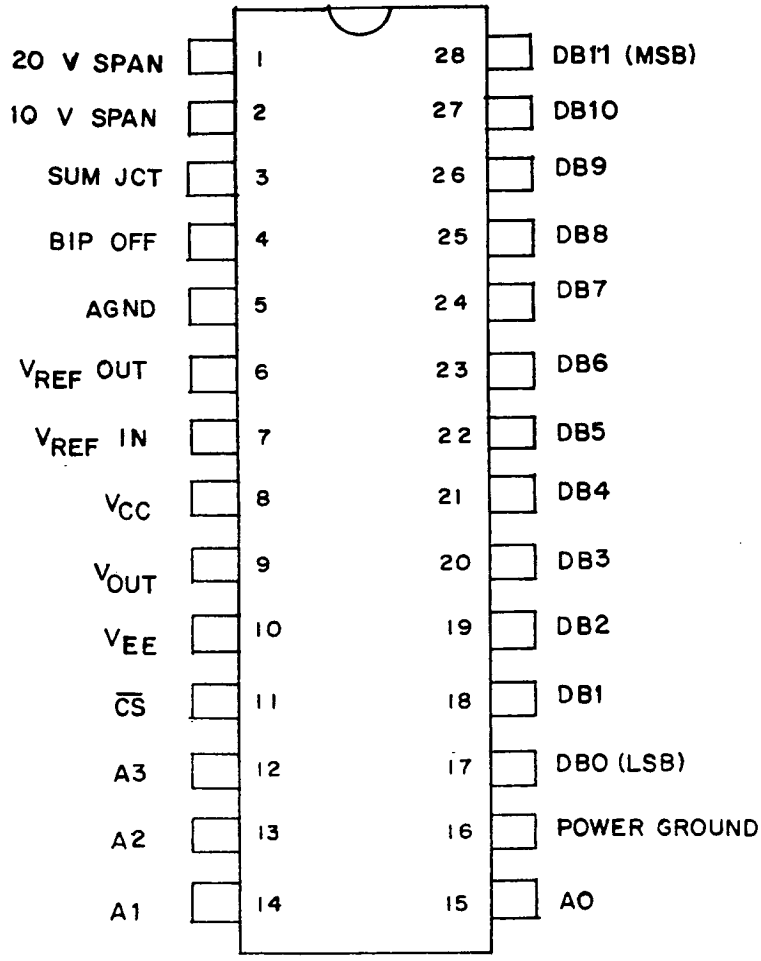

FIGURE 1. Terminal connections.

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Case outline 3

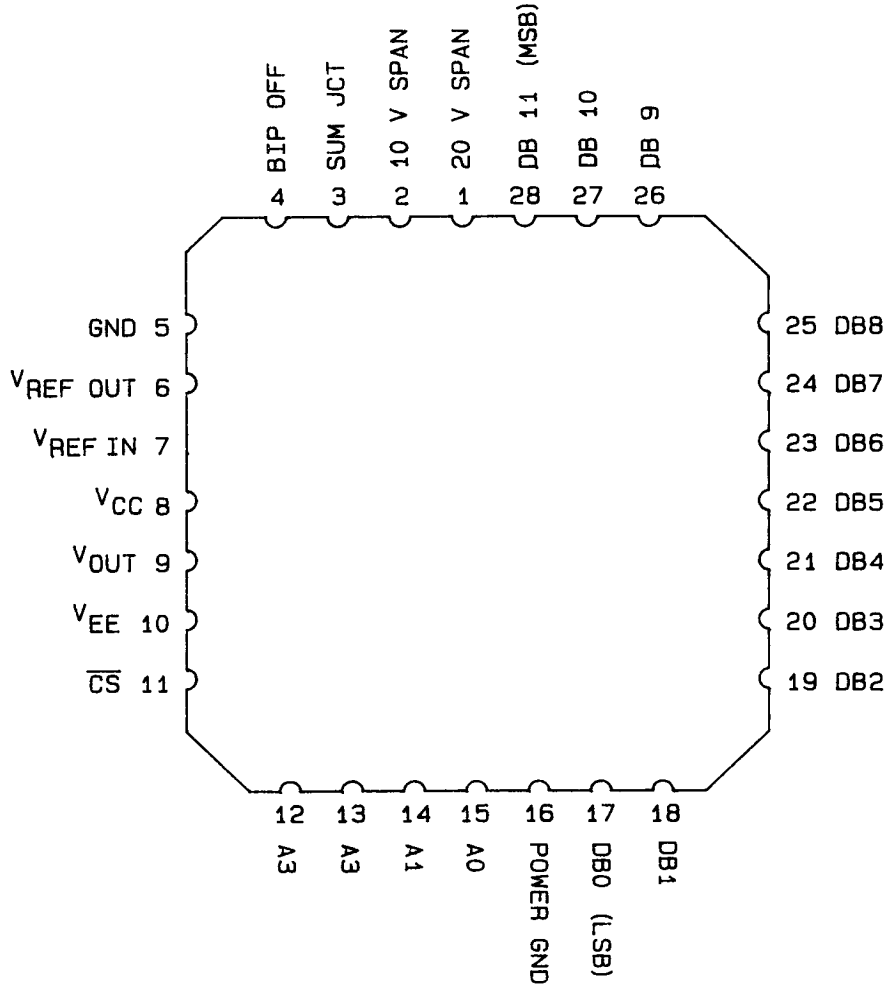

FIGURE 1. Terminal connections - Continued.

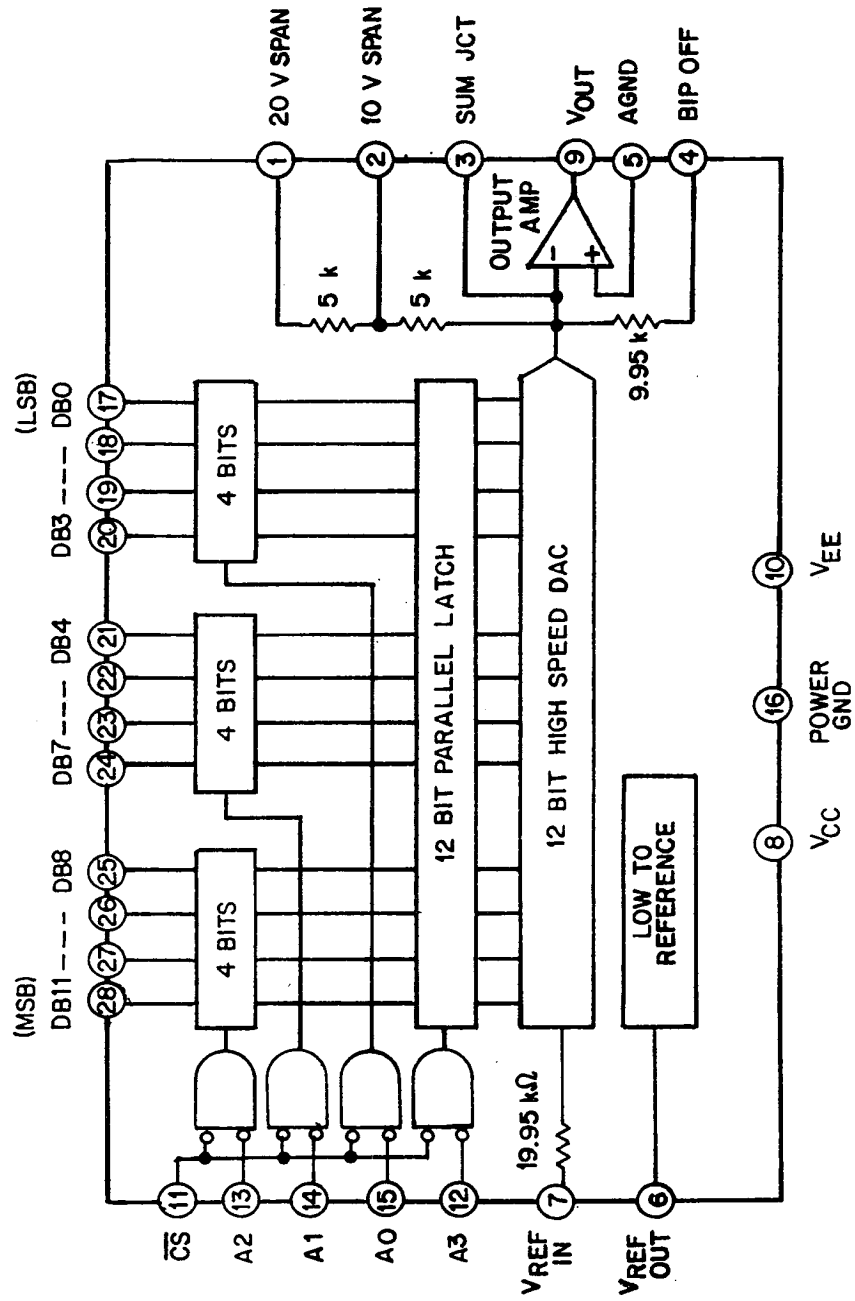

FIGURE 2. Block diagram.

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$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No operation
X	1	1	1	1	No operation
0	1	1	1	0	Enable 4 LSBs of first rank
0	1	1	0	1	Enable 4 middle bits of first rank
0	1	0	1	1	Enable 4 MSBs of first rank
0	0	1	1	1	Loads second rank from first rank
0	0	0	0	0	All latches transparent

"X" = Don't care.

FIGURE 3. Truth table.

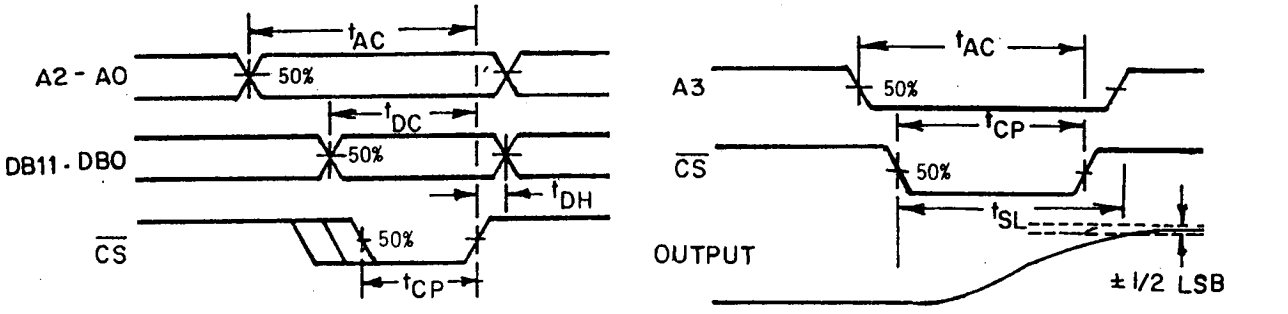
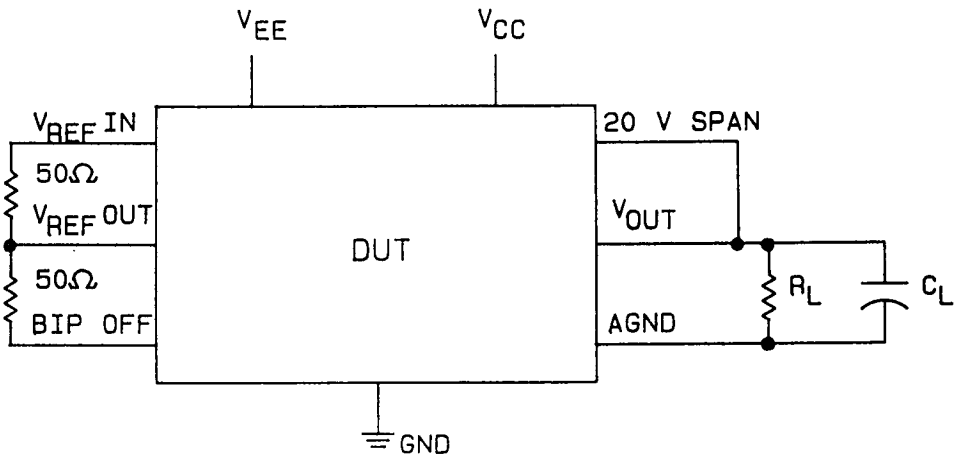
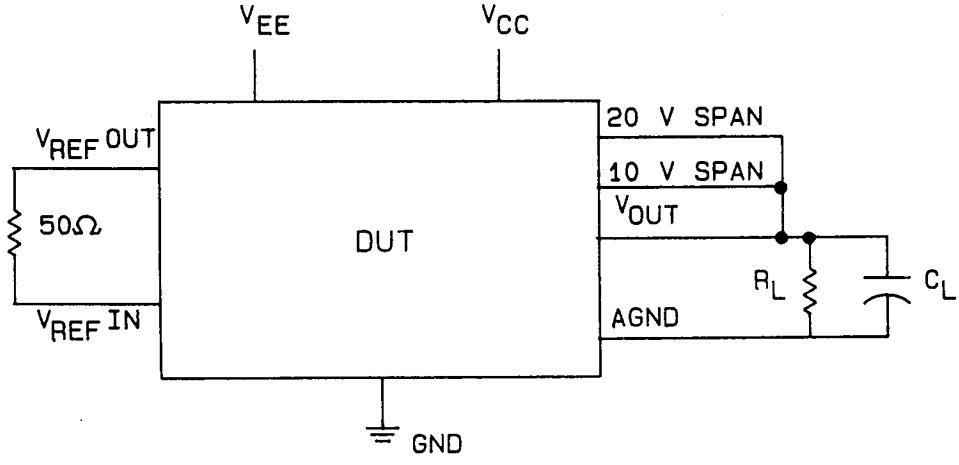


FIGURE 4. Timing diagram.



NOTE: ±10 V bipolar voltage output.

FIGURE 5. Test circuit for 20 V FSR.



NOTE: 0 V to +10 V unipolar voltage output.

FIGURE 6. Test circuit for 10 V FSR.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroup 9, if not tested, shall be guaranteed to the limits specified in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.