| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Updated boilerplate. Added device types 05 - 08. Editorial changes throughout. | 94-04-29 | M. A. Frye |

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | A | A | | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV STATUS OF SHEETS | REV | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Ken Rice

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
23 August 1989

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

# MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 64 X 4 PARALLEL FIFO, MONOLITHIC SILICON

| SIZE | CAGE CODE | 5962-89523 |
|---|---|---|
| A | 67268 | |

SHEET 1 OF 16

DESC FORM 193
JUL 91

5962-E240-94

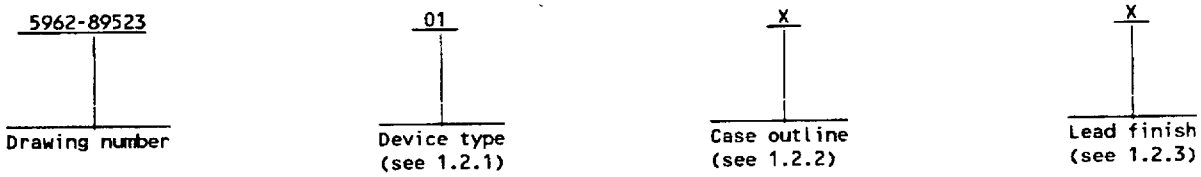
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0001312 963

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:




1.2.1 Device type. The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function | Shift in/out rate |
|---|---|---|---|
| 01,05 | (See 6.6) | 64 x 5 CMOS parallel FIFO | 10 MHz |
| 02,06 | (See 6.6) | 64 x 5 CMOS parallel FIFO | 15 MHz |
| 03,07 | (See 6.6) | 64 x 5 CMOS parallel FIFO | 25 MHz |
| 04,08 | (See 6.6) | 64 x 5 CMOS parallel FIFO | 35 MHz |

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line package |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

| | |
|---|---|
| Terminal voltage with respect to ground | -0.5 V dc to +7.0 V dc |
| DC output current | 50 mA |
| Storage temperature range | -65°C to +150°C |
| Maximum power dissipation ($P_D$) 1/ | 1.0 W |
| Lead temperature (soldering, 10 seconds) | +260°C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) | +175°C |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage ($V_{CC}$) | 4.5 V dc to 5.5 V dc |
| Supply voltage (GND) | 0 V dc |
| Input high voltage ($V_{IH}$) | 2.0 V dc minimum |
| Input low voltage ($V_{IL}$) | 0.8 V dc maximum 2/ |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1/ Must withstand the added $P_D$ due to short-circuit, test e.g., $I_{OS}$.
2/ -1.5 V undershoots are allowed for 10 ns once per cycle.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{CC}$ = 4.5 V to 5.5 V<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input low current | $I_{IL}$ | $0 V \le V_{IN} \le 5.5 V$, $V_{CC}$ = 5.5 V | 1, 2, 3 | All | -10 | | µA |
| Input high current | $I_{IH}$ | $0 V \le V_{IN} \le 5.5 V$, $V_{CC}$ = 5.5 V | 1, 2, 3 | All | | +10 | µA |
| Output low voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $I_{OL}$ = 8.0 mA<br>$V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 1, 2, 3 | All | | 0.4 | V |
| Output high voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V, $I_{OH}$ = -4.0 mA<br>$V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 1, 2, 3 | All | 2.4 | | V |
| Output short-circuit current 1/ | $I_{OS}$ | $V_{CC}$ = 5.5 V, $V_O$ = 0 V | 1, 2, 3 | All | -20 | -110 | mA |
| Off-state output high current | $I_{HZ}$ | $V_{CC}$ = 5.5 V, $V_O$ = 2.4 V | 1, 2, 3 | All | | +20 | µA |
| Off-state output low current | $I_{LZ}$ | $V_{CC}$ = 5.5 V, $V_O$ = 0.4 V | 1, 2, 3 | All | -20 | | µA |
| Operating supply current | $I_{CC}$ | outputs open, f = 10 MHz,<br>$V_{CC}$ = 5.5 V,<br>all inputs 0.0 V to 3.0 V | 1, 2, 3 | All | | 90 | mA |
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V, f = 1.0 MHz,<br>$T_A$ = +25°C, see 4.3.1c | 4 | All | | 7.0 | pF |
| Output capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V, f = 1.0 MHz,<br>$T_A$ = +25°C, see 4.3.1c | 4 | All | | 7.0 | pF |
| Functional tests | | See 4.3.1d | 7, 8A, 8B | All | | | |
| Shift in rate | $f_{IN}$ | See figures 2 - 8 as applicable 2/ | 9, 10, 11 | 01, 05 | | 10 | MHz |
| | | | | 02, 06 | | 15 | |
| | | | | 03, 07 | | 25 | |
| | | | | 04, 08 | | 35 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $V_{CC}$ = 4.5 V to 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Shift in to input ready low 3/ | $t_{IRL}$ | See figures 2 - 8 as applicable 2/ | 9, 10, 11 | 01, 05 | | 40 | ns |
| | | | | 02, 06 | | 35 | |
| | | | | 03, 07 | | 21 | |
| | | | | 04, 08 | | 18 | |
| Shift in to input ready high 3/ | $t_{IRH}$ | | 9, 10, 11 | 01, 05 | | 45 | ns |
| | | | | 02, 06 | | 40 | |
| | | | | 03, 07 | | 28 | |
| | | | | 04, 08 | | 20 | |
| Shift out rate | $f_{OUT}$ | | 9, 10, 11 | 01, 05 | | 10 | MHz |
| | | | | 02, 06 | | 15 | |
| | | | | 03, 07 | | 25 | |
| | | | | 04, 08 | | 35 | |
| Shift out to output ready low 3/ | $t_{ORL}$ | | 9, 10, 11 | 01, 05 | | 40 | ns |
| | | | | 02, 06 | | 35 | |
| | | | | 03, 07 | | 19 | |
| | | | | 04, 08 | | 18 | |
| Shift out to output ready high 3/ | $t_{ORH}$ | | 9, 10, 11 | 01, 05 | | 55 | ns |
| | | | | 02, 06 | | 40 | |
| | | | | 03, 07 | | 34 | |
| | | | | 04, 08 | | 20 | |
| Output data hold (previous word) | $t_{ODH}$ | | 9, 10, 11 | All | 5.0 | | ns |
| Output data shift (next word) 4/ | $t_{ODS}$ | | 9, 10, 11 | 01, 02, 05, 06 | | 55 | ns |
| | | | | 03, 07 | | 35 | |
| | | | | 04, 08 | | 25 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $V_{CC}$ = 4.5 V to 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits Min | Limits Max | Unit |
|---|---|---|---|---|---|---|---|
| Data throughput or "fall through" 4/ | $t_{PT}$ | See figures 2 - 8 as applicable 2/ | 9, 10, 11 | 01, 02, 05, 06 | | 65 | ns |
| | | | | 03, 07 | | 40 | |
| | | | | 04, 08 | | 28 | |
| $\overline{\text{MASTER RESET}}$ to OR low | $t_{MRORL}$ | | 9, 10, 11 | 01, 05 | | 40 | ns |
| | | | | 02, 03, 06, 07 | | 35 | |
| | | | | 04, 08 | | 28 | |
| $\overline{\text{MASTER RESET}}$ to IR high | $t_{MRIRH}$ | | 9, 10, 11 | 01, 05 | | 40 | ns |
| | | | | 02, 03, 06, 07 | | 35 | |
| | | | | 04, 08 | | 28 | |
| $\overline{\text{MASTER RESET}}$ to data output low | $t_{MRQ}$ | | 9, 10, 11 | 01, 05 | | 40 | ns |
| | | | | 02, 06 | | 35 | |
| | | | | 03, 07 | | 25 | |
| | | | | 04, 08 | | 20 | |
| Output valid from $\overline{OE}$ low | $t_{OOE}$ | | 9, 10, 11 | 01 | | 35 | ns |
| | | | | 02 | | 30 | |
| | | | | 03 | | 20 | |
| | | | | 04 | | 15 | |
| Input ready pulse high 4/ 5/ | $t_{IPH}$ | | 9, 10, 11 | 01,02,03, 05,06,07 | 11 | | ns |
| | | | | 04, 08 | 9.0 | | |
| Output high impedance from $\overline{OE}$ high 4/ 5/ | $t_{HZOE}$ | | 9, 10, 11 | 01 | | 30 | ns |
| | | | | 02 | | 25 | |
| | | | | 03 | | 15 | |
| | | | | 04 | | 12 | |
| Output ready pulse high 4/ 5/ | $t_{OPH}$ | | 9, 10, 11 | 01,02,03, 05,06,07 | 11 | | ns |
| | | | | 04, 08 | 9.0 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$V_{CC}$ = 4.5 V to 5.5 V<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Shift in high time 3/ | $t_{SIH}$ | See figures 2 - 8 as applicable 2/ | 9, 10, 11 | 01, 02<br>05, 06 | 20 | | ns |
| | | | | 03, 07 | 11 | | |
| | | | | 04, 08 | 9.0 | | |
| Shift in low time | $t_{SIL}$ | | 9, 10, 11 | 01, 05 | 30 | | ns |
| | | | | 02, 06 | 25 | | |
| | | | | 03, 07 | 24 | | |
| | | | | 04, 08 | 17 | | |
| Input data setup time | $t_{IDS}$ | | 9, 10, 11 | All | 0 | | ns |
| Input data hold time | $t_{IDH}$ | | 9, 10, 11 | 01, 05 | 40 | | ns |
| | | | | 02, 06 | 30 | | |
| | | | | 03, 07 | 20 | | |
| | | | | 04, 08 | 15 | | |
| Shift out high time 3/ | $t_{SOH}$ | | 9, 10, 11 | 01, 02<br>05, 06 | 20 | | ns |
| | | | | 03, 07 | 11 | | |
| | | | | 04, 08 | 9.0 | | |
| Shift out low time | $t_{SOL}$ | | 9, 10, 11 | 01, 02<br>05, 06 | 25 | | ns |
| | | | | 03, 07 | 24 | | |
| | | | | 04, 08 | 17 | | |
| $\overline{\text{MASTER}}$ $\overline{\text{RESET}}$ pulse width | $t_{MRW}$ | | 9, 10, 11 | 01, 05 | 30 | | ns |
| | | | | 02,03,04<br>06,07,08 | 25 | | |
| $\overline{\text{MASTER}}$ $\overline{\text{RESET}}$ pulse to SI | $t_{MRS}$ | | 9, 10, 11 | 01, 05 | 35 | | ns |
| | | | | 02, 06 | 25 | | |
| | | | | 03, 04<br>07, 08 | 10 | | |

TABLE I. Electrical performance characteristics - Continued.

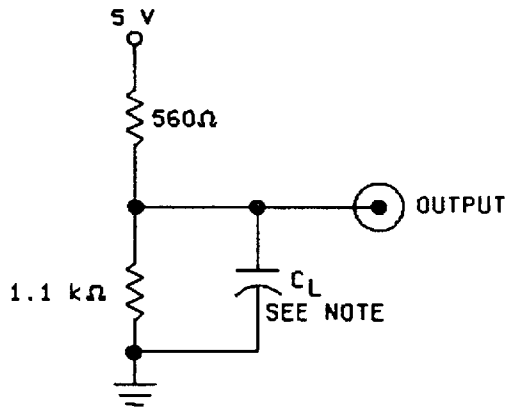
| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$ $V_{CC}$ = 4.5 V to 5.5 V unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Data setup to IR 5/ | $t_{SIR}$ | See figures 2 - 8 as applicable 2/ | 9, 10, 11 | 01,02,03 05,06,07 | 5.0 | | ns |
| | | | | 04, 08 | 3.0 | | |
| Data hold from IR 5/ | $t_{HIR}$ | | 9, 10, 11 | 01, 02 05, 06 | 30 | | ns |
| | | | | 03, 07 | 20 | | |
| | | | | 04, 08 | 15 | | |
| Data setup to OR high 5/ | $t_{SOR}$ | | 9, 10, 11 | All | 0 | | ns |

1/ Not more than one output should be shorted at a time. Duration of the short-circuit condition should not exceed one second. This parameter may not be tested, but shall be guaranteed to the limits specified in table I.
2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance. Output timing reference is 1.5 V.
3/ Since these devices are very high speed, care must be exercised in the design of the hardware and timing utilized in the design. Device grounding and decoupling are crucial to correct operation as the device will respond to very small glitches due to long reflective lines, high capacitances or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1 $\mu$F directly between $V_{CC}$ and GND with very short lead lengths is recommended.
4/ This parameter applies to devices communicating with each other in a cascaded mode.
5/ May not be tested, but shall be guaranteed to the limits specified in table I.

| Device types | All | |
|---|---|---|
| Case outlines | E | 2 |
| Terminal number | Terminal symbol | |
| 1 | $\overline{OE}$/NC 1/ | $\overline{OE}$/NC 1/ |
| 2 | IR | IR |
| 3 | SI | NC |
| 4 | $D_0$ | SI |
| 5 | $D_1$ | $D_0$ |
| 6 | $D_2$ | $D_1$ |
| 7 | $D_3$ | $D_2$ |
| 8 | GND | NC |
| 9 | MR | $D_3$ |
| 10 | $Q_3$ | GND |
| 11 | $Q_2$ | MR |
| 12 | $Q_1$ | $Q_3$ |
| 13 | $Q_0$ | NC |
| 14 | OR | $Q_2$ |
| 15 | SO | $Q_1$ |
| 16 | $V_{CC}$ | $Q_0$ |
| 17 | --- | OR |
| 18 | --- | NC |
| 19 | --- | SO |
| 20 | --- | $V_{CC}$ |

1/ For device types 05 - 08, $\overline{OE}$ will be replaced by NC.

FIGURE 1. Terminal connections.




NOTE: $C_L$ = 30 pF and includes jig and scope capacitance.

FIGURE 2. Output load circuit.

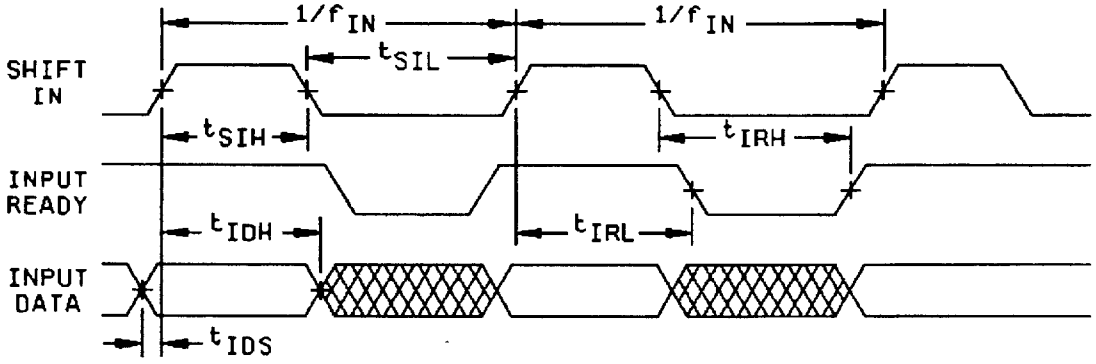
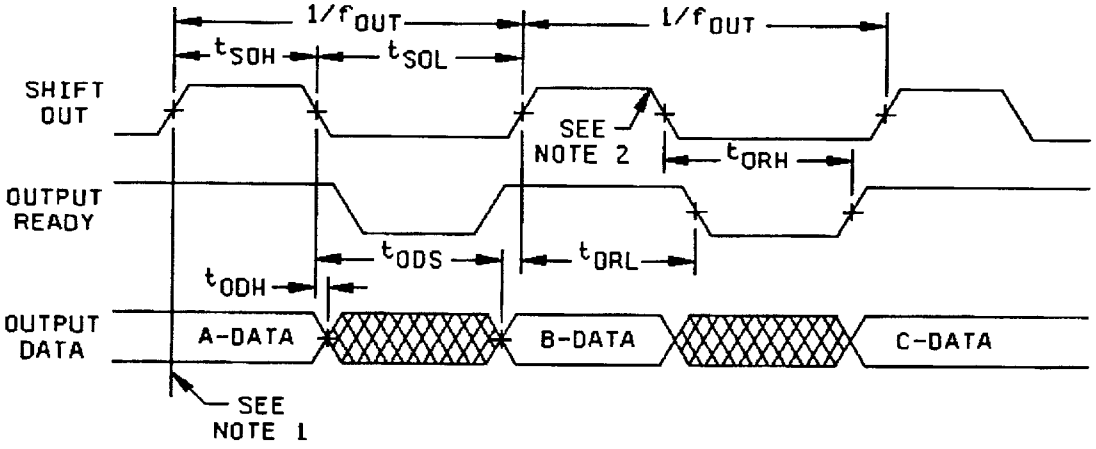
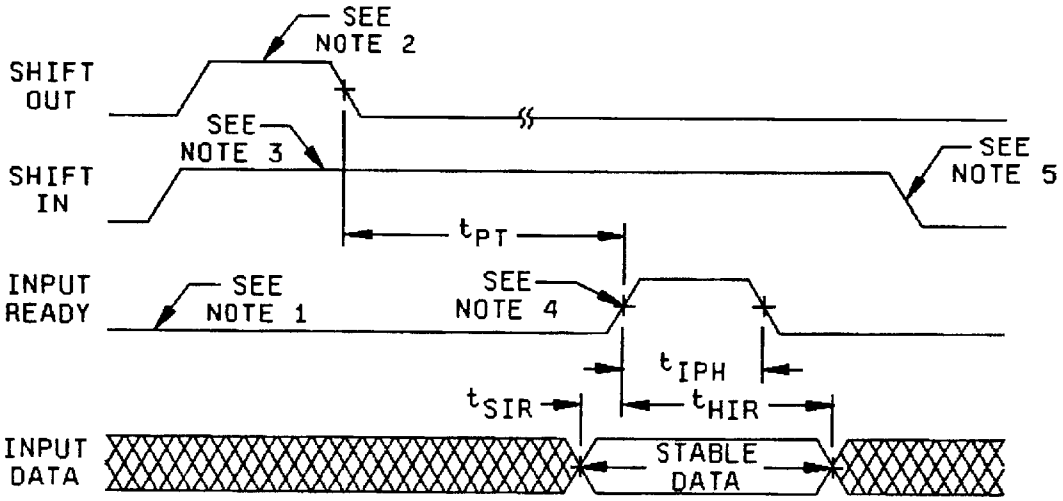



FIGURE 3. Input timing diagram.



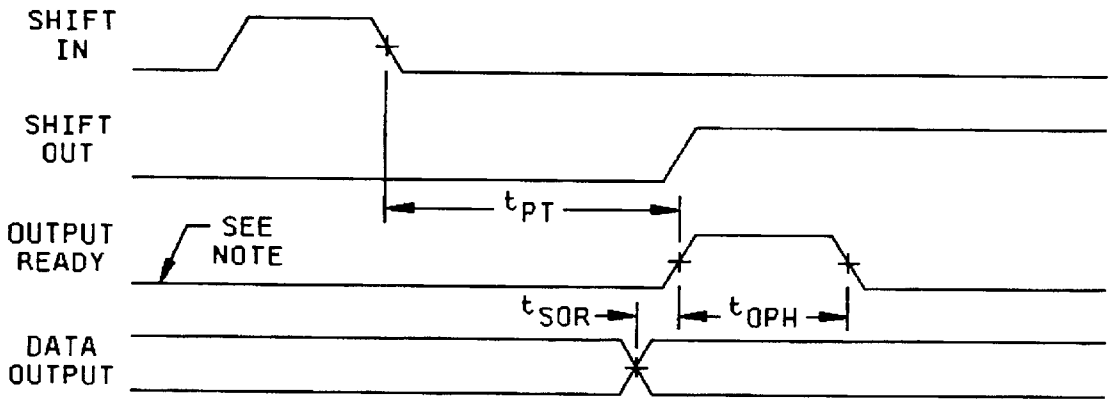

NOTES:
1. This data is loaded consecutively, A, B, C.
2. Data is shifted out when SHIFT OUT makes a high to low transition.

FIGURE 4. Output timing diagram.



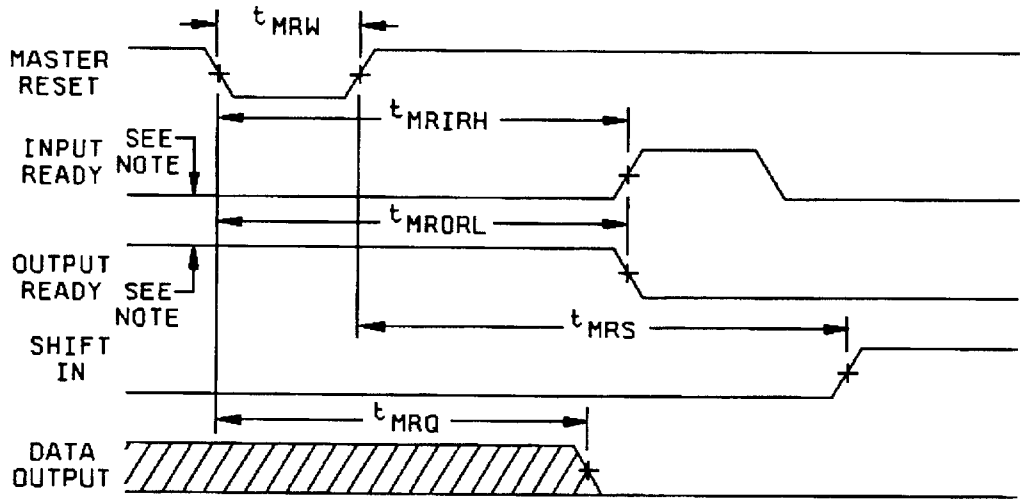

NOTES:
1. FIFO is initially full.
2. SHIFT OUT pulse is applied.
3. SHIFT IN is held high.
4. As soon as input ready becomes high the input data is loaded into the FIFO.
5. The write pointer is incremented.

FIGURE 5. $t_{IPH}$, $t_{HIR}$, and $t_{SIR}$ timing diagram.



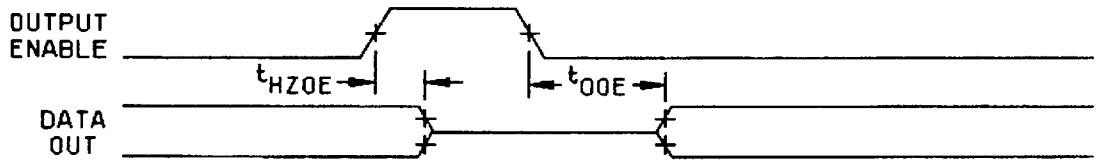

NOTE: FIFO initially empty.

FIGURE 6. $t_{PT}$ and $t_{OPH}$ timing diagram.




NOTE: Worst case, FIFO initially full.

FIGURE 7. $\overline{\text{MASTER RESET}}$ timing.




NOTE: High-Z transitions are referenced to the steady-state $V_{OH}$ - 500 mV and $V_{OL}$ + 500 mV levels on the output.

FIGURE 8. Output enable timing (device types 01-04 only).

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

| MIL-STD-883 test requirements | Subgroups (in accordance with method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | --- |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 4**, 7,8A, 8B, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3, 7, 8A, 8B |

1/ * Indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** See 4.3.1c.
4/ As a minimum, subgroups 7 and 8 shall consist of verifying the data pattern.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.