Control LED drive circuit

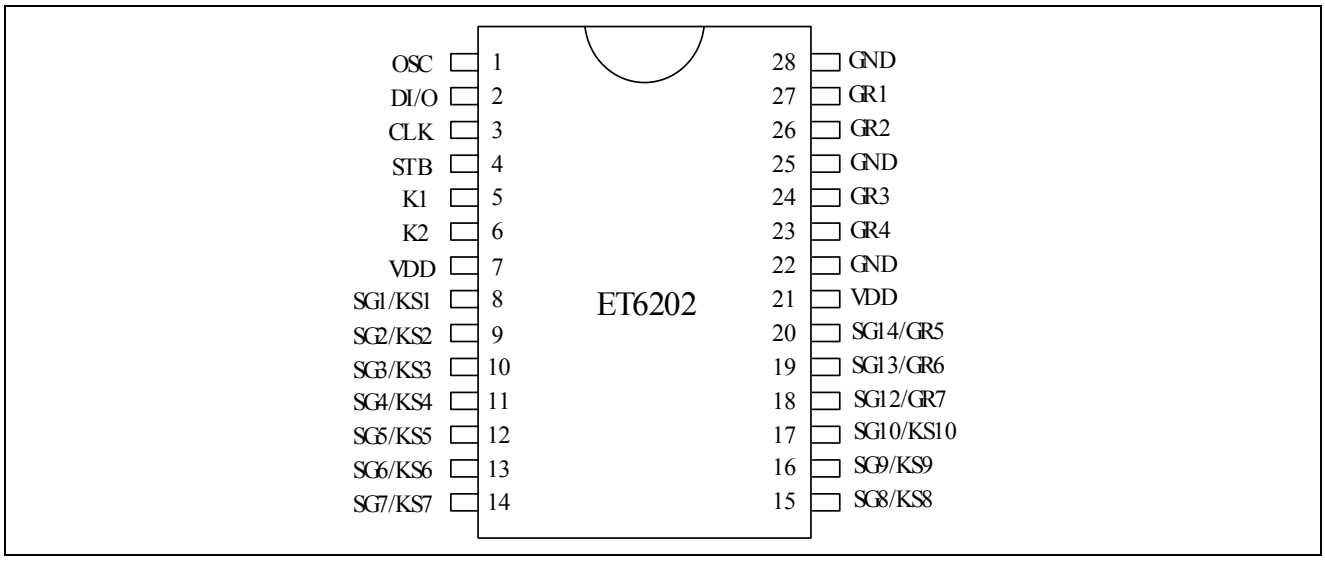
Overview

ET6202 is 1 / 7 to 1 / 8 duty cycle control of the LED display driver circuit. By paragraph 11 output, the output gate 6, paragraph 1 / output gate, A display memory, control circuit, key scan circuit composed of a single-chip high-reliability of the external LED driver circuit. Serial data 4-wire serial interface into the ET6202, the use of SOP28 package.

Features

- CMOS technology
- Low-power
- A variety of display modes: choice of settings, and the number of spaces (4 to 7, 10 to 13)
- Scan button: 10 × 2 matrix
- 8 levels of brightness adjustment circuit
- 4-wire serial interface
- Package for SOP28

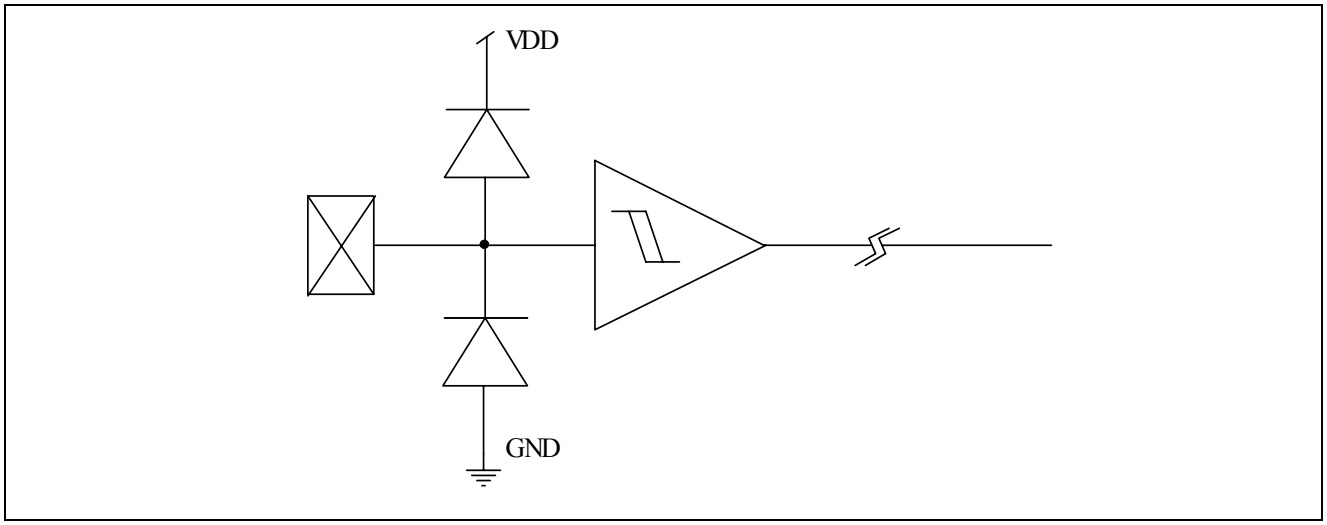
Pin assignment



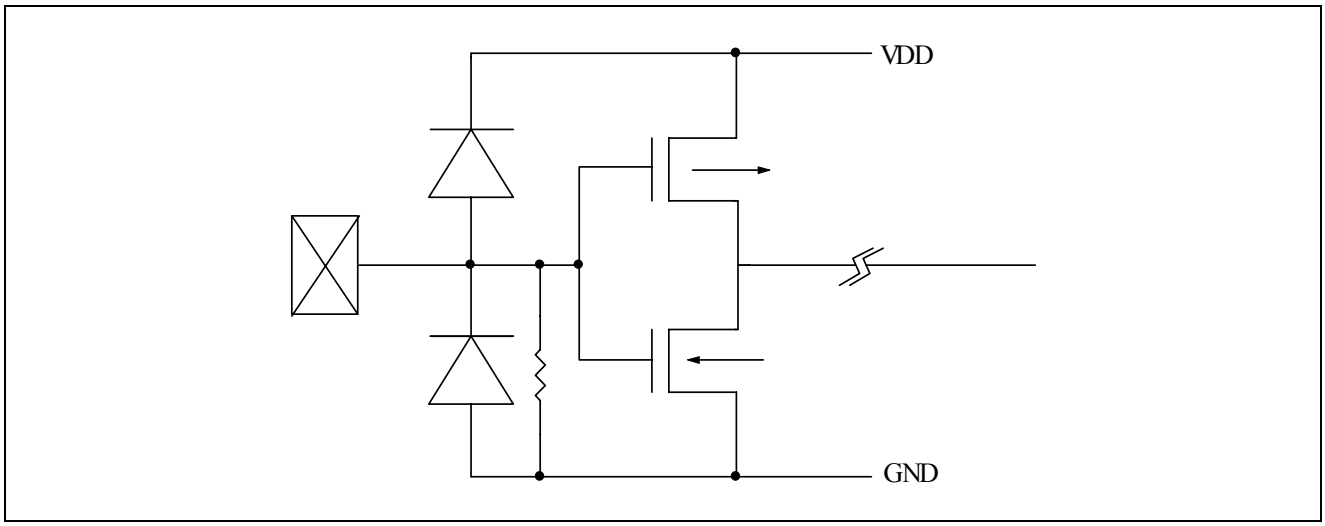
Pin Description

Number ET6202	Pin Name	I/O	Description of the function
1	OSC	I	Oscillation input port to connect a resistor to determine the oscillation frequency
2	DI/O	I/O	Data input and output ports (N-channel open drain), the clock in the serial data output falling, In the clock rising edge of the serial data input.
3	CLK	I	Clock input port, when read in the rising edge of the serial data, and in falling output when the number According to
4	STB	I	Serial interface filtering, falling in the STB input data as an order. (External pull-down power Resistance)
5，6	K1～K2	I	Key input data port, the port on the importation of these data show that there is locked at the end of the cycle End
22，25，28	GND	—	Grounding pin
8～17	SG1/KS1～SG10/KS10	O	Paragraph output port (P-channel open drain), can also be used as keys input scanning
18	SG12/GR7	O	Paragraph / output port gate
7，21	VDD	—	Power Supply
19，20，23 24，26，27	GR6～GR1	O	Gate output port

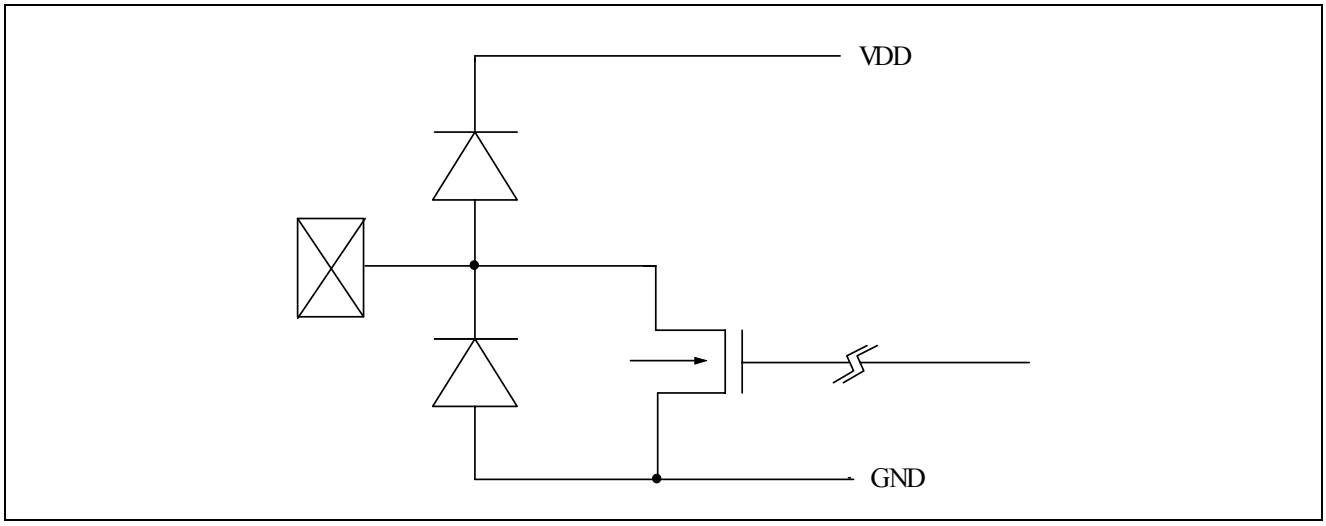
I / O configuration
The logical part of the I / O diagram below.
1. Input port: CLK, STB & DIN



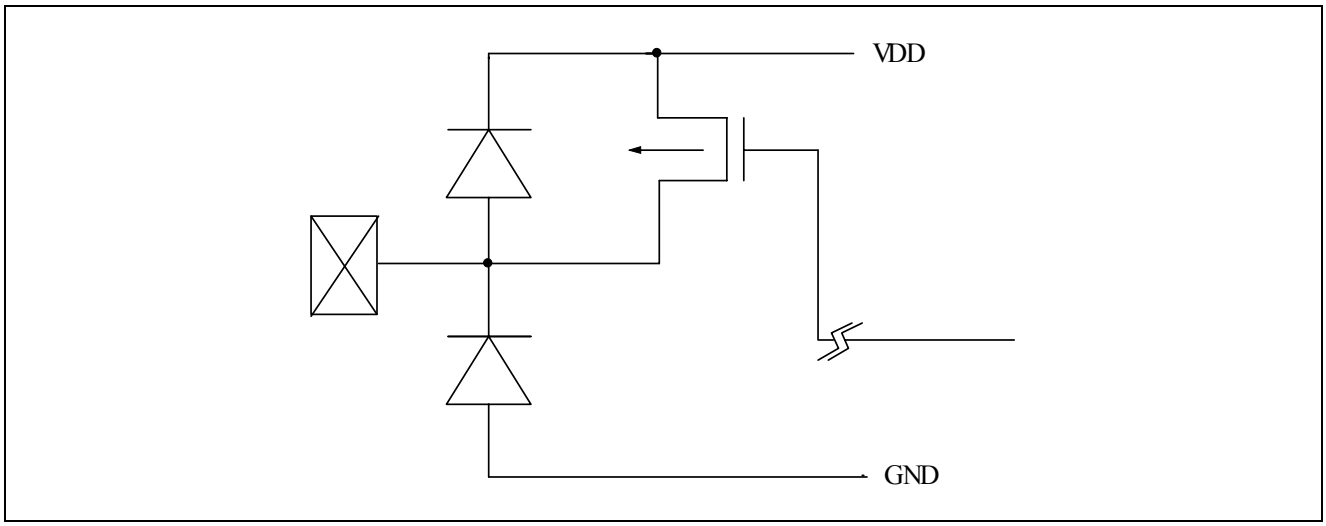
2. Input: K1 ~ K2



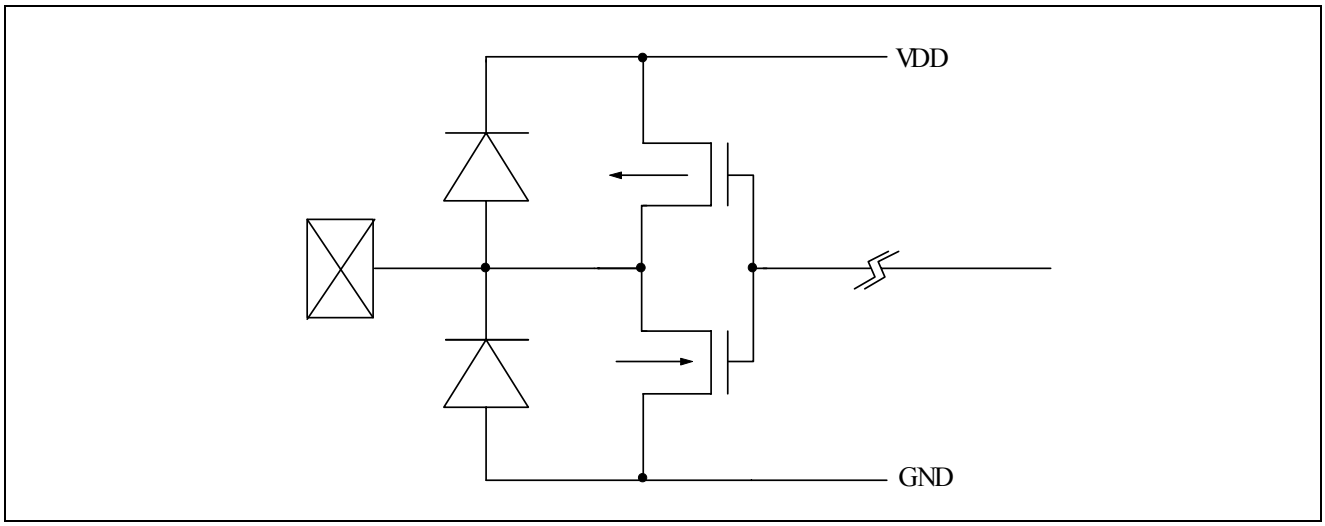
3. Output ports: DOUT, GR1 ~ GR4



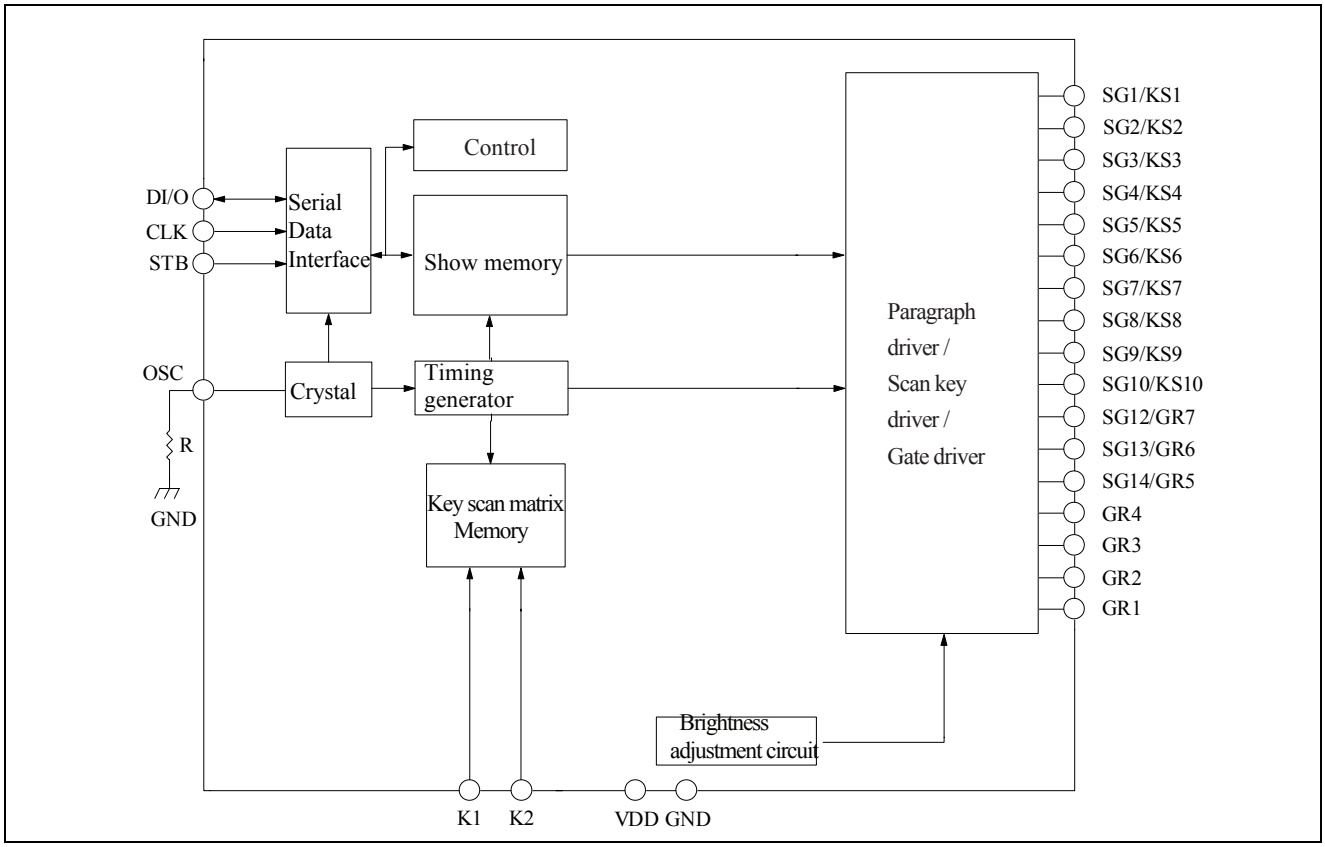
4. Outputs: SG1 ~ SG10



5. GR5,GR6 and SG12/GR7



Functional block diagram



Functions

Order

STB ports in the state by the high-low, the importation of an order by the DIN port of the first byte (b0 ~ b7). If the data or the order in the transmission For some reason, STB is set to port, serial communications are to be initialized, the data is input / command be considered invalid.

Order 1: display mode command set

ET6202 provides as follows two display modes: a command in the port of the STB by the state after the high-low by the DIN port to lose ET6202 into the first byte (b0 ~ b7). For these orders, the No. 3 to No. 6 (b2 ~ b5) are ignored, 7 and 8 (b6 ~ b7) 0. Display mode command set used by the decision, gate number (4 to 7, 10 to 13). Must show that an order to continue to make the show. If you choose the same mode settings, not to implement the order, so there will be no show. When the electric power, the choice of 10 × 7-bit mode.

MSB							**LSB**
0	0	—	—	—	—	b1	b0

b2 ~ b5 no assignment

Display mode:

b1 for 0, b0 to 0:13 paragraph × 4 bits

b1 for 0, b0 to 1:12 paragraph bit × 5

b1 for 1, b0 to 0:11 paragraph bit × 6

b1 for 1, b0 1:10 paragraph bit × 7

Order 2: Set the order data

Data set is the order of implementation of the ET6202 read and write data. The first order of 5 and 6 (b4, b5) are ignored, 8-bit (b7) 0, No. 7 (b6) is set to 1. When the electric power supply when the first 4 to a (b3 ~ b0) should be set to 0

MSB							**LSB**
0	1	—	—	b3	b2	b1	b0

b4, b5 non-assignment

Mode:

b3 0: normal mode of operation

b3 1: Test mode

Incremental mode address settings (mode):

b2 0: After the data into the Incremental address

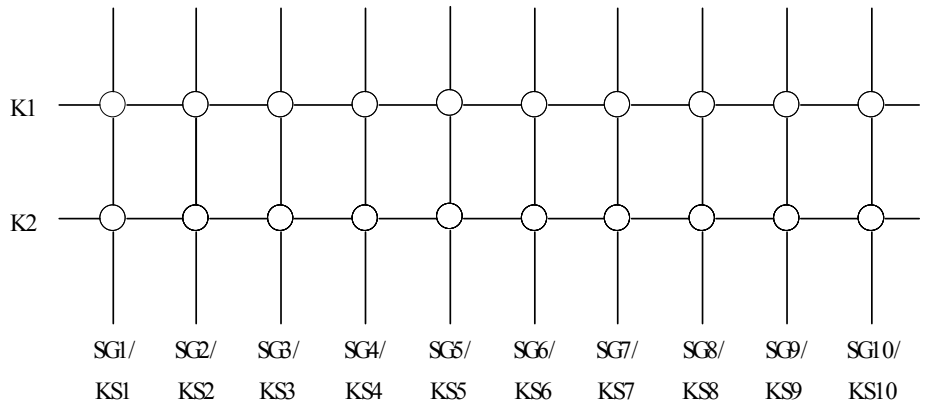
b2 1: Address the same

Read and write data mode:

b1 for 0, b0 0: write data to the display mode

b1 for 1, b0 0: Reading key scan data

ET6202's key scan matrix scan button and enter the data storage RAM
The ET6202 is a key scan matrix, as follows from the 10 × 2 array composed of:



Each scan key input data storage as follows, by an order from the highest-READ was read out. When the high data (b0) was read out, The next lowest data (b7) was read out.

K1……K2	**K1……K2**		Read order
SG1/KS1	SG2/KS2	x	
SG3/KS3	SG4/KS4	x	
SG5/KS5	SG6/KS6	x	
SG7/KS7	SG8/KS8	x	
SG9/KS9	SG10/KS10	x	
b0…….b1	b3……b4	b5……b7	

Notes: b5 ~ b7 no definition.

Order 3: Address set up a command

Address set up a command is set up for display memory address. If the address is 00H ~ 0DH, then the effective address. If the address is 0EH Address or higher, the data is invalid unless once again set the correct address. When the electric power, to address 00H.

Please refer to the chart below.

MSB							**LSB**
1	1	—	—	b3	b2	b1	b0

b4, b5 non-assignment
b0 to b3 address 00H ~ 0DH

Display mode and the address of the RAM

Display RAM memory through the serial interface from the external device to input data ET6202.

ET6202 of RAM address is as follows (8 units).

SG1……SG4	SG5……SG8	SG9……SG12	
00H$_L$	00H$_U$	01H$_L$	DIG1
02H$_L$	02H$_U$	03H$_L$	DIG2
04H$_L$	04H$_U$	05H$_L$	DIG3
06H$_L$	06H$_U$	07H$_L$	DIG4
08H$_L$	08H$_U$	09H$_L$	DIG5
0AH$_L$	0AH$_U$	0BH$_L$	DIG6
0CH$_L$	0CH$_U$	0DH$_L$	DIG7

b0…….b3	b4……b7
xxH$_L$	xxH$_U$
Low 4	High 4

Order 4: Display Control Order

Display Control command to control the display switches can also be used to set pulse width. Please refer to the table below. When the electric power, setting 1 / 16 the width letter and the show closed (key stop scanning).

MSB							LSB
1	0	—	—	b3	b2	b1	b0

b4, b5 non-assignment

Show:

b3 0: The show closed (to scan button)

b3 1: Open show

Dimming level:

000: width = 1 / 16

001: width = 2 / 16

010: width = 4 / 16

011: width = 10/16

100: width = 11/16

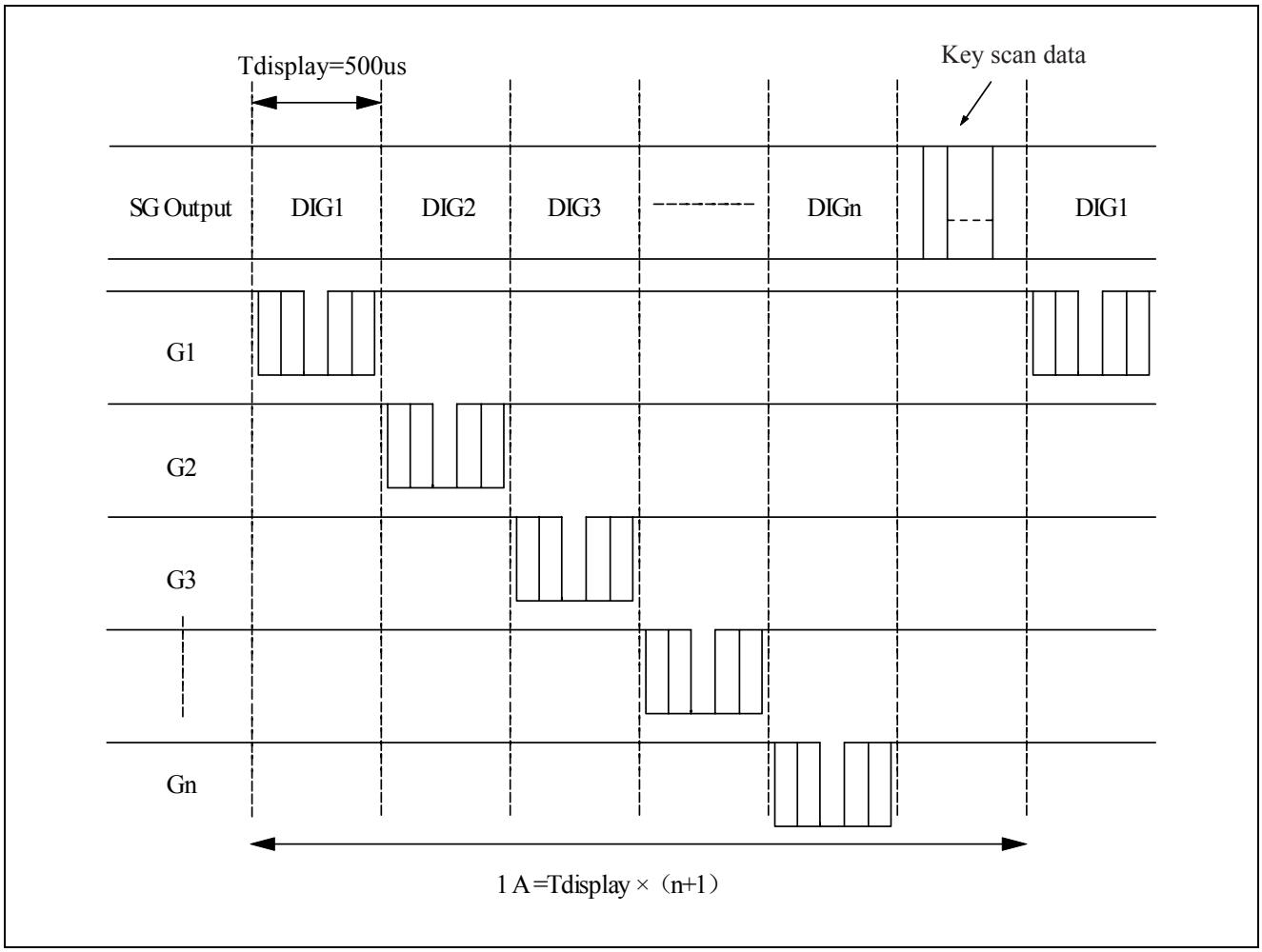
101: width = 12/16

110: width = 13/16

111: width = 14/16

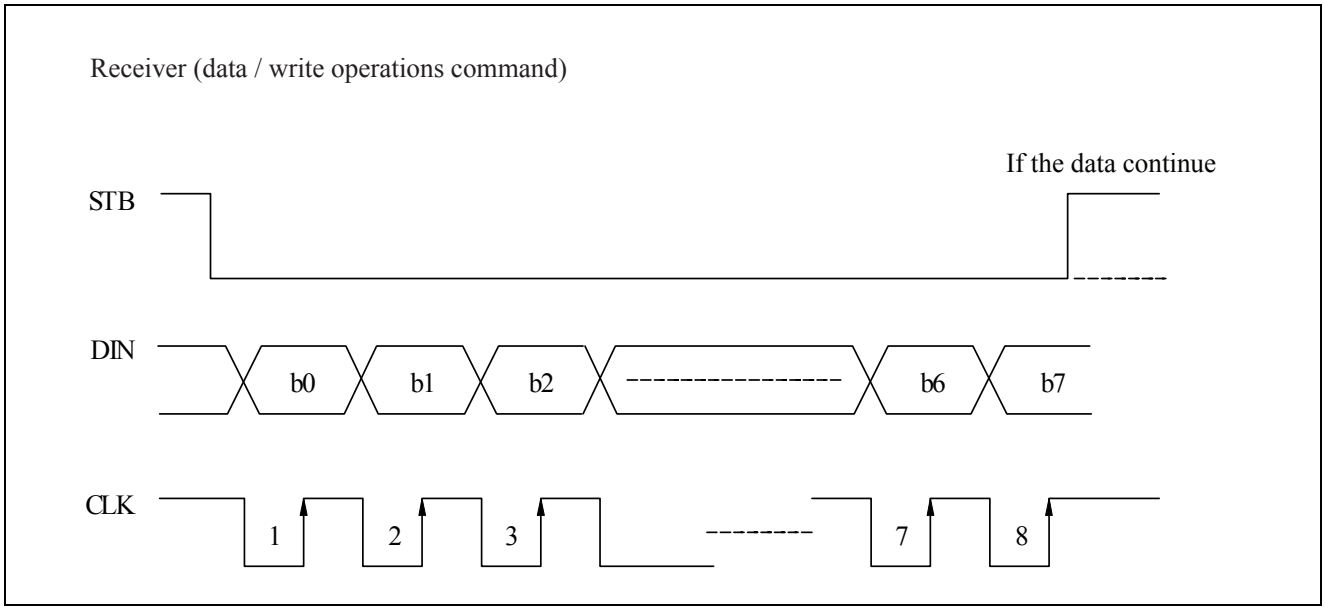
Scan timing and show

Bond plans to scan and display timing is as follows. A key scan cycle includes 2. 10 × 2 matrix of data stored in RAM.

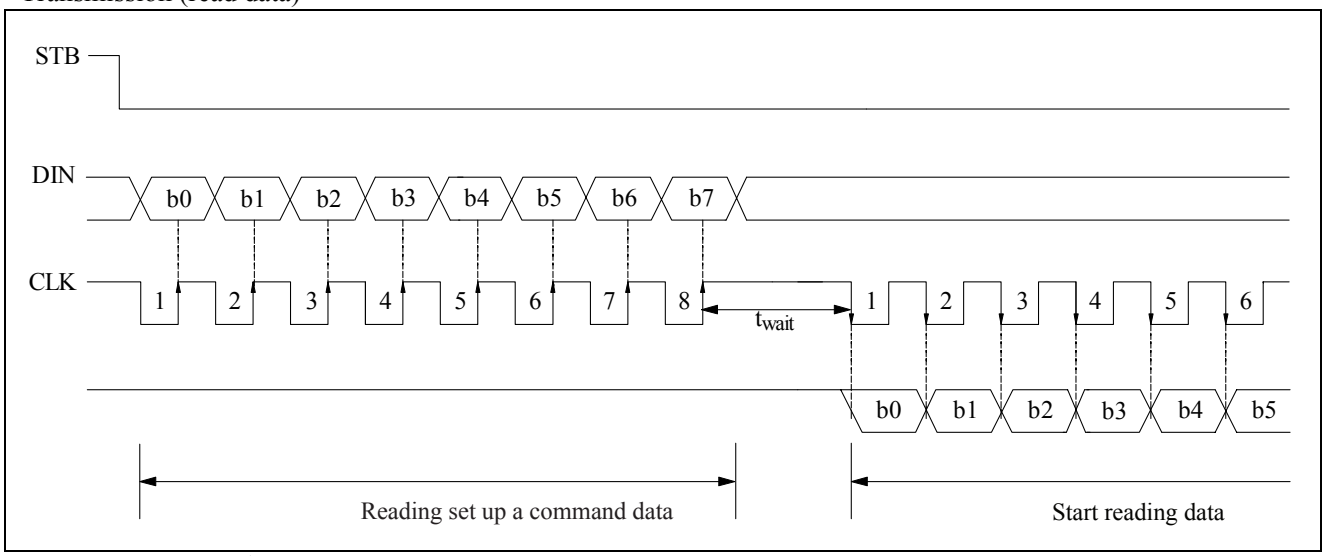


Serial communication format

The chart shown in the ET6202 is a serial communication format. DOUT port is an N-channel open drain output port, so be sure to add a guarantee Pull-up resistor (1K ~ 10K) to DOUT port.



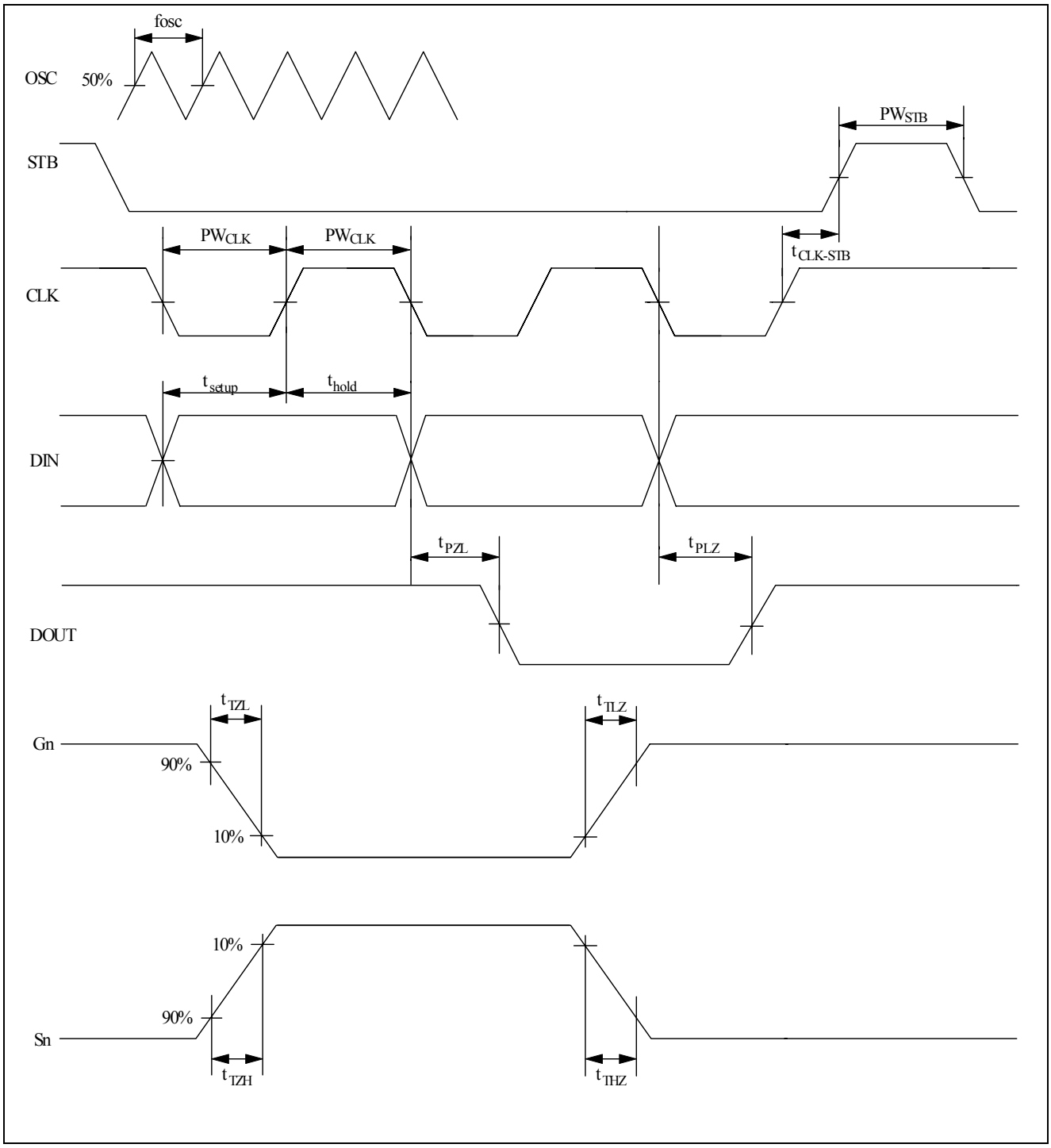
Transmission (read data)



t_{wait}(Latency) ≥ 1μs ） ≥1μs It is worth noting that when reading data, the instructions of the eighth of the clock rising edge to read the data then the first falling edge of the clock must be greater than or

1μs mean waiting time t_{wait}

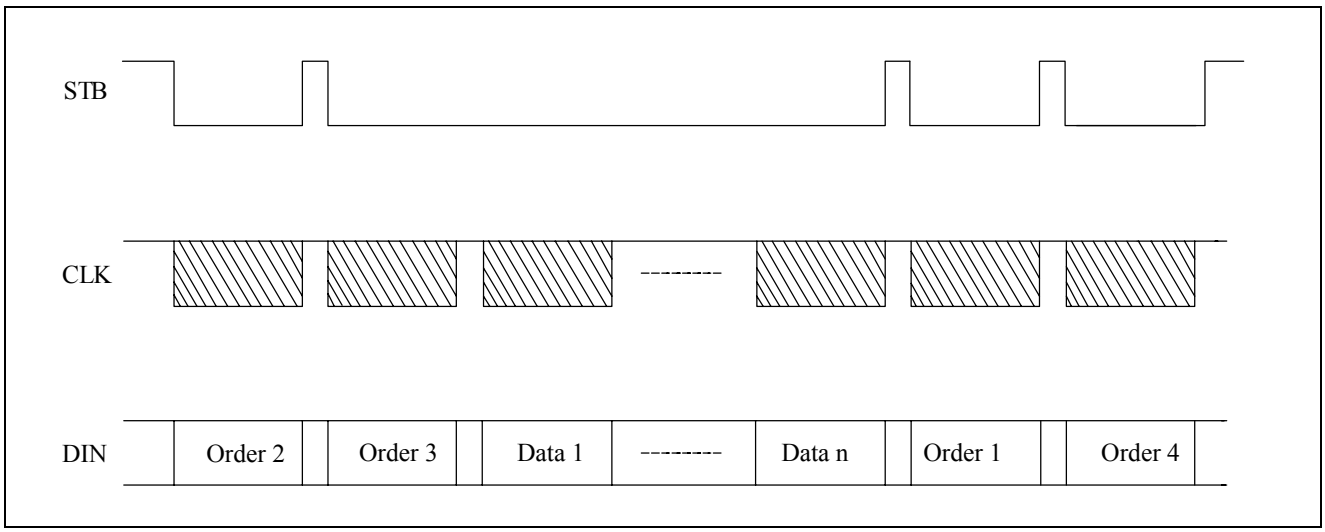
Conversion characteristic waveform
ET6202 conversion wave characteristics are as follows.



PW_{CLK} (Clock pulse) ≥ 400ns
PW_{STB}(Filter width) ≥ 1μs
t_{setup}(Data setup time) ≥ 100ns
t_{hold}(Data hold time) ≥ 100ns
$t_{CLK-STB}$(Filter clock time) ≥ 1μs
t_{THZ}(Fall time) ≤ 10μs
t_{TZH}(Rise time) ≤ 1μs
t_{PZL}(Transmission delay) ≤ 100ns
fosc = oscillation frequency
t_{PLZ}(Transmission delay) ≤ 300ns
t_{TZL}<1μs
t_{TLZ}<10μs

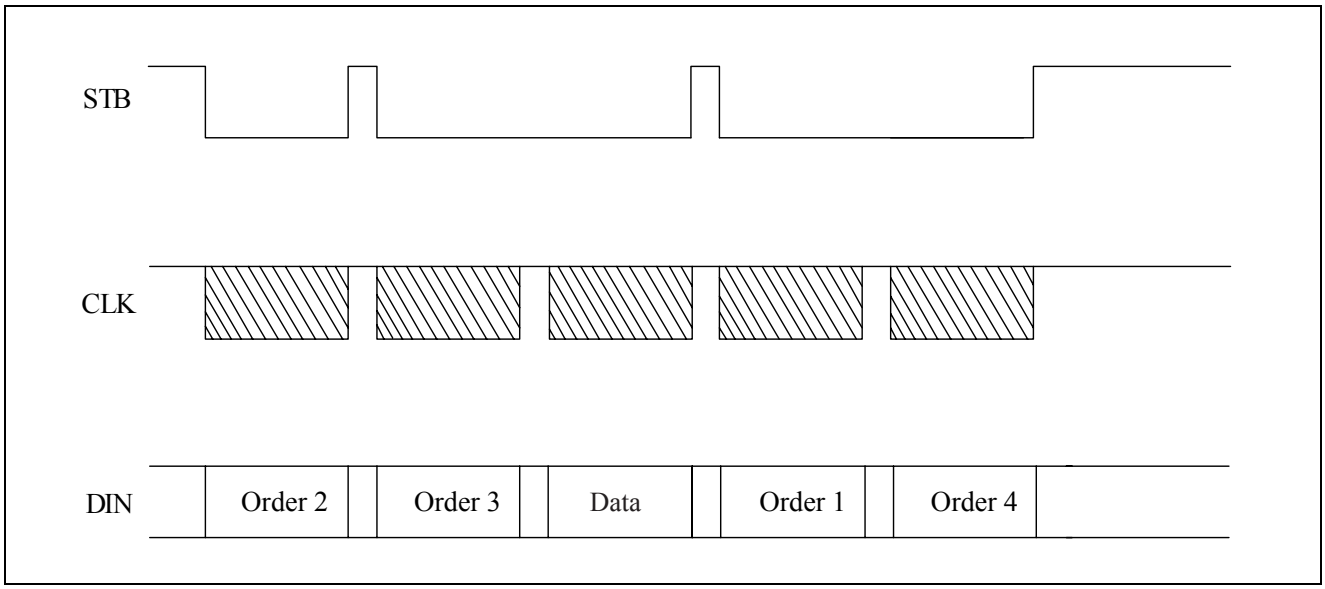
Notes: The test conditions are as follows.
t_{THZ}(Pull-down resistance = 10kΩ, load capacitance = 300pf)
t_{TLZ}(Pull-up resistor = 10kΩ, load capacitance = 300pf)

Apply
1. Input data show



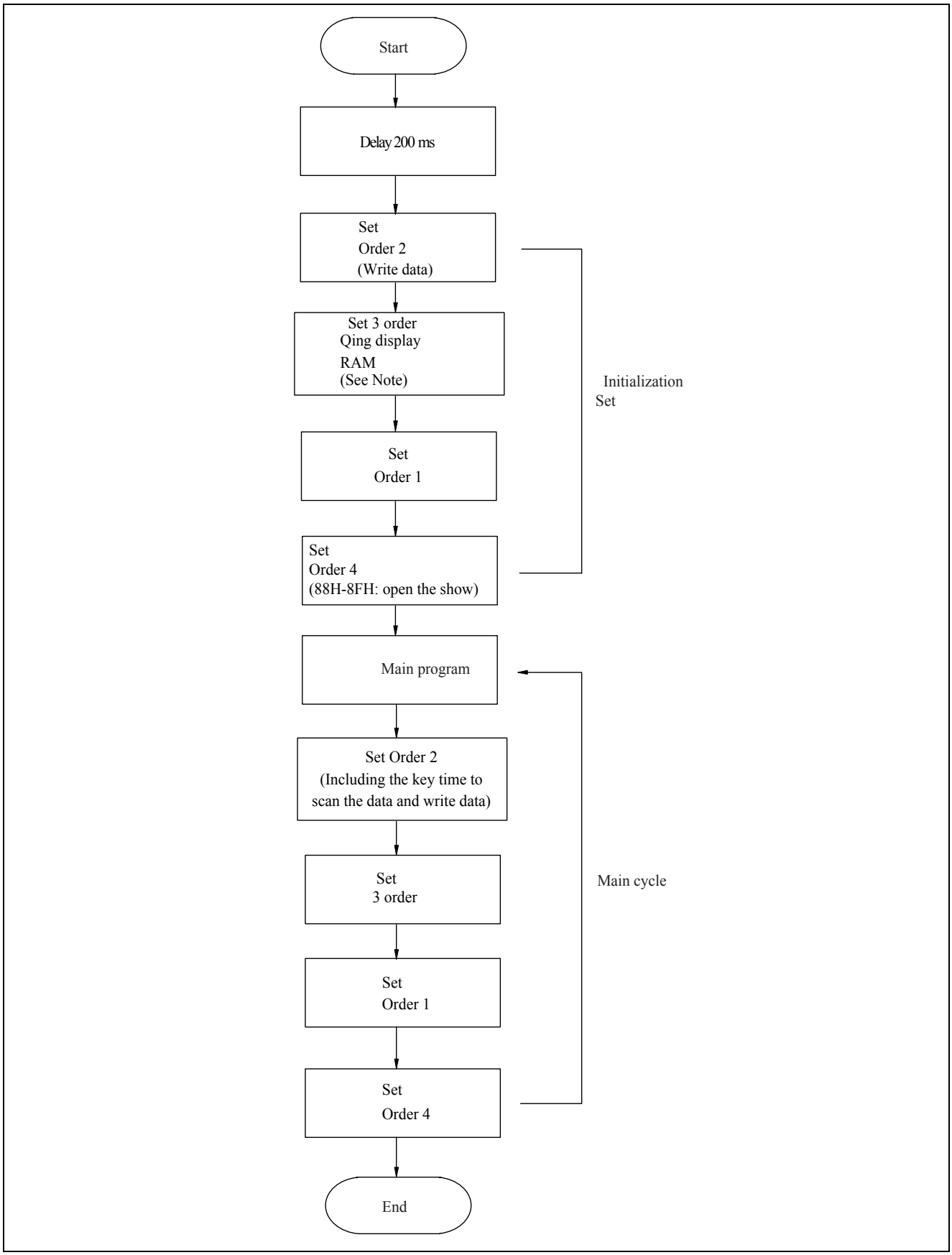
Order 1: display mode command set
Order 2: Set the order data
Order 3: Address set up a command
Data 1 ~ n: mobile data show that (the largest of 14 bytes)
Order 4: Display Control Order

2. Enter a specific address



Order 2: Set data
Order 3: Address Setting
Data: The data show

Software flow chart



Notes:
1. Order 1: display mode
2. Order 2: Set data
3. Order 3: Address Setting
4. Order 4: Display Control
When the power supply IC of the first power-on, the display RAM in the content has not been defined, so be sure to empty the initialization settings in the display RAM.

Limit parameter

1. Maximum Ratings(Ta = 25C°，GND=0V

Parameters	Symbol	Range	Unit
To provide voltage	V_{DD}	-0.5～+7	V
Logic input voltage	V_I	-0.5～V_{DD}+0.5	V
Drive output current	I_{OLGR}	+250	mA
	I_{OHSG}	-50	mA
Maximum output current	I_{TOTAL}	400	mA

2. Recommended by the working conditions(Ta = -20～+70℃，GND = 0V)

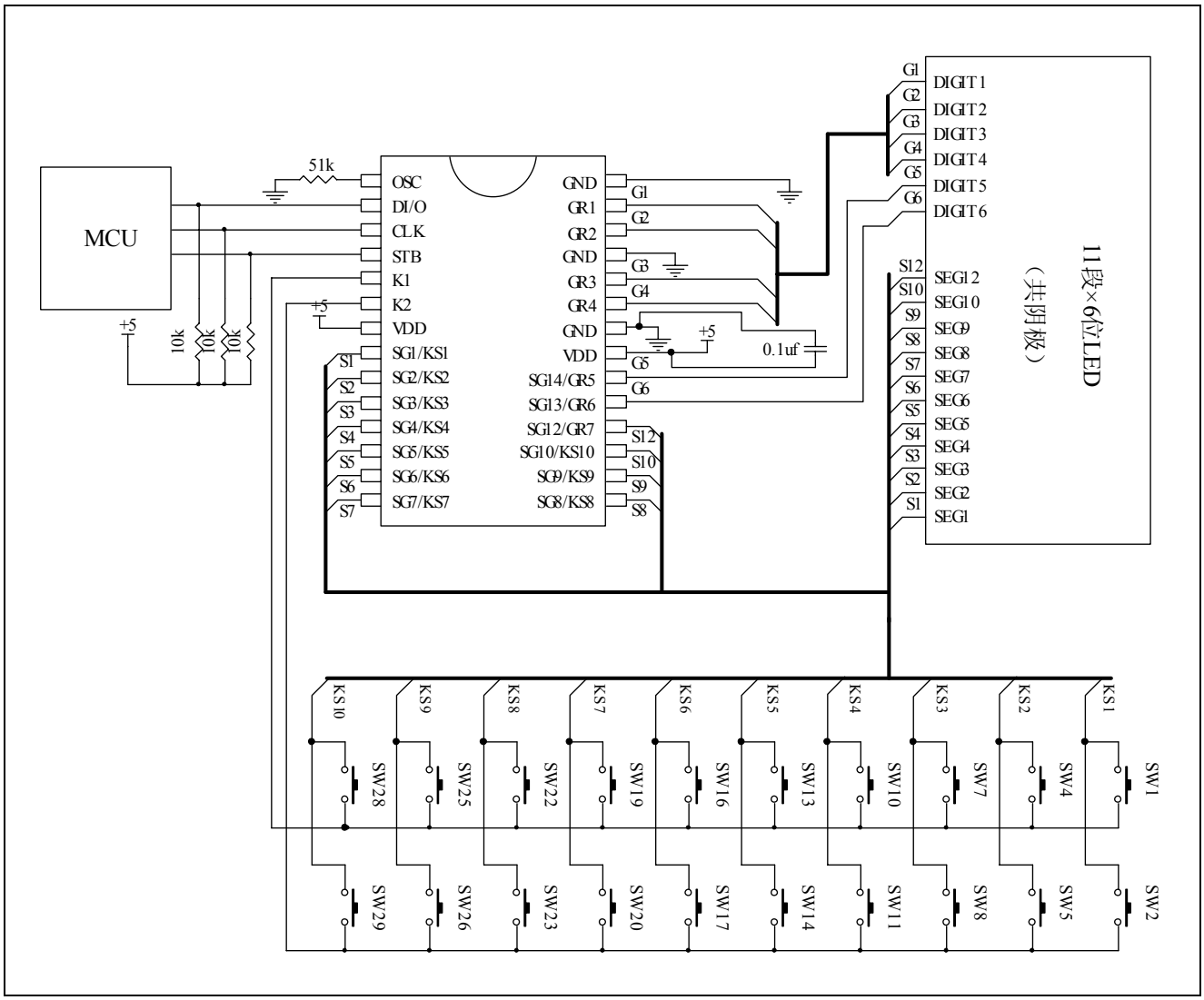
Parameters	Symbol	Minimum	Typical	Max	Unit
Logic supply voltage	V_{DD}	4.5	5	5.5	V
Dynamic current (see Note)	I_{DDdyn}	—	—	5	mA
高电平输入电压	V_{IH}	0.8V_{DD}	—	V_{DD}	V
低电平输入电压	V_{IL}	0	—	0.3V_{DD}	V

注释：测试条件：设置显示控制命令=80H（显示关闭状态&无载入情况）

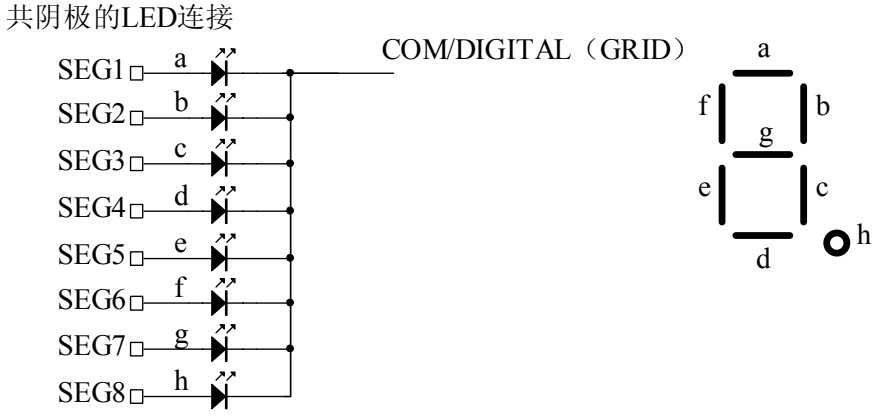
电参数（VDD = 5V，GND = 0V，Ta = 25℃）

参数	符号	测试条件	最小值	典型值	最大值	单位
高电平输出电流	IOHSG1	V0=VDD-2V SG1～SG11, SG12/GR7	-20	-25	-40	mA
	IOHSG2	V0=VDD-3V SG1～SG11, SG12/GR7	-25	-30	-50	mA
低电平输出电流	IOLGR	V0=0.3V GR1～GR6, SG12/GR7	100	140	—	mA
低电平输出电流	IOLDOUT	Vo=0.4V	4	—	—	mA
段输出端高电平输出电流百分比	ITOLSG	V0=VDD-3V SG1～SG11, SG12/GR7	—	—	+5	%
高电平输入电压	VIH	—	0.8VDD	—	5	V
低电平输入电压	VIL	—	0	—	0.3VDD	V
振荡频率	fosc	R=51k	350	500	650	kHz
K1～K2 的下拉电阻	RKN	K1～K2 VDD=5V	40	—	100	kΩ

Reference to the road map Applications



LED cathode connection



1. 连接在 GND 和 VDD 端口之间的电容（0.1μF）必须放置在离 ET6202 尽可能近的地方。
2. 建议 NC 端口（管脚 10）连接到地。

*：此电路仅供参考。