HM6709A Series

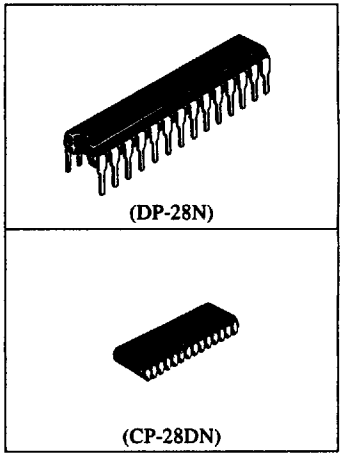
Preliminary

T-46-23-10

65536-Word × 4-Bit High Speed Static RAM

FEATURES

- 65536-words × 4 bit organization
- Fully TTL compatible input and output
- 1.0μm Hi-BiCMOS process
- +5V single supply
- Completely static memory
  No clock or timing strobe required
- Low power dissipation
  Operating: 450mW (typ.)
- Super fast
  Access time: 15/20/25 ns (max.)
  $\overline{OE}$ access time: 7/10/10ns (max.)



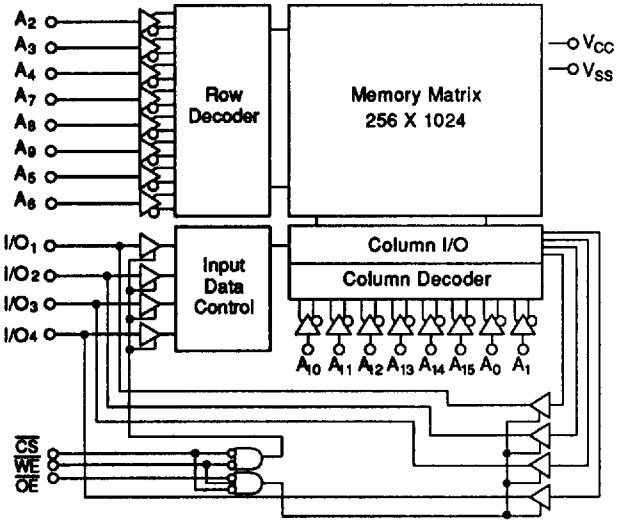
(DP-28N)

(CP-28DN)

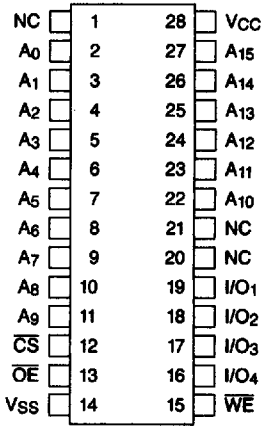
ORDERING INFORMATION

Type No.	Access Time	Package
HM6709AP-15	15ns	300 mil 28 pin
HM6709AP-20	20ns	Plastic DIP
HM6709AP-25	25ns	(DP-28N)
HM6709AJP-15	15ns	300 mil 28 pin
HM6709AJP-20	20ns	Plastic SOJ
HM6709AJP-25	25ns	(CP-28DN)

BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

PIN DESCRIPTION

Pin Name	Function
A_0-A_{15}	Address Input
I/O_1-I/O_4	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
V_{SS}	Ground
V_{CC}	Power Supply

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	-3.0	—	0.8	V

*Pulse width: 15ns, DC: -0.5V

■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5.0\ V \pm 10\%$, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6709A-15			HM6709A-20/25			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5\ V$, $V_{IN}=0\ V$ to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $\overline{WE}=V_{IL}$ $V_{I/O}=0\ V$ to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0\ mA$	—	—	100	—	—	100	mA
Average Operating Current	I_{CC1}	min. cycle, Duty: 100% $I_{I/O}=0\ mA$	—	—	140	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$, $V_{IN}=V_{IH}$ or V_{IL}	—	—	30	—	—	30	mA
	I_{SB1}	$\overline{CS} \ge V_{CC}-0.2\ V$ $V_{IN} \le 0.2\ V$ or $V_{IN} \ge V_{CC}-0.2V$	—	—	10	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8\ mA$	—	—	0.4	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-.4\ mA$	2.4	—	—	2.4	—	—	V

■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Max.	Unit	Test Condition
Input Capacitance	C_{IN}[1)]	6	pF	$V_{IN}=0\ V$
Output Capacitance	$C_{I/O}$[1)]	10	pF	$V_{I/O}=0\ V$

NOTES: 1. This parameter is sampled and not 100% tested.

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■ AC CHARACTERISTICS (V_{CC}=5 V ± 10%, Ta=0 to +70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6709A-15		HM6709A-20		HM6709A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns
Address Access Time	t_{AA}	—	15	—	20	—	25	ns
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns
Chip Selection to Output in Low Z	t_{LZ}[1), 2)]	4	—	4	—	4	—	ns
Output Enable to Output Valid	t_{OE}	0	7	0	10	0	10	ns
Output Enable to Output in Low Z	t_{OLZ}[1), 2)]	0	—	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{HZ}[1), 2)]	0	6	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	4	—	5	—	5	—	ns

NOTES: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

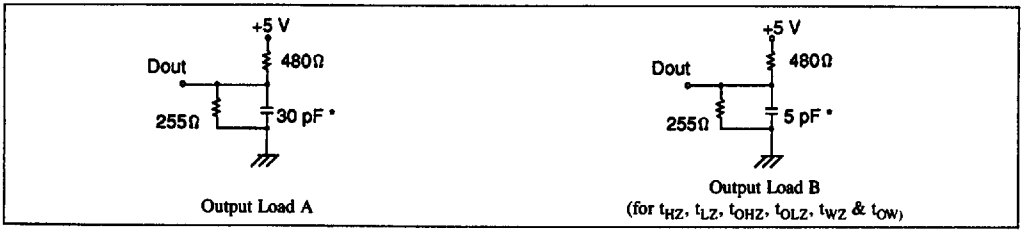
• Write Cycle

Item	Symbol	HM6709A-15		HM6709A-20		HM6709A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}[1)]	15	—	20	—	25	—	ns
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	8	—	10	—	12	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}[2), 3)]	0	6	0	8	0	10	ns
Output Disable to Output in High Z	t_{OHZ}[2), 3)]	0	6	0	8	0	10	ns
Output Active from End of Write	t_{OW}[2), 3)]	0	—	0	—	0	—	ns

NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load(B).

■ AC TEST CONDITIONS

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 2.5 V



*Including scope and jig capacitance.

■ TIMING WAVEFORM

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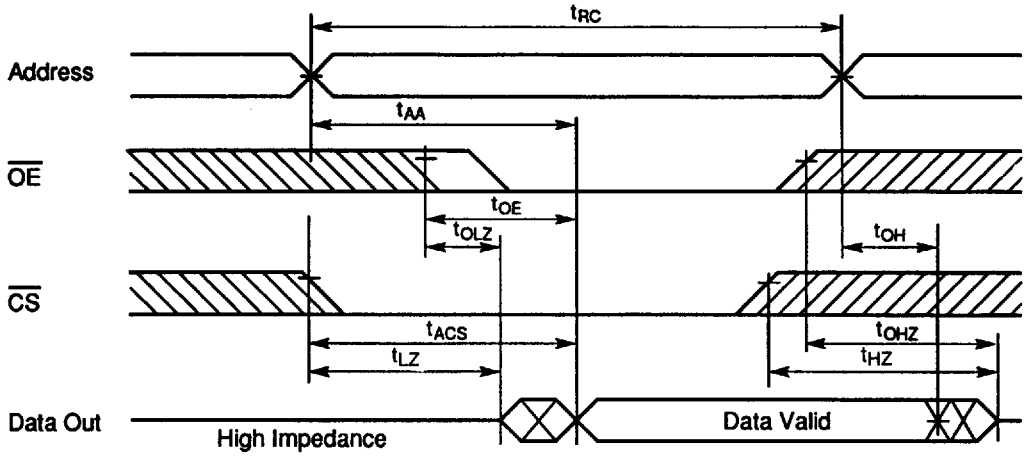
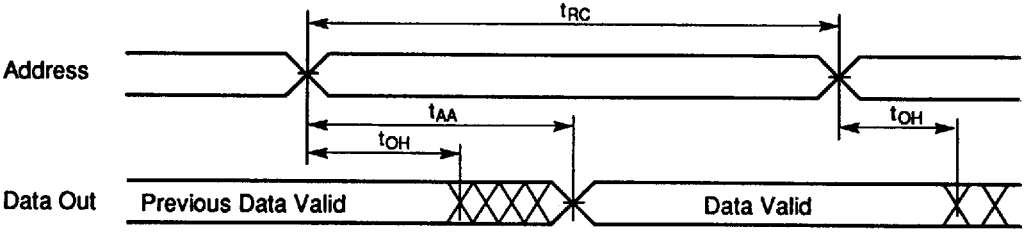
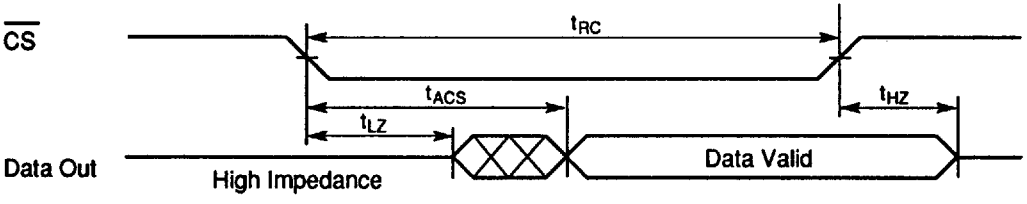
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)



• **Read Cycle (3)** (1) (3) (4)



NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}.
3. $\overline{OE}$ = V_{IL}.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

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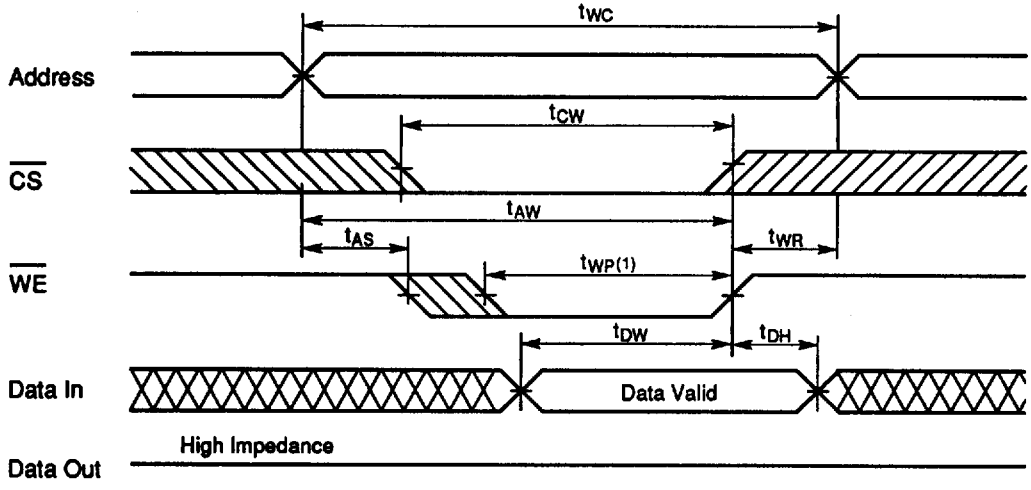
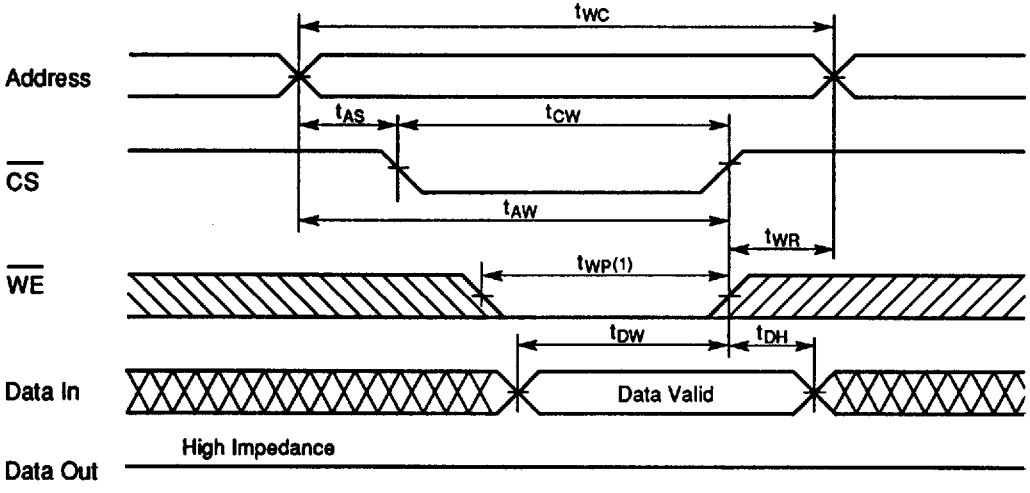
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



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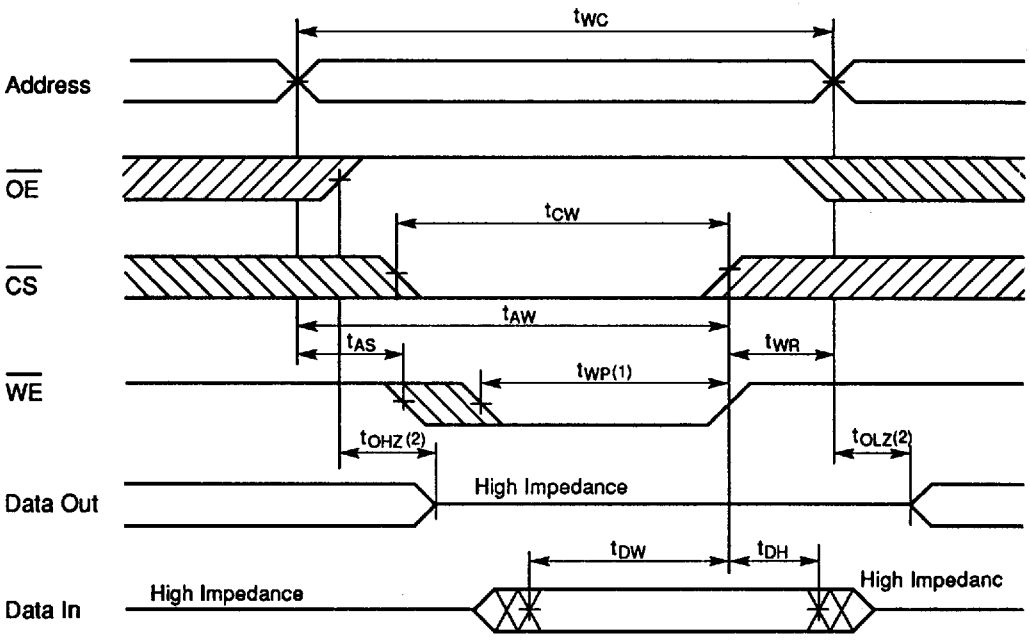
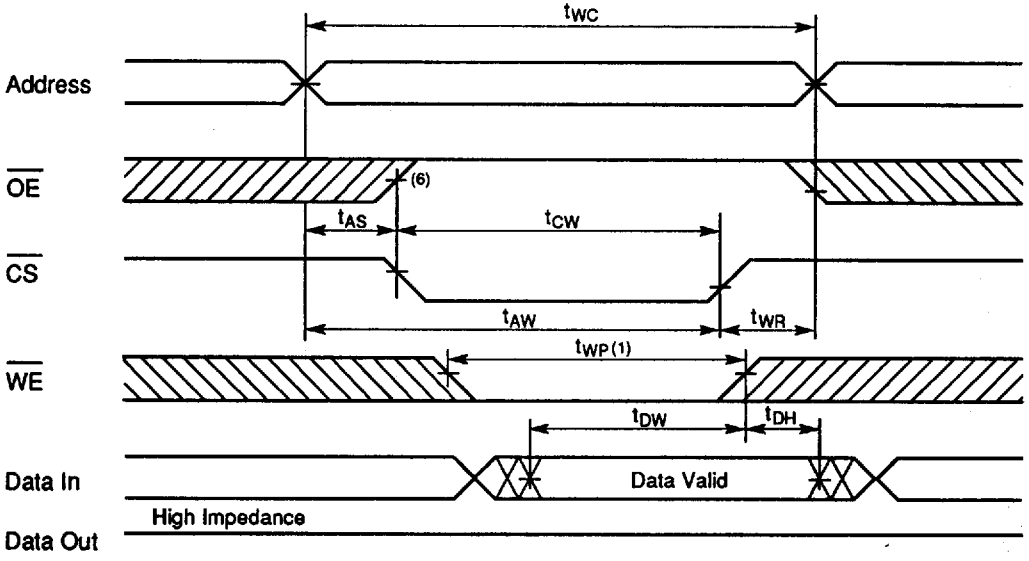
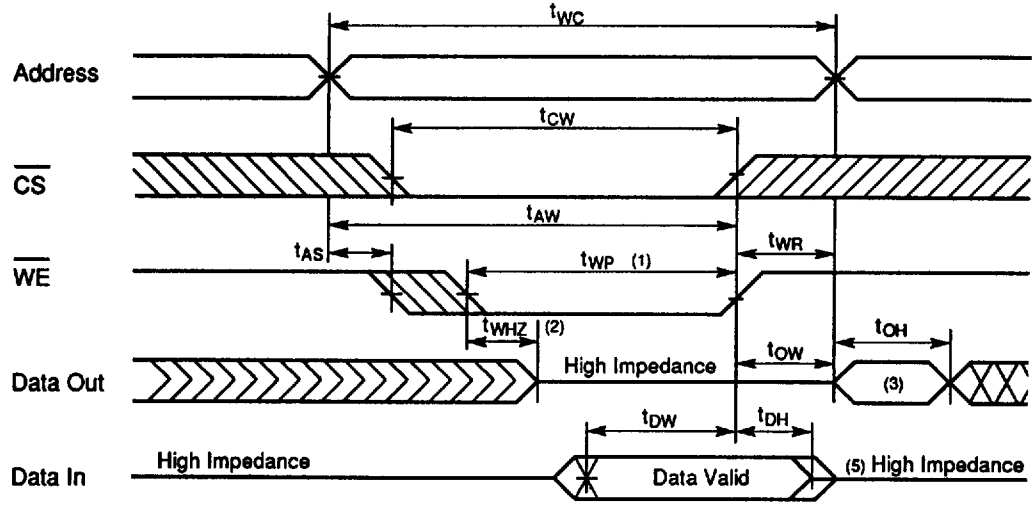
• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



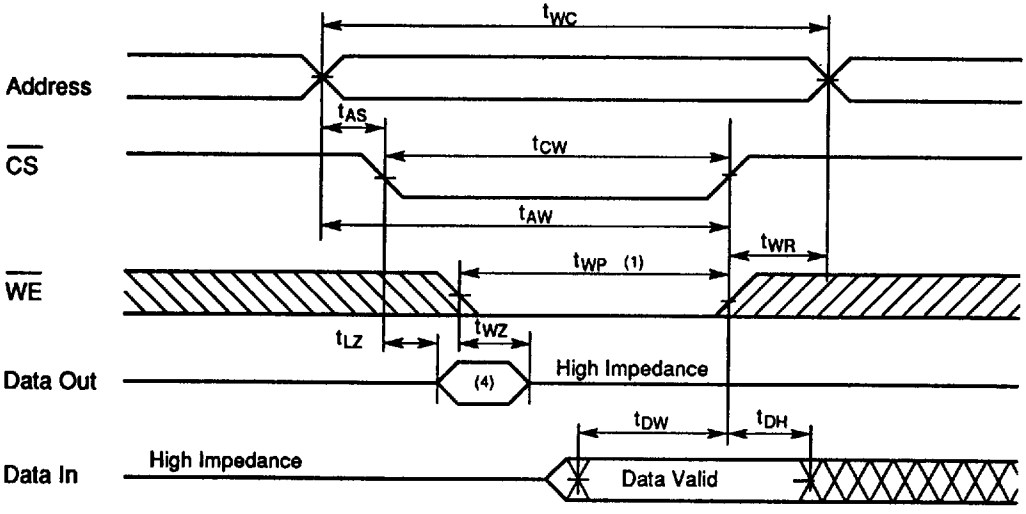
• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.