Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (64K x 1-BIT)

IDT 7187S
IDT 7187L

T-46-23-05

FEATURES:

- High speed (equal access and cycle time)
  - Military: 25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7187S
    Active: 300mW (typ.)
    Standby: 100µw (typ.)
  - IDT7187L
    Active: 250mW (typ.)
    Standby: 30µw (typ.)
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin plastic and hermetic DIP, 24-pin plastic SOIC, 22-pin and 28-pin leadless chip carrier and 24-pin flatpack and CERPACK
- Produced with advanced CEMOS™ high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86015 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability technology, CEMOS. Access times as fast as 15ns are available with maximum power consumption of 880mW.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—I_{SB} and I_{SB1}. I_{SB} provides low-power operation (358mW max.); I_{SB1} provides ultra-low-power operation (5mW max.). The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30µW.

Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil plastic or hermetic DIP, 24-pin plastic SOIC, 22- and 28-pin leadless chip carriers, or 24-pin flatpack or CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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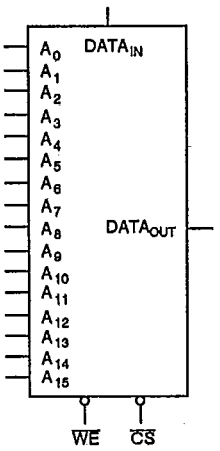
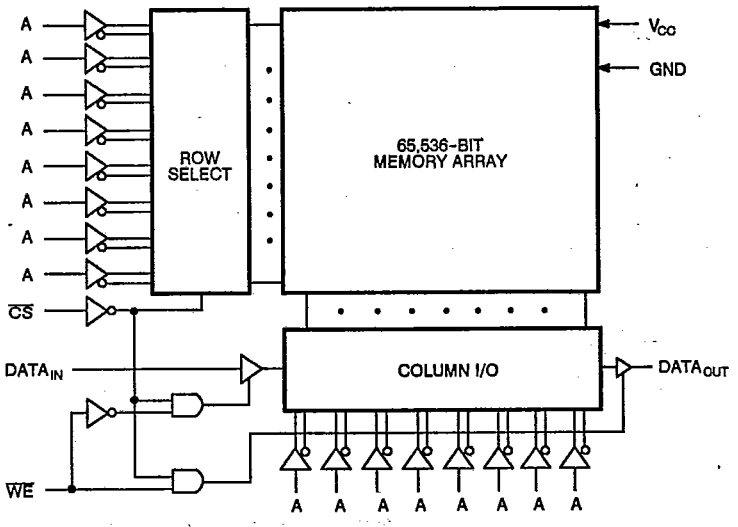
LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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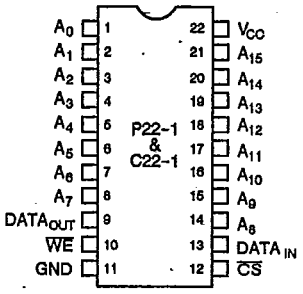
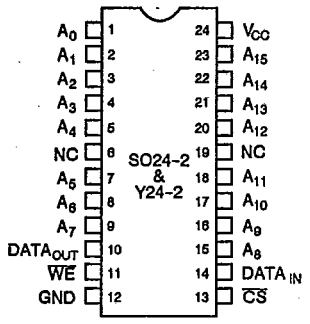
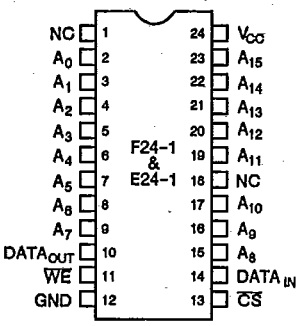
PIN CONFIGURATIONS



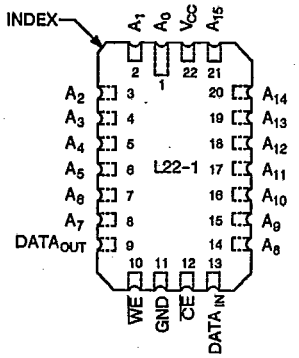
DIP
TOP VIEW



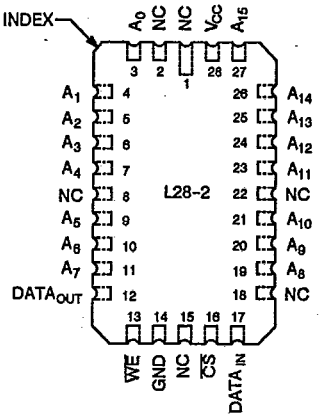
SOIC/SOJ
TOP VIEW



FLATPACK/CERPACK
TOP VIEW



22-PIN LCC
TOP VIEW



28-PIN LCC
TOP VIEW

PIN NAMES

A_0–A_{15}	Address Inputs	$DATA_{IN}$	Data Input
$\overline{CS}$	Chip Select	$DATA_{OUT}$	Data Output
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7187S MIN.	IDT7187S TYP.(1)	IDT7187S MAX.	IDT7187L MIN.	IDT7187L TYP.(1)	IDT7187L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

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DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	POWER	7187S15 COM'L.	7187S15 MIL.	7187S20 COM'L.	7187S20 MIL.	7187S25 7187L25 COM'L.	7187S25 7187L25 MIL.	7187S30/35 7187L30/35 COM'L.	7187S30/35 7187L30/35 MIL.	7187S45/55(3) 7187L45/55(3) COM'L.	7187S45/55(3) 7187L45/55(3) MIL.	7187S70 7187L70 COM'L.	7187S70 7187L70 MIL.	7187S85 7187L85 COM'L.	7187S85 7187L85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	135	–	120	140	90	105	90	105	90	105	–	105	–	105	mA
		L	–	–	–	–	70	85	70	85	70	85	–	85	–	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	180	–	155	175	120	130	110	120	110	120	–	120	–	120	mA
		L	–	–	–	–	100	110	95/90	110/100	85	95	–	90	–	90	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S	65	–	60	65	55	55	45	50	45	50	–	50	–	50	mA
		L	–	–	–	–	45	50	40/35	45/40	30/25	35/30	–	28	–	28	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	–	–	–	–	0.3	1.5	0.3	1.5	0.3	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. f = f_{MAX} (All inputs except Chip Select cycling at f = $1/t_{RC}$). f = 0 means no address or control lines change.
3. -55°C to +125°C temperature range only.

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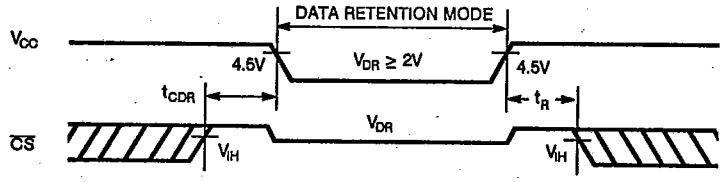
DATA RETENTION CHARACTERISTICS

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

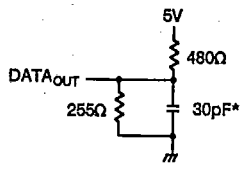


Figure 1. Output Load

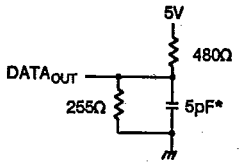


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7187S15[1]/20 MIN.	7187S15[1]/20 MAX.	7187S25/30 7187L25/30 MIN.	7187S25/30 7187L25/30 MAX.	7187S35/45 7187L35/45 MIN.	7187S35/45 7187L35/45 MAX.	7187S55[2] 7187L55[2] MIN.	7187S55[2] 7187L55[2] MAX.	7187S70[2] 7187L70[2] MIN.	7187S70[2] 7187L70[2] MAX.	7187S85[2] 7187L85[2] MIN.	7187S85[2] 7187L85[2] MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15/20	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	–	6	–	12/15	–	17/20	–	30	–	30	–	40	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	15/20	–	20/30	–	30/35	–	35	–	35	–	40	ns

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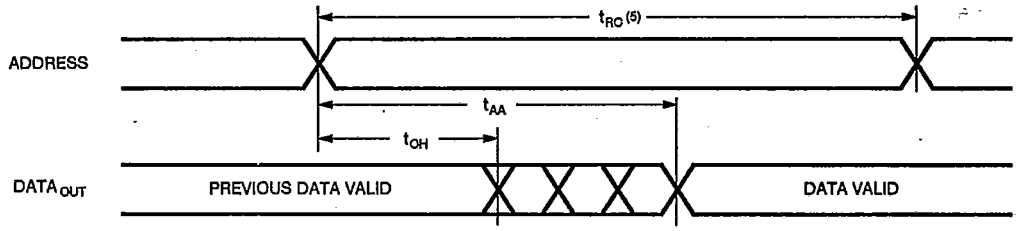
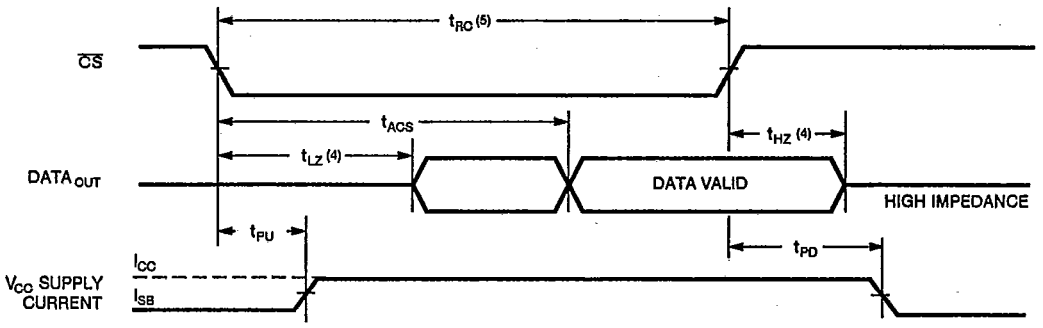
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



NOTES:
1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7187S15[1]/20 MIN.	7187S15[1]/20 MAX.	7187S25/30 7187L25/30 MIN.	7187S25/30 7187L25/30 MAX.	7187S35/45 7187L35/45 MIN.	7187S35/45 7187L35/45 MAX.	7187S55[2] 7187L55[2] MIN.	7187S55[2] 7187L55[2] MAX.	7187S70[2] 7187L70[2] MIN.	7187S70[2] 7187L70[2] MAX.	7187S85[2] 7187L85[2] MIN.	7187S85[2] 7187L85[2] MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	12/15	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{CW}	Chip Select to End of Write	12/15	–	20/22	–	25/40	–	50	–	55	–	65	–	ns
t_{AW}	Address Valid to End of Write	12/15	–	20/22	–	25/40	–	50	–	55	–	65	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	12/15	–	20	–	20/25	–	35	–	40	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	8/10	–	15/20	–	15/25	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z[3]	–	6/8	–	12/15	–	15/30	–	30	–	30	–	40	ns
t_{OW}	Output Active from End of Write[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

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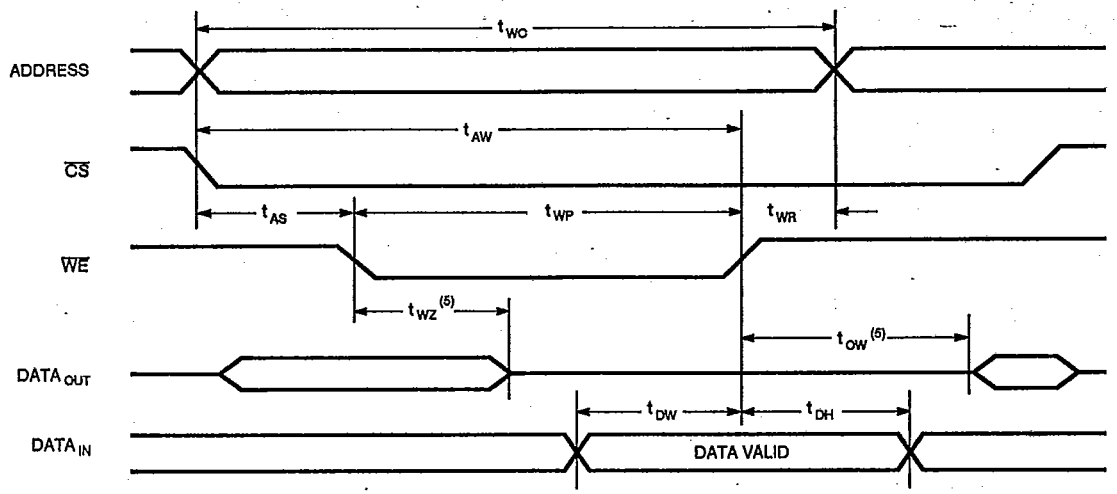
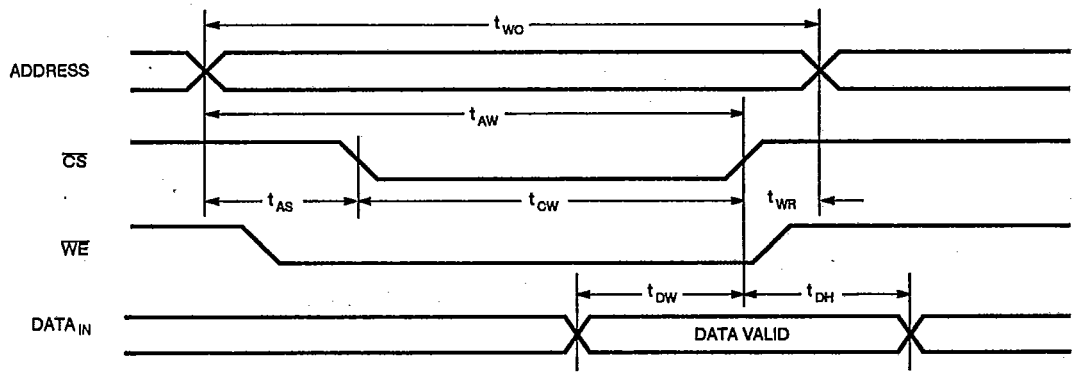
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 4)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).

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TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

ORDERING INFORMATION