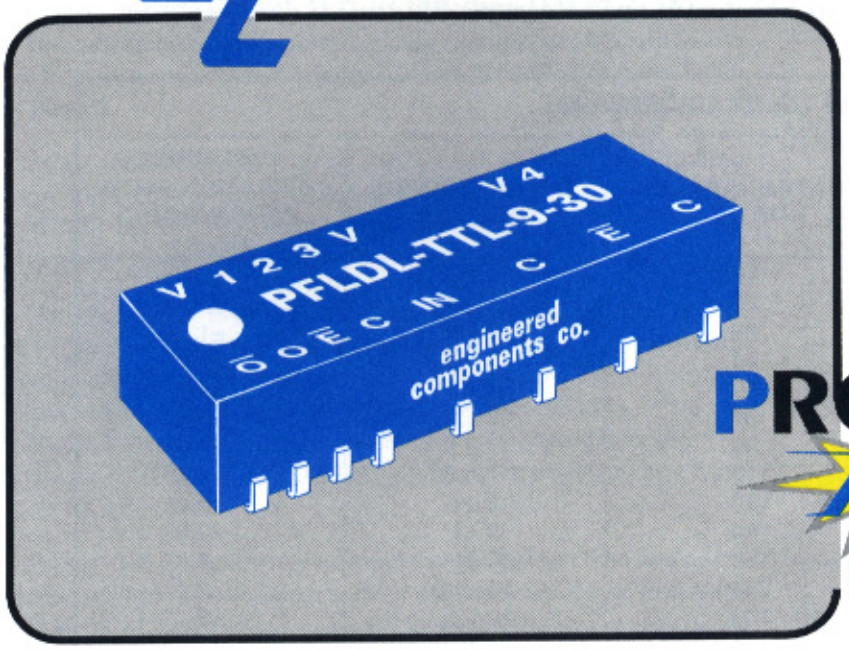
EC²



low profile

T²L COMPATIBLE 4-BIT PROGRAMMABLE FAST LOGIC DELAY LINE

- T²L input and output
- Delays stable and precise
- 24-pin DIP package
- Leads - thru-hole, J, Gull Wing or Tucked
- Available in delays up to 1509ns
- Available in 24 delay steps with resolution from .5 to 100ns
- Propagation delays fully compensated
- All delays are digitally programmable
- 10 T²L fan-out capacity

design notes

The "DIP Series" of Programmable Logic Delay Lines developed by Engineered Components Company have been designed to allow for final delay adjustment during or after installation in a circuit. These Logic Delay Lines incorporate required driving and pick-off circuitry and are contained in a 24-pin DIP package compatible with FAST and Schottky T²L circuits. These modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The MTBF on these modules, when calculated per MIL-HDBK-217 for 50°C ground fixed environment, is in excess of 1 million hours. The design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the required delay.

The Logic Delay Lines are digitally programmable by the presence of either a "1" or a "0" at each of the programming pins. Since the input and the output terminals are fixed and the programming is accomplished only by DC voltage levels, programming may be accomplished by remote switching or permanent termination of the appropriate programming pins of the Logic Delay Line to ground; The Logic Delay Line may also be programmed automatically by computer generated data. MUX set-up time is 4ns typical. When no need exists in the application to change delay time during normal use, the desired delay is most conveniently established by use of a ground pad around each programming pin; programming is accomplished by cutting off those pins which are to remain at state "1" before insertion of the Logic Delay Line into the printed circuit board.

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DESIGN NOTES (continued)

The PFLDL-TTL is offered in 24 models with time delays to a maximum of 1509ns and with step resolution as shown in the Part Number Table. Programming of maximum delay is accomplished in 16 steps in accordance with the Truth Table example shown on page 3. Tolerances on minimum delay, delay change per step and deviation from the programmed delay are shown in the Part Number Table on page 3.

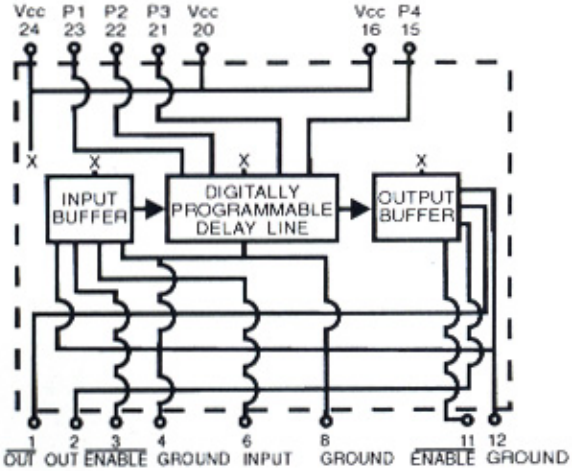
Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 4ns maximum, when measured from 0.8V to 2.0V. Temperature coefficient of delay is approximately -300 ppm/°C over the operating temperature range of 0 to +70°C.

The PFLDL-TTL is designed for use with positive input pulses and will reproduce these at the output without inversion. A complementary ($\overline{OUT}$) output is provided approximately 1ns before normal output. All modules can be driven by a standard Schottky T^2L gate. Output is Schottky T^2L toggle; programming inputs are Schottky T^2L single fan-in. These Logic Delay Lines have the capability of driving up to 10 T^2L loads.

These "DIP Series" Programmable Logic Delay Lines are packaged in a 24-pin DIP housing, molded of flameproof Diallyl Phthalate per MIL-M-14, type SDG-F, and are fully encapsulated in epoxy resin. Thru-hole, J, Gull Wing or Tucked Lead configurations are available on these modules (see Part Number Table note to specify). Leads meet the solderability requirements of MIL-STD-202, Method 208. Corner standoffs on the housing of the thru-hole lead version and lead design of the surface mount versions provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

Marking consists of the manufacturer's name, logo (EC^2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

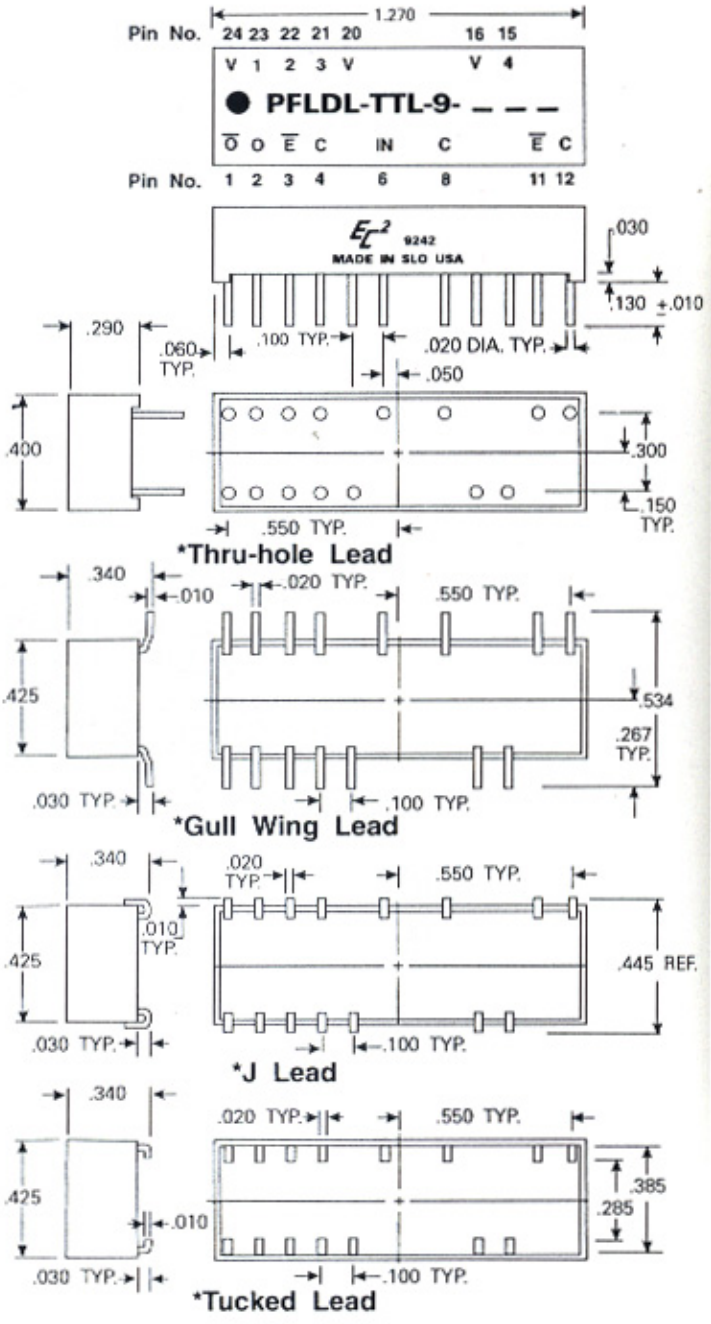
BLOCK DIAGRAM IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. V_{CC} supply voltage is maintained at 5.0V DC.
3. All units are tested using a Schottky toggle-type positive input pulse and one Schottky T^2L load at the output.
4. Input pulse width used is 40ns for units with delay change of 0.5 to 5.0ns/step and 400ns for units with delay change of 6ns/step and greater. Pulse period for all units is 5000ns.

MECHANICAL DETAIL IS SHOWN BELOW



OPERATING SPECIFICATIONS

* V_{CC} supply voltage:	4.75 to 5.25V DC
V_{CC} supply current:	80mA typical
Logic 1 Input:	
Voltage	2V min.; 5.5V max.
Current	2.7V = 40uA max.
	5.5V = 2mA max.
Logic 0 Input:	
Voltage	.8V max.
Current	-1.2mA max.
Logic 1 Voltage out:	2.7V min.
Logic 0 Voltage out:	.5V max.
Operating temperature range:	0 to 70°C
Storage temperature:	-55 to +125°C.

* Delays increase approximately 1.5% for a decrease of 5% in supply voltage and decrease approximately 1.5% for an increase of 5% in supply voltage.

PART NUMBER TABLE

***Suffix Part Number with G (for Gull Wing Lead), J (for J Lead), F (for Thru-hole Lead) or T (for Tucked Lead). Examples: PFLDL-TTL-9-50G (Gull Wing), PFLDL-TTL-9-70J (J Lead), PFLDL-TTL-9-80F (Thru-hole Lead) or PFLDL-TTL-9-15T (Tucked Lead).**

Ø DELAYS AND TOLERANCES (in ns)				
PART NUMBER	*STEP ZERO DELAY TIME	MAXIMUM DELAY TIME (NOM)	DELAY CHANGE PER STEP	**MAXIMUM DEVIATION FROM PROGRAMMED DELAY
PFLDL-TTL-9-.5	9.0 ±.6	16.5	.5 ±.3	±.7
PFLDL-TTL-9-1	9.0 ±.6	24	1 ±.4	±.8
PFLDL-TTL-9-2	9.0 ±.6	39	2 ±.5	±1.2
PFLDL-TTL-9-3	9.0 ±.6	54	3 ±.5	±1.6
PFLDL-TTL-9-4	9.0 ±.6	69	4 ±.6	±1.8
PFLDL-TTL-9-5	9.0 ±.6	84	5 ±.6	±2.0
PFLDL-TTL-9-6	9.0 ±.6	99	6 ±.8	±2.4
PFLDL-TTL-9-7	9.0 ±.6	114	7 ±.8	±2.8
PFLDL-TTL-9-8	9.0 ±.6	129	8 ±1	±3.2
PFLDL-TTL-9-9	9.0 ±.6	144	9 ±1	±3.6
PFLDL-TTL-9-10	9.0 ±.6	159	10 ±1	±4
PFLDL-TTL-9-15	9.0 ±.6	234	15 ±1.5	±6
PFLDL-TTL-9-20	9.0 ±.6	309	20 ±2	±8
PFLDL-TTL-9-25	9.0 ±.6	384	25 ±2	±10
PFLDL-TTL-9-30	9.0 ±.6	459	30 ±2.5	±12
PFLDL-TTL-9-35	9.0 ±.6	534	35 ±2.5	±14
PFLDL-TTL-9-40	9.0 ±.6	609	40 ±3	±16
PFLDL-TTL-9-45	9.0 ±.6	684	45 ±3	±18
PFLDL-TTL-9-50	9.0 ±.6	759	50 ±3	±20
PFLDL-TTL-9-60	9.0 ±.6	909	60 ±4	±24
PFLDL-TTL-9-70	9.0 ±.6	1059	70 ±4	±27
PFLDL-TTL-9-80	9.0 ±.6	1209	80 ±5	±30
PFLDL-TTL-9-90	9.0 ±.6	1359	90 ±5	±34
PFLDL-TTL-9-100	9.0 ±.6	1509	100 ±6	±38

TRUTH TABLE EXAMPLES

PROGRAMMING PINS / PART NUMBER	4 0 3 0 2 0 1 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
PFLDL-TTL-9-.5	9	.5	1	1.5	2	2.5	3	3.5	4	4.5	5	5.5	6	6.5	7	7.5
PFLDL-TTL-9-1	9	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PFLDL-TTL-9-2	9	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
ETC.																

* Delay at step zero is referenced to the input pin.

** All delay times after step zero are referenced to step zero.

Ø All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.