32-Bit Edge Triggered D-Type Flip-Flop with 3-State Outputs

Product Features

- PI74ALVCH32374 is designed for low voltage operation
- V_{CC} = 2.3V to 3.6V
- Typical V_{OLP} (Output Ground Bounce)
  < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
  > 2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-State eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 96-ball, 13.5mm x 5.5mm x 1.4mm low profile fine pitch ball grid array, LFBGA (NB)

Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

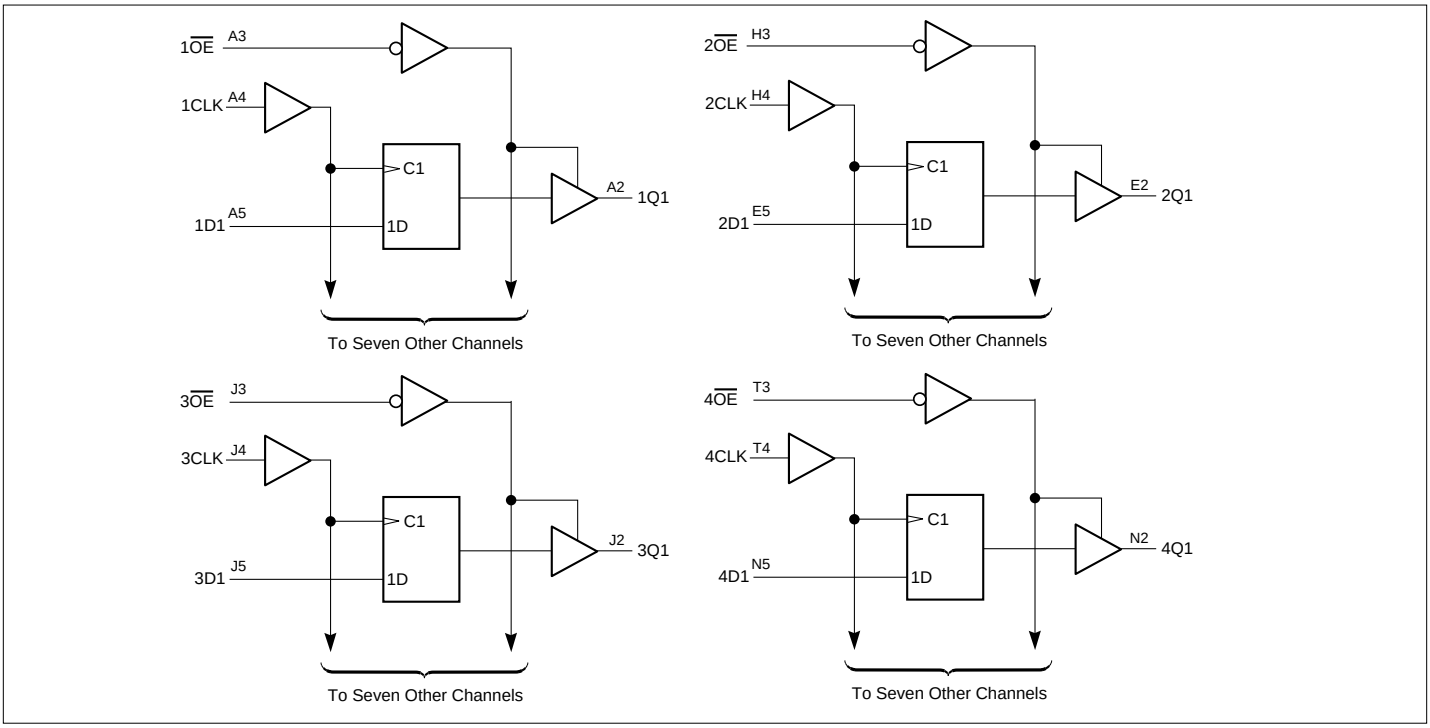
This 32-bit edge-triggered D-type flip-flop is designed for 2.3V to 3.6V V_{CC} operation.

The PI74ALVCH32374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as four 8-bit flip-flops or two 16-bit flip-flops or one 32-Bit flip-flop. On the positive transition of the Clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs. $\overline{OE}$ can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In that state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Logic Block Diagram



Product Pin Description

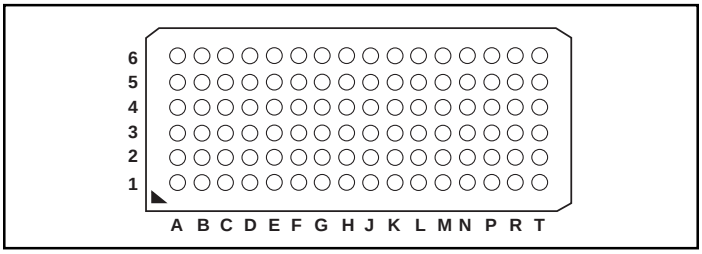
Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
V_{CC}	Power

Truth Table(1)

Inputs			Outputs
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

Notes:
1. H = High Signal Level
   L = Low Signal Level
   X = Irrelevant
   Z = High Impedance
   ↑ = LOW to HIGH Transition
   n = 1,2

NB Package (Top View)



Terminal Assignments

6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1CLK	GND	V_{CC}	GND	GND	V_{CC}	GND	2CLK	3CLK	GND	V_{CC}	GND	GND	V_{CC}	GND	4CLK
3	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$2\overline{OE}$	$3\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{CC}	–0.5V to 4.6V
Input Voltage Range, V_I: Except I/O ports (1)	–0.5V to 4.6V
I/O ports (1,2)	–0.5V to V_{CC} + 0.5V
Output Voltage Range, V_O (1,2)	–0.5V to V_{CC} +0.5V
Input Clamp Current, I_{IK} (V_I <0)	–50mA
Output Clamp Current, I_{OK} (V_O <0)	–50mA
Continuous Output Current, I_O	±50mA
Continuous Current through each V_{CC} or GND	±100mA
Package Thermal Impedance, θ_{JA} (3)	40ºC/W
Storage Temperature Range, T_{STG}	–65ºC to 150ºC

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note:

1. The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions(1)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}	Input Voltage		0		V_{CC}	
V_{OUT}	Output Voltage		0		V_{CC}	
I_{OH}	Output HIGH Current	V_{CC} = 2.3V			–12	mA
		V_{CC} = 2.7V			–12	
		V_{CC} = 3.0V			–24	
I_{OL}	Output LOW Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate		0		10	ns/V
T_A	Operating Free-Air Temperature		–40		85	°C

Note 1: All unused inputs must be held at V_{CC} or GND to ensure proper device operation

DC Electrical Characteristics (Over the Operating Range, $T_A = -40°C$ to $+85°C$, $V_{CC} = 3.3V \pm 10\%$)

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -100\mu A$, V_{CC} = Min. to Max.	V_{CC}- 0.2			V
		$V_{IH} = 1.7V$, $I_{OH} = -6mA$, $V_{CC} = 2.3V$	2.0			
		$V_{IH} = 1.7V$, $I_{OH} = -12mA$, $V_{CC} = 2.3V$	1.7			
		$V_{IH} = 2.0V$, $I_{OH} = -12mA$, $V_{CC} = 2.7V$	2.2			
		$V_{IH} = 2.0V$, $I_{OH} = -12mA$, $V_{CC} = 3.0V$	2.4			
		$V_{IH} = 2.0V$, $I_{OH} = -24mA$, $V_{CC} = 3.0V$	2.0			
V_{OL}	Output LOW Voltage	$I_{OL} = -100\mu A$, V_{IL} = Min. to Max.			0.2	
		$V_{IL} = 0.7V$, $I_{OL} = 6mA$, $V_{CC} = 2.3V$			0.4	
		$V_{IL} = 0.7V$, $I_{OL} = 12mA$, $V_{CC} = 2.3V$			0.7	
		$V_{IL} = 0.8V$, $I_{OL} = 12mA$, $V_{CC} = 2.7V$			0.4	
		$V_{IL} = 0.8V$, $I_{OL} = 24mA$, $V_{CC} = 3.0V$			0.55	
I_{IN}	Input Current	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.6V$			±5	µA
I_{IN} (HOLD)	Input Hold Current	$V_{IN} = 0.7V$, $V_{CC} = 2.3V$	45			
		$V_{IN} = 1.7V$, $V_{CC} = 2.3V$	–45			
		$V_{IN} = 0.8V$, $V_{CC} = 3.0V$	75			
		$V_{IN} = 2.0V$, $V_{CC} = 3.0V$	–75			
		$V_{IN} = 0$ to $3.6V$, $V_{CC} = 3.6V$[3]			±500	
I_{OZ}	Output Current (3-State Outputs)	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 3.6V$			±10	
I_{CC}	Supply Current	$V_{CC} = 3.6V$, $I_{OUT} = 0\mu A$, $V_{IN} = GND$ or V_{CC}			40	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = 3.0V$ to $3.6V$ One Input at V_{CC} - 0.6V Other Inputs at V_{CC} or GND			750	
C_I	Control Inputs	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3V$		3		pF
	Data Inputs			6		
C_O	Outputs	$V_O = V_{CC}$ or GND, $V_{CC} = 3.3V$		7		

Notes:

1. For Min. or Max conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$, $+25°C$ ambient and maximum loading.
3. This is the bushold maximum dynamic current. It is the mimum overdrive current necessary to switch the input from one state to another.

Timing Requirements over Operating Range

Parameters	Description	V_{CC} = 2.5V ±0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ±0.3V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock Frequency	0	150	0	150	0	150	MHz
t_W	Pulse Duration CLK HIGH or LOW	3.3		3.3		3.3		ns
t_{SU}	Setup Time Data Before CLK↑	2.1		2.2		1.9		
t_H	Hold Time Data After CLK↑	0.6		0.5		0.5		

Switching Characteristics over Operating Range[1]

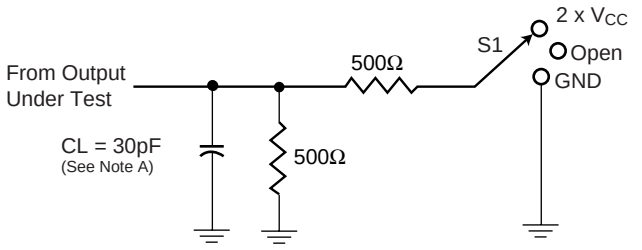
Parameters	From (INPUT)	To (OUTPUT)	V_{CC} = 2.5V ±0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ±0.3V		Units
			Min.[2]	Max.	Min.	Max.	Min.[2]	Max.	
f_{MAX}			150		150		150		MHz
t_{PD}	CLK	Q	1.0	5.3		4.9	1.0	4.2	ns
t_{EN}	$\overline{OE}$		1.0	6.2		5.9	1.0	4.8	
t_{DIS}	$\overline{OE}$		1.0	5.3		4.7	1.0	4.3	

Notes:
1. See test circuit and waveforms, Figures 1 and 2.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, T_A = 25°C

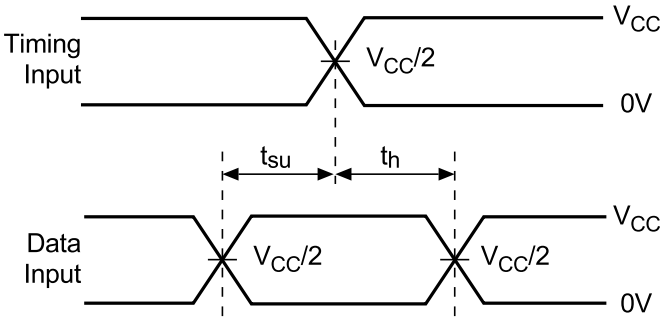
Parameter		Test Conditions	V_{CC} = 2.5V ±0.2V	V_{CC} = 3.3V ±0.3V	Units
			Typ.		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF, f = 10 MHz	62	60	pF
	Outputs Disabled		32	36	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5V ±0.2V

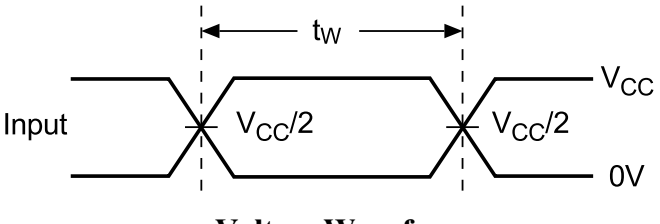


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZH}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

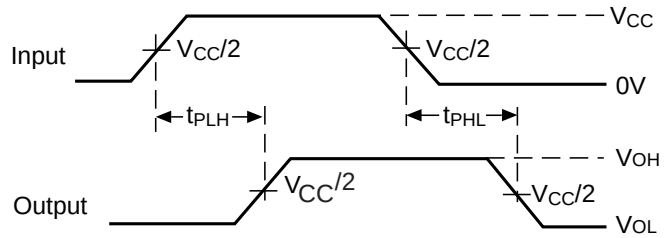
Load Circuit



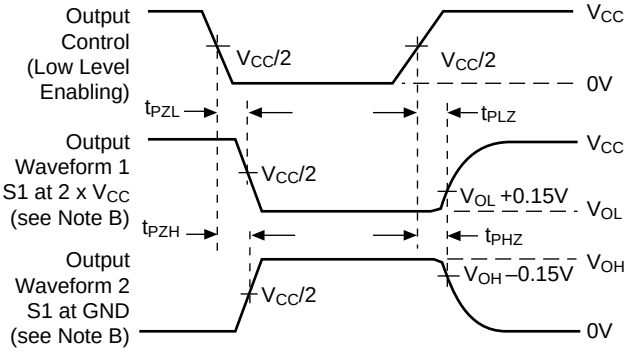
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



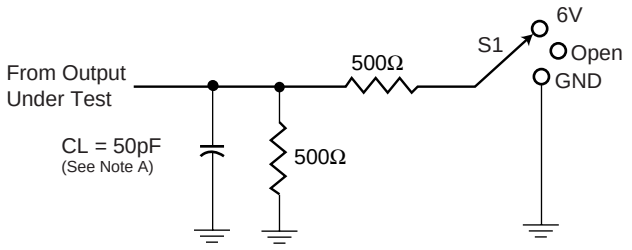
Voltage Waveforms
Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

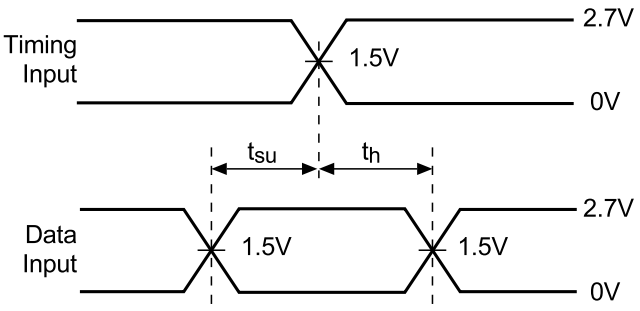
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7V and 3.3V ±0.3V

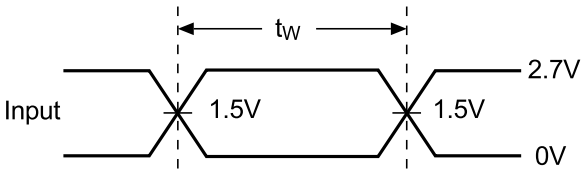


Load Circuit

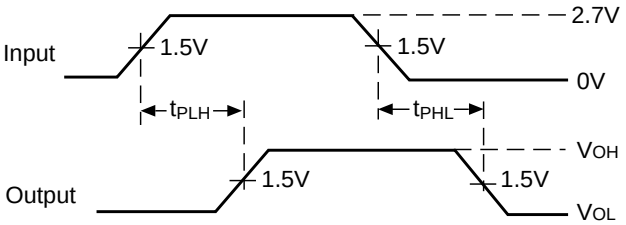
Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZH}	6V
t_{PHZ}/t_{PZH}	GND



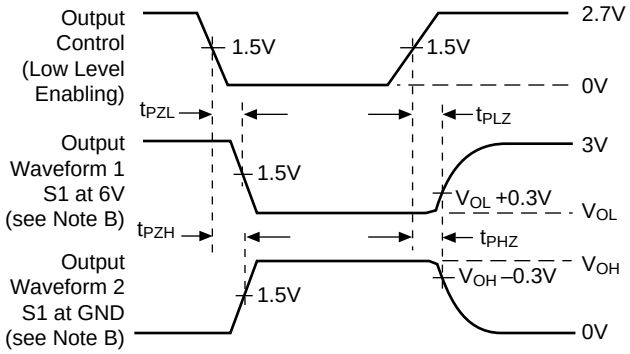
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 2. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}