I-Cube PSX Family Data Sheet

Features

- SRAM-based, In-system Programmable
- Switch Matrix
  - Non-Blocking
  - Programmable Bus Widths of 4, 8, 16 and 32 bits
  - Identical and Predictable Delays
  - One-to-One, One-to-Many and Many-to-One Connections
  - RapidConnect™ parallel interface for Fast, Incremental Switching of Buses in 12.5 ns
  - Bank Switching for Instantaneous Reconfiguration of Entire Switch Matrix
- I/O Ports
  - Individually Programmable as Input, Output or Bidirectional
  - For Each I/O Port, Clock, Clock Enable, Input Enable and Output Enable Can Be Selected Independently From A Large Pool of Common Control Signals
  - 16 mA Current Drive
  - Separated I/O Power Pins for Easy Interfacing to 3V/3.3V signals
- Clocked, Latched and Flow-through Dataflow Modes
  - 7.0 ns Port-to-Port Delay in Flow-through Mode
  - 133 MHz Clock Frequency
- 100% JTAG Compliant

Description

The PSX160, PSX128B and PSX96B are SRAM-based bus oriented switches with 160, 128 and 96 I/Os respectively. The devices are manufactured using a 0.6µm CMOS process and can be clocked up to 133 MHz.

The PSX devices are used in applications requiring dynamic switching, such as communication switches, network hubs and routers, image processing engines, file/video servers and multiprocessing shared-memory systems.

At the heart of PSX devices is a non-blocking, Switch Matrix. The lines in the Switch Matrix can be grouped and controlled as 4, 8, 16 or 32 signal busses. Any bus can be connected to one or more other busses. The Switch Matrix lines are connected to I/O Ports whose functional attributes are programmable.

The RapidConnect interface allows connections in the Switch Matrix to be changed quickly and incrementally. In addition, the dual configuration memory banks allow a new switch configuration to be loaded in the inactive bank and swap it in instantaneously. In either case, data integrity is maintained on all unchanged connections.

The PSX devices support an industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The same interface is also used for downloading the configuration bit stream into the PSX devices.

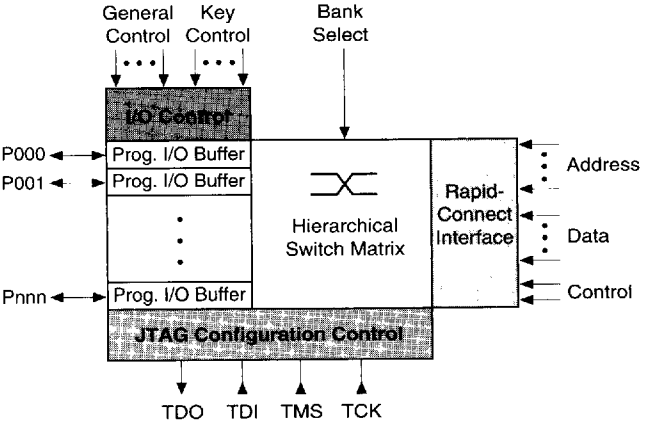


Figure 1: PSX Functional Block Diagram

Table of Contents

Architecture

PSX devices are SRAM-based bus-oriented switching matrices. The devices can be configured and controlled in-system by storing appropriate data into the internal SRAM cells and configuration registers. The main functional blocks of the device are the Hierarchical, Dual-Bank Switch Matrix, Programmable I/O Ports, I/O Control signal block, RapidConnect Switching Interface and a JTAG-based Configuration Controller.

The full-featured programmable I/O Ports are grouped into 4 (i. e. nibbles) for the purpose of switching. They can be further grouped into 8 (2 nibbles), 16 (4 nibbles) or 32-bit (8 nibbles) groups for byte, word and long word buses respectively. These port groups and their associated signal lines can be connected internally to other buses using the Switch Matrix. The I/O Port control signals such as clock, clock enable, input enable, and output enable are used to control the flow of data through the I/O Ports.

The JTAG-based serial configuration controller is used to configure the I/O Ports and Switch Matrix SRAM cells, thereby establishing the desired functional attributes for the I/O Ports and connections among them through the Switch Matrix.

The RapidConnect interface is used to directly address the SRAM cells controlling the switches allowing connections to be changed with a single write operation.

Hierarchical, Dual-bank Switch Matrix

The Switch Matrix is an x-y routing structure (or grid). Each horizontal signal trace is hardwired to a corresponding vertical signal trace as shown by the junction dots in Figure 2. An I/O Port pin connects to this horizontal-vertical trace pair through a programmable buffer. The PSX Switch Matrix has a nibble or 4-bit granularity; i.e. the wires in the Switch Matrix are combined as 4-bit buses or nibbles and switched as groups. Signal paths through the Switch Matrix are very well balanced, resulting in predictable and uniform pin-to-pin delays.

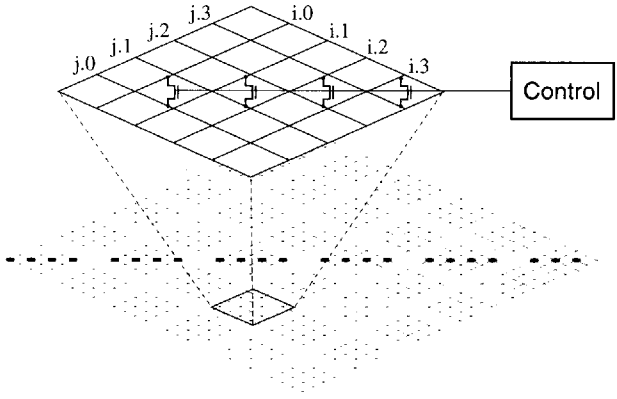


Figure 2: Switch Matrix and Nibble Switch

At the intersection of unique nibble buses are four pass transistors with a common control. These pass transistors allow a one-to-one connection of the corresponding bits between two nibbles (i.e., bit_0 in nibble i and bit_0 in nibble j). Bits within a nibble (i.e., bit_0 and bit_1 in nibble i) cannot be connected. Similarly, non-corresponding bits between the nibbles (i.e., bit_0 in nibble i and bit_2 in nibble j) cannot be connected either. Multicasting/broadcasting operation is supported by allowing one nibble to be connected to multiple other nibbles.

Hierarchical Control Structure

The pass transistors are controlled by a hierarchical (two-level) SRAM cell structure as shown in Figure 3. The two level structure allows the PSX device to switch 4-bit buses or 8, 16, 32-bit buses. To activate (turn ON) a group of 4 switches (nibble), two SRAM cells, one at Level 1 *and* one at Level 2 must be set. Notice from the figure that a Level-2 SRAM cell is common to two 4-bit buses, and therefore controls an 8-bit bus.

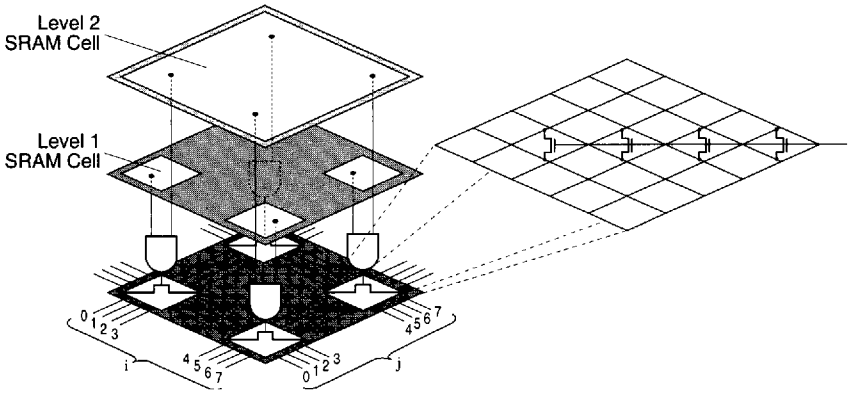


Figure 3: Two Level SRAM Cell Structure (8 x 8 Section of Switch Matrix is shown)

Switching of 4-Bit Buses

Switching of 4-bit buses is achieved by first setting the corresponding *Level-2* SRAM cell (statically, or during device initialization), and then writing to the appropriate *Level-1* SRAM cell(s) to make or break connections. If all I/O Ports are used for 4-bit switching, then all Level-2 SRAM cells are set to 1.

Switching of 8-Bit Buses

Switching of 8-bit buses is achieved by first setting the appropriate *Level-1* SRAM cells (statically, or during device initialization; see section "Level 1 Configuration"), and then writing to the appropriate *Level-2* SRAM cell to make or break an 8-bit bus connection. Notice from Figure 4 that four (2 x 2) Level-1 SRAM cells must be initialized to facilitate the switching of two 8-bit buses.

Switching of 16 and 32-Bit Buses

This is conceptually similar to switching of 8-bit buses. It is accomplished by first setting the appropriate *Level-1* SRAM cells (statically, or during device initialization), and then writing to *multiple Level-2* SRAM cells to make or break a 16 or 32-bit bus

connection. The RapidConnect Switching Interface, described in detail later, allows changing the contents of multiple Level-2 SRAM cells simultaneously. The multiple Level 2 SRAM cells are clustered as shown in Figure 4. A 2 x 2 cluster of Level-2 SRAM cells is simultaneously written (with the same data) to effect 16-bit switching, while a 4 x 4 cluster of Level-2 SRAM cells is simultaneously written (with the same data) to effect 32-bit switching. Notice from Figure 4 that 16 (4 x 4) and 64 (8 x 8) Level-1 SRAM cells must be initialized to facilitate the switching of two 16-bit and 32-bit buses respectively.

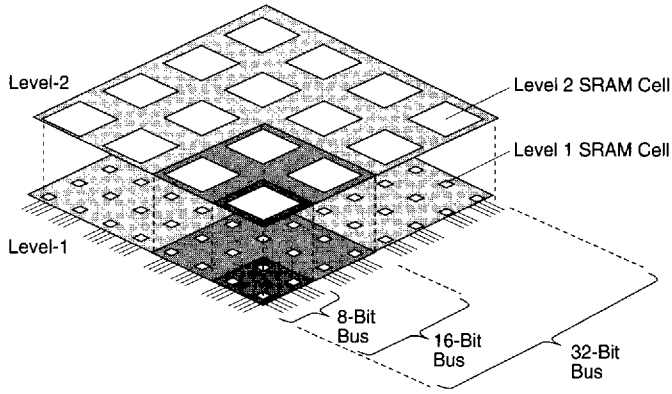


Figure 4: SRAM Clusters for Wider Bus Switching

Level-1 Configuration

In order to perform switching of 8, 16 and 32-bit buses, Level 1 SRAM cells must first be initialized. For each 8-bit switch, four (2 x 2) Level 1 SRAM cells must be programmed. For each 16-bit switch, sixteen (4 x 4) Level 1 SRAM cells must be programmed and for each 32-bit switch, 64 (8 x 8) Level 1 SRAM cells must be programmed. The typical Level 1 bit pattern is 1's along the diagonal and 0's in the remaining SRAM cells. Figure 5 illustrates some patterns for byte and word switching. The same concepts can be applied to 32-bit switching.

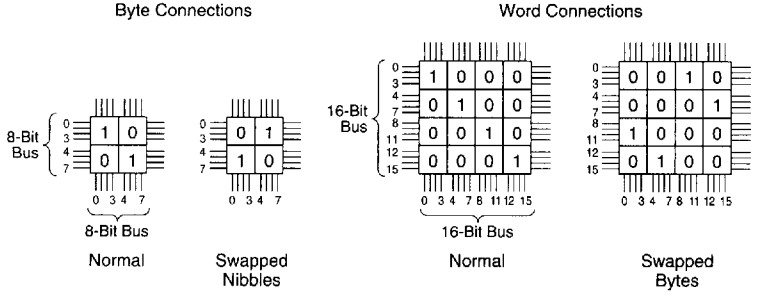


Figure 5: Level-1 SRAM cell Data for 8 and 16-bit Buses (can be extended to 32-bits)

For proper operation, no more than one Level-1 SRAM cell should be set for each cluster row. Likewise, no more than one Level-1 SRAM cell should be set for each

cluster column. As shown in the figure, normal bus switching is achieved with a diagonal pattern. Bus swapping is achieved with an offset "striped" diagonal pattern. Any swapping pattern is permitted as long as the "one cell per cluster row and one cell per cluster column" rule is followed.

I/O Port Grouping

I/O Ports are grouped in a predefined manner to form buses. I/O Ports for a given bus must be contiguous and as specified in section "I/O Port Assignment for Nibble, Byte, Word and Long Word Groups".

Dual Banks

The PSX family provides dual SRAM banks to enable changing to an entirely new Switch Matrix configuration instantaneously. As shown in Figure 6 the ON/OFF control for the pass transistors in the Switch Matrix is derived by multiplexing the data from two SRAM cells belonging to Bank 0 and Bank 1. A "Bank Select" pin on the device selects the *controlling* or *active* SRAM bank. The contents of the other (*inactive*) bank can be changed using the RapidConnect interface, described later, without affecting the Switch Matrix configuration that is active. When the required changes to the inactive bank are completed, the Bank Select pin can be used to toggle the active bank.

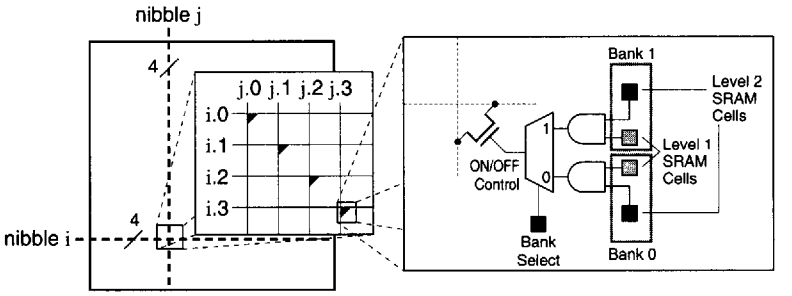


Figure 6: Switch Matrix Control

Note that the contents of the active bank can also be changed using either the RapidConnect or the JTAG interfaces. In doing so the Switch Matrix connections change as soon as the configuration data is written to the SRAM cells. The integrity of other connections defined by the active bank are not affected. This is useful when the Switch Matrix connections are changed one at a time.

Programmable I/O Port

Each signal line in the Switch Matrix is connected to a programmable I/O Port. The functional attributes of I/O Ports are individually programmable. The I/O Port attributes include its signal direction (In, Out or Bidirectional), data flow mode (flow through, registered or latched), and pull-up current. Figure 7 shows the structure of the programmable I/O Port for PSX. Also programmable are the sources for the four control signals: clock, clock enable, input enable, and output enable. The sources of these control signals are later described in the section on "I/O Control Signals".

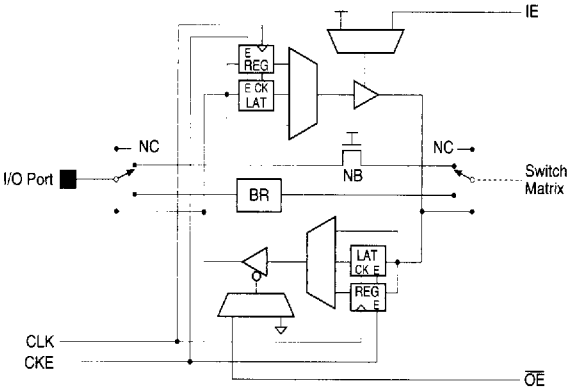
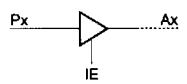
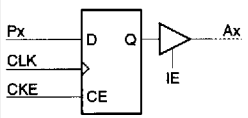
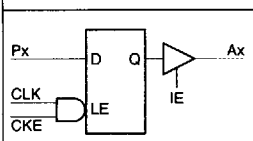
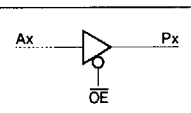
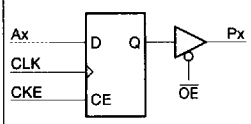
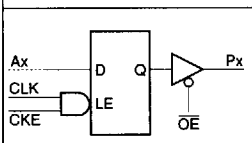
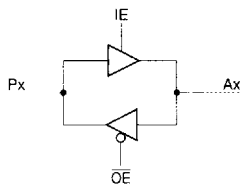
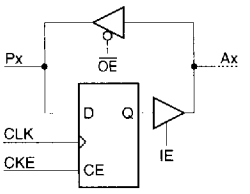
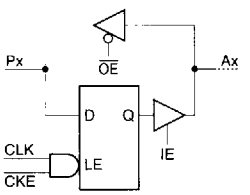
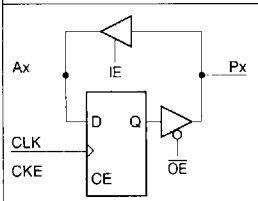
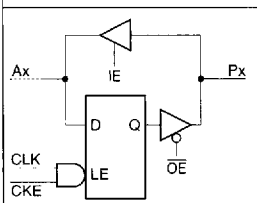
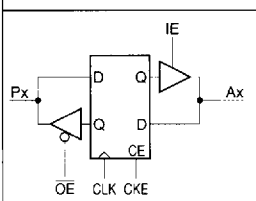


Figure 7: Programmable I/O Port Buffer

I/O Port Functional Modes

Table 1 describes the various modes of the I/O Port and the mnemonic used by I-Cube Development System Software. Signals A_X and P_X in the table refer to the Switch Matrix (array) line and I/O Port pin respectively.

Symbol	I/O Port Function	Mnemonic
	**Input** - The external signal is buffered from the I/O Port pin to the corresponding Switch Matrix line. In this mode an optional input enable (IE) can be selected. Either polarity can be selected for IE. The default level is a logic 1.	IN
	**Registered Input** - The external signal at the I/O Port pin is registered by an edge-triggered flip-flop within the I/O Port. A clock source is required in this mode. Either edge of CLK can be selected. The default for CLK is rising edge. A clock enable (CKE) and input enable (IE) are also available but not required. Either polarity can be selected for IE and CKE. The default level for IE and CKE is a logic 1. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	RI
	**Latched Input** - The external signal at the I/O Port pin is latched by a level-sensitive flip-flop within the I/O Port. A latch enable source is required in this mode. The latch enable source is composed of CLK and CKE, and at least one must be specified. An input enable (IE) is also available but not required. Either polarity can be selected for CLK, CKE and IE. The default level for all three is a logic 1. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	LI
	**Output** - The internal signal is buffered from the corresponding Switch Matrix line to the I/O Port pin. In this mode an optional output enable ($\overline{OE}$) can be selected. Either polarity can be selected for $\overline{OE}$. The default level is a logic 0.	OP
	**Registered Output** - The internal signal on the Switch Matrix line is registered by an edge-triggered flip-flop within the I/O Port. A clock source is required in this mode. Either edge of CLK can be selected. The default for CLK is rising edge. A clock enable (CKE) and output enable ($\overline{OE}$) are also available but not required. Either polarity can be selected for CKE and $\overline{OE}$. The default level for CKE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	RO
	**Latched Output**- The internal signal on the Switch Matrix line is latched by a level-sensitive flip-flop within the I/O Port. A latch enable source is required in this mode. The latch enable source is composed of CLK and CKE, and at least one must be specified. An output enable ($\overline{OE}$) is also available but not required. Either polarity can be selected for CLK and CKE. The default level for both is a logic 1. Either polarity can be selected for $\overline{OE}$. The default level is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	LO

Symbol	I/O Port Function	Mnemonic
	**Bidirectional Transceiver** - In this mode, the I/O buffer acts as a bidirectional transceiver between the I/O Port pin and the corresponding Switch Matrix line. This mode requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for each but the default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. When the same source (with default polarities) is used for IE and $\overline{OE}$, it effectively acts as a direction control. When the same control signal (with one polarity inverted) is used for IE and $\overline{OE}$, it effectively acts as a Bus Repeater (BR) (see below) when both are enabled, and as No Connect (NC) when neither is enabled.	BT
	**Bidirectional Transceiver with Registered Input** - This mode combines Registered Input (RI) and output buffer (OP). A clock source is required in this mode. Either edge of CLK can be selected. The default for CLK is rising edge. A clock enable (CKE) is available but not required. Either polarity can be selected. The default level for CKE is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for each. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	BT&RI
	**Bidirectional Transceiver with Latched Input** - This mode combines Latched Input (LI) and output buffer (OP). A latch enable source is required in this mode. The latch enable source is composed of CLK and CKE, and at least one must be specified. Either polarity can be selected for CLK and CKE. The default level for both is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for IE and $\overline{OE}$. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	BT&LI
	**Bidirectional Transceiver with Registered Output** - This mode combines Registered Output (RO) and input buffer (IN). A clock source is required in this mode. Either edge of CLK can be selected although the default is rising edge. A clock enable (CKE) is available but not required. Either polarity can be selected but the default level is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for IE and $\overline{OE}$. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	BT&RO
	**Bidirectional Transceiver with Latched Output** - This mode combines Latched Output (LO) and input buffer (IN). A latch enable source is required in this mode. The latch enable source is composed of CLK and CKE. A t least one must be specified. Either polarity can be selected for CLK and CKE. The default level for both is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for IE and $\overline{OE}$. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	BT&LO
	**Bidirectional Transceiver with Registered I/O**- This mode is a combination of Registered Input (RI) and Registered Output (RO). A clock source is required in this mode. Either edge of CLK can be selected. The default is rising edge. A clock enable (CKE) is available but not required. Either polarity can be selected for CKE. The default level is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for IE and $\overline{OE}$. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flops is unknown after hardware reset (TRST* = 0).	BT&RI&RO

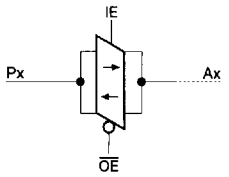
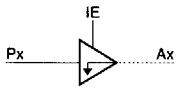
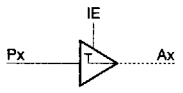
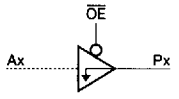
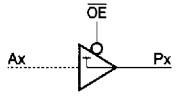
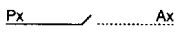
Symbol	I/O Port Function	Mnemonic
	Other BT Modes- Other combinations of I/O Port modes (not covered in this table) are less likely but can be used. The mnemonic is BT [&RI | &LI] [&RO | &LO], where the specification inside the brackets "[ ]" is optional and "|" stands for either or. Insure that control signal requirements are met. In these modes, the output of the flip-flops is unknown after hardware reset (TRST* = 0).	
	**Bus Repeater** - In the Bus Repeater mode, the I/O Port behaves as a wire (with a non-zero propagation delay). This unique feature (patented by I-Cube) incorporates a self-sensing circuit to determine signal direction and does not require a direction control signal. When multiple I/O Ports, configured as "Bus Repeater", are connected together through the Switch Matrix to form a single internal node, a signal appearing at any one of the I/O Ports gets repeated (or broadcast) to other I/O Ports. The Bus Repeater mode requires a pull-up current source (see section on "Programmable Pull-Up Current") to operate properly. For more details, refer to the Technical Note: "The Bus Repeater Mode" in the "Programmable Switching and Interconnect Devices - Applications Handbook".	BR
	**Array Side Force 0** - In this input mode, the Switch Matrix line is forced low (logic 0), regardless of the signal on the corresponding I/O Port. In this mode an optional input enable (IE) can be selected. Either polarity can be selected for IE. The default level is a logic 1.	A0
	**Array Side Force 1** - In this input mode, the Switch Matrix line is forced high (logic 1), regardless of the signal on the corresponding I/O Port. In this mode an optional input enable (IE) can be selected. Either polarity can be selected for IE. The default level is a logic 1.	A1
	**Pin Side Force 0** - In this output mode, the I/O Port pin is forced low (logic 0), regardless of the signal on the corresponding Switch Matrix line. In this mode an optional output enable ($\overline{OE}$) can be selected. Either polarity can be selected for $\overline{OE}$. The default level is a logic 0.	F0
	**Pin Side Force 1** - In this output mode, the I/O Port pin is forced high (logic 1), regardless of the signal on the corresponding Switch Matrix line. In this mode an optional output enable ($\overline{OE}$) can be selected. Either polarity can be selected for $\overline{OE}$. The default level is a logic 0.	F1
	**Non-Buffered** - In this mode, the I/O Port pin is directly connected to the corresponding line in the Switch Matrix through a pass transistor, bypassing the buffer. This mode is not controlled by any of the four control signals (CLK, CKE, IE, and $\overline{OE}$) and is not used for passing digital signals.	NB
	**No Connect** - In this mode, the I/O Port pin is isolated from the Switch Matrix. This is done by tristating both the input and output part of the I/O buffer. Upon hardware reset (TRST* = 0), all I/O Ports are automatically configured in this mode No Connect (NC).	NC

Table 1: Summary of Programmable I/O Attributes for PSX Devices

Legend:

A_X - Switch Matrix Signal
P_X - I/O Port pin Signal
IE - Input Enable
$\overline{OE}$ - Output Enable
CLK - Clock
CKE - Clock Enable

Pin and Array side Trickle Current

N-channel devices are used as a trickle current source (nominally 10μA) I_{PT}, on the pin side and Switch Matrix side for each I/O Port. Upon reset, these current sources are turned ON. They can be turned OFF by configuring the I/O Port to do so.

Programmable Pull-up Current

As shown in Figure 8, the I/O Port contains several pull-up devices. The normal pull-up current is supplied by an n-channel device which is controlled by internally generated control signals.

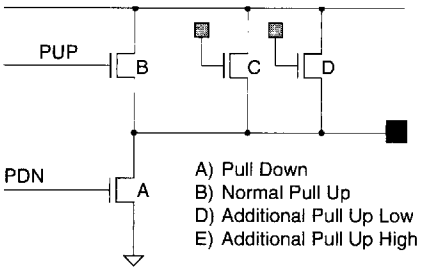


Figure 8: PSX Output Driver and Pull-Up Current

An additional static pull-up current (I_{PU-WK}) or (I_{PU-SG}) can be programmed at each I/O Port pin. This additional pull-up current is primarily used for the Bus Repeater (BR) mode, but its use is not restricted to that mode alone.

I/O Control Signals

The PSX family has a flexible control structure that gives the user complete control over the behavior of each I/O Port. As shown in Figure 9 and described below, clock (CLK), clock enable (CKE), input enable (IE) and output enable ($\overline{OE}$) for each I/O Port can be selected from two different sets of control inputs. The control polarity can be individually selected.

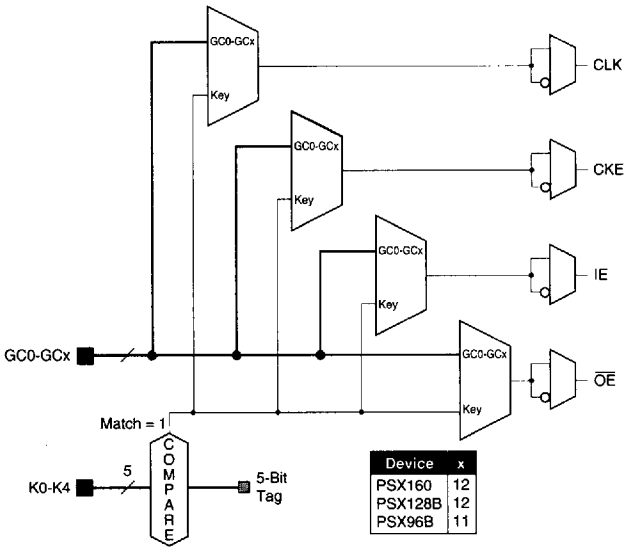


Figure 9: I/O Control

General Control

I/O Ports can be individually programmed to use a signal from a large pool of dedicated control pins called General Control (GC x) on the device.

Key Controls

Each I/O Port contains a 5-bit *tag* which can be programmed with a unique value. A comparator in each I/O Port continually compares the assigned tag value with the signals present on the Key Control pins. The output of the comparator, which produces a logic 1 on a match, can be selected as a control signal. The Key Control is intended for use with level sensitive signals such as IE, $\overline{OE}$, CKE (in registered modes only). If Key Control is used in situations where a short glitch on the internal "Match" signal is unacceptable (i.e. using the Key Port for CLK in *registered* modes and CLK and/or CKE in *latched* modes), it is recommended that one of the Key Port pins be used as a qualifier and switched after the other Key Port pins have stabilized to prevent glitches on the internal "Match" signal. Note that when the key control is used as an output enable, which is low active, a match will disable the I/O Port driver, unless a reverse polarity is selected for output enable.

I/O Port Assignment for Nibble, Byte, Word and Long Word Groups

The following table shows the assignment of I/O Ports for nibble, byte, word and long word groups. The PSX128B and PSX96B are "bond out" versions of the PSX160. Table 2 shows the I/O Port pins that are made available on the PSX128B and PSX96B.

Long Word Number	Word Number	Byte Number	Nibble Number	PSX160 I/O Port Numbers	PSX128B I/O Port Numbers	PSX96B I/O Port Numbers
0	0	0	0	P000 - P003	P000 - P003	P000 - P003
			1	P004 - P007	P004 - P007	P004 - P007
		1	2	P008 - P011	P008 - P011	P008 - P011
			3	P012 - P015	P012 - P015	P012 - P015
	1	2	4	P016 - P019	P016 - P019	P016 - P019
			5	P020 - P023	P020 - P023	P020 - P023
		3	6	P024 - P027	P024 - P027	P024 - P027
			7	P028 - P031	P028 - P031	P028 - P031
1	2	4	8	P032 - P035	P032 - P035	P032 - P035
			9	P036 - P039	P036 - P039	P036 - P039
		5	10	P040 - P043	P040 - P043	P040 - P043
			11	P044 - P047	P044 - P047	P044 - P047
	3	6	12	P048 - P051	P048 - P051	P048 - P051
			13	P052 - P055	P052 - P055	P052 - P055
		7	14	P056 - P059	P056 - P059	P056 - P059
			15	P060 - P063	P060 - P063	P060 - P063
2	4	8	16	P064 - P067	Not Available	Not Available
			17	P068 - P071		
		9	18	P072 - P075		
			19	P076 - P079		
	5	10	20	P080 - P083		
			21	P084 - P087		
		11	22	P088 - P091		
			23	P092 - P095		
3	6	12	24	P096 - P099	P096 - P099	
			25	P100 - P103	P100 - P103	
		13	26	P104 - P107	P104 - P107	
			27	P108 - P111	P108 - P111	
	7	14	28	P112 - P115	P112 - P115	
			29	P116 - P119	P116 - P119	
		15	30	P120 - P123	P120 - P123	
			31	P124 - P127	P124 - P127	
4	8	16	32	P128 - P131	P128 - P131	P128 - P131
			33	P132 - P135	P132 - P135	P132 - P135
		17	34	P136 - P139	P136 - P139	P136 - P139
			35	P140 - P143	P140 - P143	P140 - P143
	9	18	36	P144 - P147	P144 - P147	P144 - P147
			37	P148 - P151	P148 - P151	P148 - P151
		19	38	P152 - P155	P152 - P155	P152 - P155
			39	P156 - P159	P156 - P159	P156 - P159

Table 2: I/O Port Assignment for Nibble, Byte, Word and Long Word

RapidConnect Switching Interface

The RapidConnect Switching Interface allows the Switch Matrix connections to be changed quickly by providing direct write access to the Switch Matrix SRAM cells. The RapidConnect interface shown in Figure 10 is a write only interface. It uses address, data and control signals to write to the Switch Matrix SRAM cells.The Switch Matrix SRAM cells are addressed as a two dimensional matrix, requiring a Row Address and Column Address to uniquely identify the SRAM cell(s) being written to.

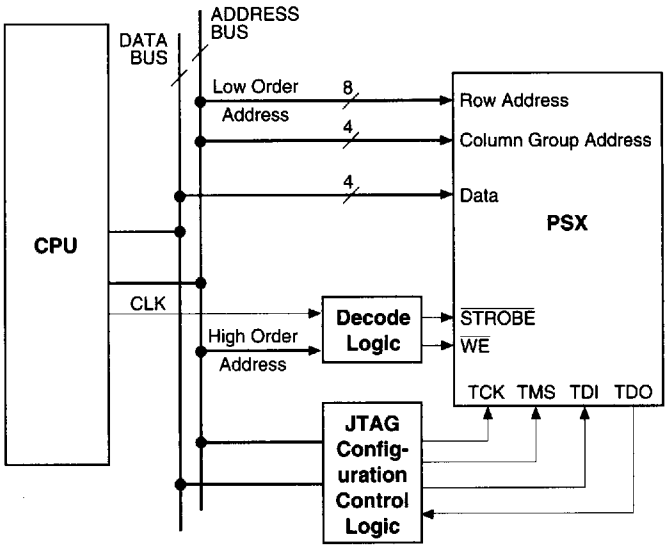


Figure 10: PSX RapidConnect System Interface

On the PSX160, PSX128B and PSX96B devices, the RapidConnect interface consists of an 8-bit Row Address, RA[7:0], 4-bit Column Group Address, CA[3:0], 4-bit data bus, DATA[3:0], Write Enable, $\overline{WE}$ and a write strobe, $\overline{STROBE}$.

The Row Address, Column Group Address and DATA values for the different RapidConnect operations are calculated as shown in the section "RapidConnect Address Computation".

In a typical system, an embedded processor will compute the required Row Address, Column Group Address and Data values and apply them to the PSX device. Alternatively, these values could be computed before hand using the I-Cube supplied software, and stored in a lookup table.

Upon power-up all Switch Matrix SRAM cells are cleared, all I/O Ports are set to NC and the RapidConnect mode is enabled.

JTAG-based Configuration Controller

In the PSX devices, the I/O attributes and Switch Matrix connections can be programmed using the JTAG serial bus. Additionally, the RapidConnect Switching Interface, used for dynamically changing Switch Matrix connections, can be enabled or disabled using the JTAG serial bus.

In most cases, the user does not need to know the details of the JTAG protocol. The I-Cube supplied software will automatically generate the necessary bit stream from a higher-level textual description of the required configuration.

JTAG Interface

The JTAG interface is a serial interface and uses four pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). TCK is used to clock data in and out of TDI and TDO. TMS, in conjunction with TDI implements a state machine that controls the various operations of the JTAG protocol. In addition, the device reset signal (TRST*) is used to reset both the device and the JTAG controller.

I/O Port Configuration

I/O Port configuration is accomplished by loading the appropriate bit stream into the programming registers present at each I/O Port. Only the JTAG interface can be used to load these programming registers.

Switch Matrix Configuration

The contents of the SRAM cells controlling Switch Matrix connections can be modified using either the JTAG interface or the RapidConnect interface.

The JTAG serial interface is used to load the data, one word at a time into the SRAM cells in the Switch Matrix. The RapidConnect mode, on the other hand, provides direct write access to SRAM cells in the Switch Matrix. When using the JTAG interface to change the Switch Matrix configuration, the RapidConnect mode must first be disabled by resetting the RapidConnect Enable flag in the Mode Control Register (see the section "Miscellaneous Details").

Mode Control Register Configuration

The PSX device contains a Mode Control Register. Certain bits in the register, used to store certain user flags such as RapidConnect Enable and other flags which must be set correctly for the proper functioning of the device, can be changed using the JTAG interface.

Miscellaneous Details

Device Reset

To ensure proper operation, the device reset pin, TRST* must be held low during power up. The recommended reset circuitry is shown in Figure 11.

The device can be reset by pulsing TRST* low or by shifting in the JTAG instruction reserved for device reset (this is different from the JTAG reset instruction, which resets only the JTAG state machine). When the device is reset, the I/O Ports return to their default state of No Connect (NC), the Switch Matrix SRAM cells are cleared and the RapidConnect mode is enabled.

The PSX device is ready for configuration as soon as it comes out of reset. The edge and level-sensitive flip-flops in the I/O Port buffers are not cleared by device reset and will have unknown output values after reset.

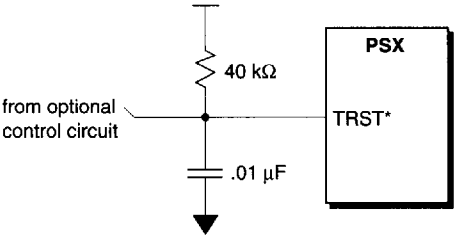


Figure 11: Reset Circuit

Mode Control Register

The PSX device contains a 16-bit Mode Control Register. It stores the RapidConnect Enable flag and certain other flags which must be set correctly for the proper functioning of the device.

Mixed Voltage Operation

There are three distinct sources for power on the PSX device. The first one called V_{DD} is a 5V source and is used to power the device core, including the Switch Matrix SRAM cells, I/O Port logic (excluding the I/O pin driver buffer), I/O Control Logic, JTAG logic (except TDO pin driver) and other circuitry. The I/O buffer drivers are powered by either V_{DD}.PAD1 or V_{DD}.PAD2. Table 6 provides the details on power source assignment. V_{DD}.PAD1 and/or V_{DD}.PAD2 can be connected to either a 5V or 3V supply. This makes it easy to interface these device to 5V or 3V logic level. The TDO pin is driven by V_{DD}.PAD2.

RapidConnect Address Computation

The 160 I/O Ports on the PSX160 can be configured into 40 nibbles, 20 bytes, 10 words or 5 long words for switching. On the PSX128B and PSX96B, bondout versions of the PSX160, 128 and 96 I/O Ports are externally accessible. See the "PSX Pin Summary" section for details. Table 3 shows how to compute the RapidConnect addresses for changing connections. Table 3 also shows the data values for unicast and multicast and clear operations. RA[7], which is not shown in the tables, indicates the configuration bank for the write operation.

Mode	Operation	Row Address RA[6:0]	Column Group Address CA[3:0]	DATA[3:0] For Make	DATA[3:0] For Break
U N I C A S T	Change Connection Between Nibbles i & j [0 ≤ i < j ≤ 39]	RA[6] = "0"; RA[5:0] =BIN(i)[5:0][2]	CA[3:0] = BIN(j)[5:2]	DECODE[3] (BIN(j)[1:0])	"0000"
	Change Connection Between Bytes i & j [0 ≤ i < j ≤ 19]	RA[6] = "1"; RA[5:1] = BIN(i)[4:0] RA[0] = "0"	CA[3:0] = (BIN(j)[4:1]	if BIN(j)[0] ="0" then "0011" else "1100"	"0000"
	Change Connection Between Words i & j [0 ≤ i < j ≤ 9]	RA[6] = "1"; RA[5:2] = BIN(i)[3:0] RA[1:0] = "01"	CA[3:0] = BIN(j)[3:0]	"1111"	"0000"
	Change Connection Between LWords i & j [0 ≤ i < j ≤ 4]	RA[6:3] = "1101"; RA[2:0] = BIN(i)[2:0]	CA[3:1] = BIN(j)[2:0] CA[0] = don't care	"1111"	"0000"
M U L T I C A S T	Change Connection Between Nibbles i & j [0 ≤ i < j ≤ 39]	RA[6] = "0"; RA[5:0] = BIN(j)[5:0]	CA[3:0] = BIN(j)[5:2]	DATA[3:0][4] ORed with DECODE(BIN(j)[1:0])	DATA[3:0] ANDed with INVERTed DECODE(BIN(j)[1:0])
	Change Connection Between Bytes i & j [0 ≤ i < j ≤ 19]	RA[6] = "1"; RA[5:1] = BIN(i)[4:0] RA[0] = "0"	CA[3:0] = BIN(j)[4:1]	if BIN(j)[0] = "0" then DATA[3:0] ORed with "0011" else DATA[3:0] ORed with "1100"	if BIN(j)[0] = "0" then DATA[3:0] ANDed with "1100" else DATA[3:0] ANDed with "0011"
	Change Connection Between Words i & j [0 ≤ i < j ≤ 9]	RA[6] = "1"; RA[5:2] = BIN(i)[3:0] RA[1:0] = "01"	CA[3:0] = BIN(j)[3:0]	"1111"	"0000"
	Change Connection Between LWords i & j [0 ≤ i < j ≤ 4]	RA[6:3] = "1101"; RA[2:0] = BIN(i)[2:0]	CA[3:1] = BIN(j)[2:0] CA[0] = don't care	"1111"	"0000"
C L R	Clear Switch Matrix Configuration Cells (Break all connections)	"1101111"	Don't Care	Don't Care	Don't Care

Table 3: Making / Braking a Connection

(1) For PSX96B, RA[4] is not available externally, but is internally forced to a"0". For PSX96B, all legal Row Address calculations should result in RA[4] = "0" or "don't care"
(2) BIN function is the n-bit binary equivalent value.
(3) DECODE function decodes a two-bit binary value, i.e., DECODE(00) = "0001", DECODE(01) = "0010", DECODE(10) = "0100" & DECODE(11) = "1000".
(4) DATA[3:0] is the previous value used in a make/break operation involving i and another k that is in the same "4-column" group, i.e., INTEGER(j/4) = INTEGER(k/4).

In System Configuration Using JTAG-based Configuration Controller

The primary configuration mode for the PSX devices is the JTAG-based serial mode. The JTAG-based serial configuration mode allows the user to initialize the device, configure the I/O Ports and establish connections through the Switch Matrix. In addition, the RapidConnect interface can be used for changing Switch Matrix connections dynamically and quickly. Even if the user is planning to use RapidConnect for dynamic switching, the device must first be initialized using JTAG.

Configuring the device using JTAG involves two steps. In the first step, the user generates the bit stream, which, when loaded into the device, establishes the desired configuration. Two different software options - off-line and embedded bit stream generation - are available to accomplish this task, depending on the target application. The second step is the actual downloading of the bit stream into the device. The downloading circuitry can take on different forms, depending on the target application.

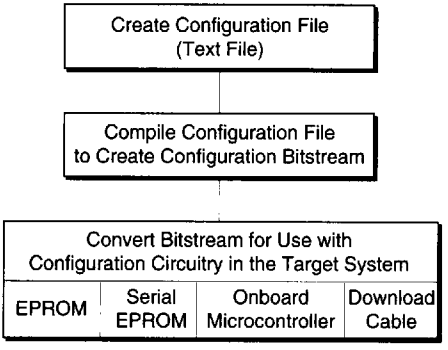


Figure 12: Off-line Bit Stream Generation

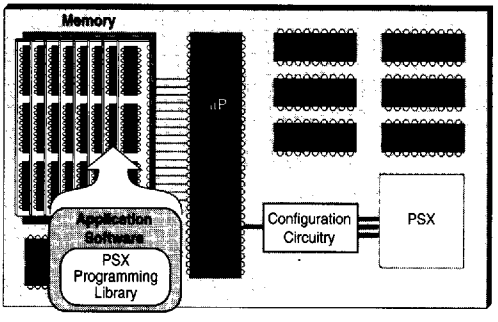


Figure 13: Embedded Bit Stream Generation

Bit Stream Generation

The configuration bit stream can be generated off-line or in-system by an embedded CPU using one of the following methods:

- By using I-Cube Development System Software products IDS100 or IDS 200.
- By using I-Cube's "Programming Library for PSX Devices" software product IDS550, and an embedded processor.
- By user written code based on the information provided in the "PSX Register-level Programming Users Guide".

If the bit stream is generated off-line then, depending on the application, it is either stored in non-volatile memory or directly downloaded from a host processor such as a PC connected to the target hardware.

The software used for off-line generation accepts a text file describing the desired configuration - connections between different I/O Ports and functional attributes of each I/O Port - and generates a file containing the bit stream. This software is a part of the development system available on PC and Sparcstation.

Bit Stream Downloading

The bit stream can be downloaded into the PSX device using several different hardware schemes. The choice depends on the end application. All these schemes use the standard JTAG protocol and timing. As per the JTAG protocol, the clock signal (TCK) must be supplied externally.

If the target hardware is controlled by a computer such as a PC, the parallel port on the computer can be used to download the bit stream. I-Cube provides a software utility to perform the downloading. Under this scheme, the necessary data for TDI and TMS pins as well as the (software generated) TCK clock signal are sent over the parallel port.

An on-board EPROM or E^2PROM, in either bit-wide or byte-wide configuration, or a serial E^2PROM can be used to store the bit stream. Using minimal external logic, the bit stream stored in one of these devices can be downloaded into the PSX device(s) over the TDI and TMS pins, with the TCK pin used for synchronization. The clock signal for the TCK pin is generated by the external logic.

If the target system has an on-board microcontroller, the bit stream data can be read from memory (either an EPROM or SRAM) and downloaded into the PSX device(s) using 3 I/O pins on the microcontroller to generate the required TDI, TMS and TCK signals. For real-time applications, the microcontroller/microprocessor can generate the bit stream (using the I-Cube supplied software library or user written code) and then download it into the PSX device in a single operation.

The actual time required to download the configuration bit stream and program a PSX device depends on the device(s) used, the user's specific configuration pattern, and JTAG clock frequency. Table 4 shows the number of JTAG cycles and configuration time required for some typical operations. The size of the memory (number of bits) required is two times the number of JTAG cycles.

Configuration Time and Bit Stream Size

Table 4 shows the JTAG cycle counts, configuration times and bit stream size for some typical operations.

Operation	PSX160			PSX128B			PSX96B		
	# of JTAG Cycles	Config. Time	Bit-stream Size	# of JTAG Cycles	Config. Time	Bit-stream Size	# of JTAG Cycles	Config. Time	Bit-stream Size
JTAG Reset Sequence	5	250 ns	10	5	250 ns	10	5	250 ns	10
Set ALL I/O Ports to their default value	27	1.35 µs	54	27	1.35 µs	54	27	1.35 µs	54
Enable or Disable RapidConnect	42	2.1 µs	84	42	2.1 µs	84	42	2.1 µs	84
Change IOB attributes of ONE I/O Port	70	3.5 µs	140	70	3.5 µs	140	70	3.5 µs	140
Change IOB attributes of ALL I/O Ports	160 * 70 or 11,200	0.56 ms	22,400	128 * 70 or 8,960	0.448 ms	17,920	96 * 70 or 6,720	0.336 ms	13,440
Reset JTAG Controller + Reset ALL I/O + Clear ALL SRAM cells in BOTH banks (This is equivalent to a hardware reset using TRST*)	5 + 27 + 2 * 27 or 86	4.3 µs	172	5 + 27 + 2 * 27 or 86	4.3 µs	172	5 + 27 + 2 * 27 or 86	4.3 µs	172
Connect or disconnect two nibbles, assumes second -level SRAM cells are set to a correct value. This operation involves writing to one first-level SRAM word in ONE bank	66	3.3 µs	132	66	3.3 µs	132	66	3.3 µs	132
Connect or disconnect two bytes, words or long words, assumes the first-level SRAM cells are set to a correct value. This operation involves writing to one second-level SRAM word in ONE bank	66	3.3 µs	132	66	3.3 µs	132	66	3.3 µs	132
Clear ALL SRAM cells (first and second-level) in ONE bank	27	1.35 µs	54	27	1.35 µs	54	27	1.35 µs	54
Clear ALL SRAM cells (first and second-level) in BOTH banks	2 * 27 or 54	2.7 µs	108	2 * 27 or 54	2.7 µs	108	2 * 27 or 54	2.7 µs	108
Completely Configure the Device (All I/O and One Bank)	approx. 16,000	0.8 ms	approx. 4 kB	approx. 13,000	0.65 ms	approx. 3.25 kB	approx. 10,000	0.5 ms	approx. 2.5 kB
Completely Configure Entire Device (All I/O and Both Banks)	approx. 20,000	1.0 ms	approx. 5 kB	approx. 17,000	0.85 ms	approx. 4.25 kB	approx. 13,000	0.65 ms	approx. 3.25 kB

Table 4: Number of JTAG Cycles and Configuration Time (using a 20 MHz JTAG Clock)

Configuring Multiple PSX Devices

The JTAG-based controller allows a single device or multiple PSX devices connected in a chain to be configured in a single operation. For multiple device configuration, the pins are connected as shown in Figure 14.

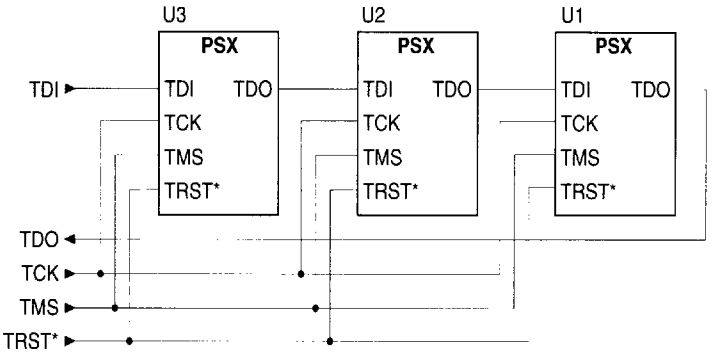


Figure 14: Configuring Multiple PSX Devices

During the initial configuration sequence, the internal controllers on all PSX devices are first brought to their reset state by pulsing the TRST* reset pin low. This is followed by the actual configuration bit stream, which is downloaded into the PSX devices over the TDI and TMS pins.

Pin Summary

PSX160	PSX128B	PSX96B [1]	DIR	Description
P000 - P159	P000 - P063, P96 - P159 [P064 - P095 are not available]	P000 - P063, P128 - P159 [P064 - P127 are not available]	I/O	**I/O Ports** Addressable as nibbles, bytes, words and Long Words
GC0 - GC12	GC0 - GC12	GC0 - GC11	I	**General Purpose Control Pins** Used for Clock, Clock Enable, Input Enable and Output Enable Signals
K0 - K4	K0 - K4	K0 - K4	I	**Key Control Pins** Additional Control Pins Used to Generate CLK, CKE, IE and $\overline{OE}$ Signals. Refer to Section "I/O Control Signals".
RA0 - RA7	RA0 - RA7	RA0 - RA3, RA5 - RA7	I	**RapidConnect Control Pins** Row Address Vector
CA0 - CA3	CA0 - CA3	CA0 - CA3	I	Column Group Address Vector
DATA0 - DATA3	DATA0 - DATA3	DATA0 - DATA3	I	Data Bus
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	I	RapidConnect Write Enable
$\overline{STROBE}$	$\overline{STROBE}$	$\overline{STROBE}$	I	RapidConnect Write Strobe
$\overline{BANK}$	$\overline{BANK}$	$\overline{BANK}$	I	Active Bank Select
$\overline{TRST}$*	$\overline{TRST}$*	$\overline{TRST}$*	I	Hardware Reset Refer to Section on Device Reset
TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	I O	**JTAG Pins** for downloading the serial configuration bitstream
V_{DD}.PAD1	V_{DD}.PAD1	V_{DD}.PAD1	P	**Power & Ground Pins** Power Pins for Group 1 I/O Buffer Drivers
V_{DD}.PAD2	V_{DD}.PAD2	V_{DD}.PAD2	P	Power Pins for Group 2 I/O Buffer Drivers
V_{DD}	V_{DD}	V_{DD}	P	Power Pins for on-chip circuitry and Pins other than I/O Buffer Drivers
V_{SS}	V_{SS}	V_{SS}	P	Ground Pins

Table 5: Pin Summary

Note:
(1) RA4 is not available externally on the PSX96B. It is connected to V_{SS} internally.

Supply Voltage	Pins Powered by Supply Voltage
V_{DD}	RA[0:7], CA[0:3],DATA[0:3], GC[0:12], KEY[0:4], $\overline{WE}$, $\overline{STROBE}$, BANK, TDI, TMS, TCK, $\overline{TRST}$*,
V_{DD}.PAD1	P000:P015, P024:P039, P056:P071, P088:P103, P120:P135
V_{DD}.PAD2	P016:P023, P040:P055, P072:P087, P104:P119, P136:P159, TDO

Table 6: Source Voltages for Different Pins

Electrical Specifications

Unless otherwise stated, the specifications apply to all PSX devices.

Absolute Maximum Rating (1)

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	-0.3 to +7.0	V
V_{DD}.PAD1,2	Supply Voltage for I/O Buffer Driver	-0.3 to +7.0	V
V_{IN} (2)	Input Voltage	-0.3 to (V_{DD}.PAD + 0.3)	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{SINK}	Sink Current per Port Pin	- 150	mA

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	4.75 to 5.25	V
V_{DD}.PAD1,2	Supply Voltage for I/O Buffer Driver (V_{DD}.PAD1 and V_{DD}.PAD2 can operate at different voltages)	4.75 to 5.25 or 2.7 to 3.3	V V
T_A	Operating Temperature	0 to +70	°C

Capacitance (3)

Symbol	Parameter	PSX160		PSX128B		PSX96B		Units
		Min	Max	Min	Max	Min	Max	
C_{IN}	Input Capacitance (JTAG pins)	-	8	-	8	-	8	pF
C_{OUT}	Output Capacitance (TDO pin)	-	8	-	8	-	8	pF
C_{PORT}	I/O Signal Port Capacitance	-	10	-	10	-	10	pF
C_{CNTL}	General Control, Key Control and RapidConnect Pin Capacitance	-	8	-	8	-	8	pF

Notes:
(1) Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) A maximum overshoot and undershoot of 2V for a maximum duration of 20 ns is acceptable.
(3) Capacitance measured at 25°C. Sample-tested only.

DC Electrical Specifications

(T_A = 0 °C to 70 °C, V_{DD} = 5V ±5%; V_{DD}.PAD1,2 = 4.75V to 5.25V, or V_{DD}.PAD1,2 = 2.7V to 3.3V)

Symbol	Parameter	Conditions	PSX160, PSX128B, PSX96B		Units
			Min	Max	
V_{IH}	High-Level Input Voltage		2.0	V_{DD}.PAD + 0.3	V
V_{IL}	Low-Level Input Voltage		-0.3	0.8	V
V_{OH}	High-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 4.75 I_{OH} = - 8 mA(3)	2.4	-	V
	High-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 2.7 I_{OH} = - 4mA(3)	2.4	-	V
V_{OL}	Low-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 4.75 I_{OL} = 16 mA	-	0.4	V
	Low-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 2.7 I_{OL} = 16 mA	-	0.4	V
$\|I_{IH}\|$, $\|I_{IL}\|$	Input Leakage Current for I/O Ports	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}.PAD	-	5	µA
I_{PT}	I/O Port Trickling Current (1)	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}.PAD	-	-25	µA
$\|I_{OZ}\|$	Tristate Output Off-State Current	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}.PAD	-	5	µA
I_{PU-WK}	Programmed-Weak Additional Pull-Up Current	V_{DD} = Min, V_{DD}.PAD = Min, V_O = GND	2.5	4.5	mA
I_{PU-SG}	Programmed-Strong Additional Pull-Up Current	V_{DD} = Min, V_{DD}.PAD = Min, V_O = GND	12	20	mA
I_{OS}	Short Circuit Current (1, 2)	V_{DD} = Max, V_{DD}.PAD = Max, V_O = GND	-60	-	mA
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max, V_{DD}.PAD = Max, V_O = GND	-	3.0	mA
Q_{DDD}	Dynamic Power Supply Current per Input/Output Pair (1)	V_{DD} = Min, No Load, Connect one output per input @ 50% duty cycle with all other inputs at GND or V_{DD}	-	0.15	mA/ MHz

Notes:
(1) These parameters are guaranteed but not tested in production.
(2) No more than one output should be tested at a time and the duration of the test should be less than one second.

AC Electrical Specifications

(T_A = 0°C to 70°C, V_{DD} = 5V±5%; V_{DD}.PAD1,2 = 5V±5%, or V_{DD}.PAD1,2 = 3V±10%)
(Assume two I/O Ports connected through the Switch Matrix with 35 pF external loading.)

Speed Grade		-133		-100		-80		-66		Units	Ref. Timing Diagram
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
f_{RIO}	Register Input/Output, Clock Frequency (1)		133		100		80		66	MHz	
$t_{W\text{-}RIO}$	Register Input/Output, Clock Pulse Width, Low or High	3.5		4.5		5.5		6.5		ns	
$t_{S\text{-}RIO}$	Register Input/Output, Data Setup Time to CLK	3.0		3.0		3.0		3.0		ns	1
$t_{H\text{-}RIO}$	Register Input/Output, CLK to Data Hold Time	1.0		1.0		1.0		1.0		ns	
$t_{CO\text{-}RIO}$	Register Input/Output, Clock to Output Data Valid		7.5		10.0		12.0		15.0	ns	
f_{RI}	Register Input, Clock Frequency (1)		133		100		80		66	MHz	
$t_{W\text{-}RI}$	Register Input, Clock Pulse Width, Low or High	3.5		4.5		5.5		6.5		ns	
$t_{S\text{-}RI}$	Register Input, Data Setup Time to CLK	3.0		3.0		3.0		3.0		ns	2
$t_{H\text{-}RI}$	Register Input, CLK to Data Hold Time	1.0		1.0		1.0		1.0		ns	
$t_{CO\text{-}RI}$	Register Input, Clock to Output Data Valid		11.0		13.5		16.0		18.0	ns	
f_{RO}	Register Output, Clock Pulse Frequency (1)		133		100		80		66	MHz	
$t_{W\text{-}RO}$	Register Output, Clock Width, Low or High	3.5		4.5		5.5		6.5		ns	
$t_{S\text{-}RO}$	Register Output, Data Setup Time to CLK	5.0		6.0		7.0		8.0		ns	3
$t_{H\text{-}RO}$	Register Output, CLK to Data Hold Time	0.0		0.0		0.0		0.0		ns	
$t_{CO\text{-}RO}$	Register Output, Clock to Output Data Valid		7.5		10.0		12.5		15.0	ns	
t_{PHL} t_{PLH}	One Way Signal Propagation Delay		7.0		9.0		11.0		13.5	ns	
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)		0.35		0.40		0.50		0.55	ns	4
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode		0.0		0.0		0.0		0.0	ns	
t_{SK}	Skew Between Output Ports (1)		1.5		1.5		1.5		1.5	ns	
t_{W+}	Input Flow Through Positive Pulse Width	5.5		6.5		8.0		10.0		ns	
t_{W-}	Input Flow Through Negative Pulse Width	5.5		6.5		8.0		10.0		ns	
R_{DATA}	NRZ Data Rate (1)		160		133		100		80	Mb/s	
$t_{PZH\text{-}OT}$, $t_{PZL\text{-}OT}$	Output Enable (GC) to Data Valid		9.5		11.5		13.5		16.0	ns	
$t_{PHZ\text{-}OT}$, $t_{PLZ\text{-}OT}$	Output Enable (GC) to Output at High Z (1)		9.5		11.5		13.5		16.0	ns	5
$t_{PZH\text{-}IT}$, $t_{PZL\text{-}IT}$	Input Enable (GC) to Data Valid		9.5		11.5		13.5		16.0	ns	
$t_{PHZ\text{-}IT}$, $t_{PLZ\text{-}IT}$	Input Enable (GC) to Output at High Z (1)		9.5		11.5		13.5		16.0	ns	6
$t_{W\text{-}LI}$	Latch Input, Latch Enable (GC) Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}LI}$	Latch Input, Data Setup Time to Latch Enable (GC) Trailing Edge	3.0		3.0		3.0		3.0		ns	
$t_{H\text{-}LI}$	Latch Input, Data to Latch Enable (GC) Trailing Edge Hold Time	1.0		1.0		1.0		1.0		ns	7
$t_{CO\text{-}LI}$	Latch Input, Latch Enable (GC) Leading Edge to Data Out Delay		11.0		13.5		16.0		18.0	ns	
$t_{P\text{-}LIT}$	Latch Input, Transparent Mode Propagation Delay		9.0		11.0		13.0		15.5	ns	
$t_{W\text{-}LO}$	Latch Output, Latch Enable (GC) Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}LO}$	Latch Output, Data Setup Time to Latch Enable (GC) Trailing Edge	5.0		6.0		7.0		8.0		ns	
$t_{H\text{-}LO}$	Latch Output, Data to Latch Enable (GC) Trailing Edge Hold Time	0.0		0.0		0.0		0.0		ns	8
$t_{CO\text{-}LO}$	Latch Output, Latch Enable (GC) Leading Edge to Data Out Delay		7.5		10.0		12.5		15.0	ns	
$t_{P\text{-}LOT}$	Latch Output, Transparent Mode Propagation Delay		9.0		11.0		13.0		15.5	ns	

AC Electrical Specifications (cont.)

Symbol	Parameter	Speed Grade	-133		-100		-80		-66		Units	Ref. Timing Diagram
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{KW-RI}	Register Input, Minimum Pulse Width of KEY as Clock Enable, Low or High (1)		5.0		6.0		7.0		8.0		ns	9
t_{KS-RI}	Register Input, Clock Enable (Key) Setup Time to CLK (GC) (1)		3.0		3.0		3.0		3.0		ns	
t_{KH-RI}	Register Input, CLK (GC) to Clock Enable (Key) Hold Time (1)		1.0		1.0		1.0		1.0		ns	
t_{KCO-RI}	Register Input, Key Clock to Output Data Valid (1)			11.0		13.5		16		18	ns	
t_{KW-RO}	Register Output, Minimum Pulse Width of KEY as Clock Enable, Low or High (1)		5.0		6.0		7.0		8.0		ns	10
t_{KS-RO}	Register Output, Clock Enable (Key) Setup Time to CLK (GC) (1)		3.0		3.0		3.0		3.0		ns	
t_{KH-RO}	Register Output, CLK (GC) to Clock Enable (Key) Hold Time		1.0		1.0		1.0		1.0		ns	
t_{KCO-RO}	Register Output, Key Clock to Output Data Valid			7.5		10.0		12.0		15.0	ns	
$t_{KPZH-OT}$ $t_{KPZL-OT}$	Output Enable (Key) to Data Valid (1)			9.5		11.5		13.5		16.0	ns	11
$t_{KPHZ-OT}$ $t_{KPLZ-OT}$	Output Enable (Key) to Output at High Z (1)			9.5		11.5		13.5		16.0	ns	
$t_{KPZH-IT}$ $t_{KPZL-IT}$	Input Enable (Key) to Data Valid (1)			9.5		11.5		13.5		16.0	ns	12
$t_{KPHZ-IT}$ $t_{KPLZ-IT}$	Input Enable (Key) to Output at High Z (1)			9.5		11.5		13.5		16.0	ns	
t_{KW-LI}	Latch Input, Minimum Pulse Width of KEY as Latch Enable, Low or High (1)		5.0		6.0		7.0		8.0		ns	13
t_{KS-LI}	Latch Input, Data Setup Time to Latch Enable (Key) Trailing Edge (1)		3.0		3.0		3.0		3.0		ns	
t_{KH-LI}	Latch Input, Data to Latch Enable (Key) Trailing Edge Hold Time (1)		1.0		1.0		1.0		1.0		ns	
t_{KCO-LI}	Latch Input, Latch Enable (Key) Leading Edge to Data Out (1)			11.0		13.5		16.0		18.0	ns	
t_{KP-LIT}	Latch Input, Transparent Mode Propagation Delay (1)			9.0		11.0		13.0		15.5	ns	
t_{KW-LO}	Latch Output, Minimum Pulse Width of KEY as Latch Enable, Low or High		5.0		6.0		7.0		8.0		ns	14
t_{KS-LO}	Latch Output, Data Setup Time to Latch Enable (Key) Trailing Edge		5.0		6.0		7.0		8.0		ns	
t_{KH-LO}	Latch Output, Data to Latch Enable (Key) Trailing Edge Hold Time		0.0		0.0		0.0		0.0		ns	
t_{KCO-LO}	Latch Output, Latch Enable (Key) Leading Edge to Data Out			11.0		12.5		15.0		17.5	ns	
t_{KP-LOT}	Latch Output, Transparent Mode Propagation Delay			9.0		11.0		13.0		15.5	ns	
T_{RC}	RapidConnect Strobe Period		12.0		13.5		15.5		18.0		ns	15
$t_{W+ -RC}$ $t_{W- -RC}$	RapidConnect Strobe Pulse Width		5.0 4.5		6.0 5.5		7.0 6.0		8.0 7.0		ns	
t_{S-RC}	RapidConnect Address and Data Setup Time		4.0		4.0		4.0		4.0		ns	
t_{H-RC}	RapidConnect Address and Data Hold Time		0.0		0.0		0.0		0.0		ns	
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection			13.0		15.0		17.0		20.0	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency			20		20		20		20	MHz	16
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width		20.0		20.0		20.0		20.0		ns	
t_{S-JTAG}	JTAG Setup Time		4.0		4.5		5.0		5.5		ns	
t_{H-JTAG}	JTAG Hold Time		0.0		0.5		1.0		1.5		ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid		15.0		15.0		15.0		15.0		ns	
t_{BO}	Bank to Output Data Valid			9.5		11.5		13.5		16.0	ns	

Note:
(1) These parameters are guaranteed but not tested in production.

Test Circuit and Timing Diagrams

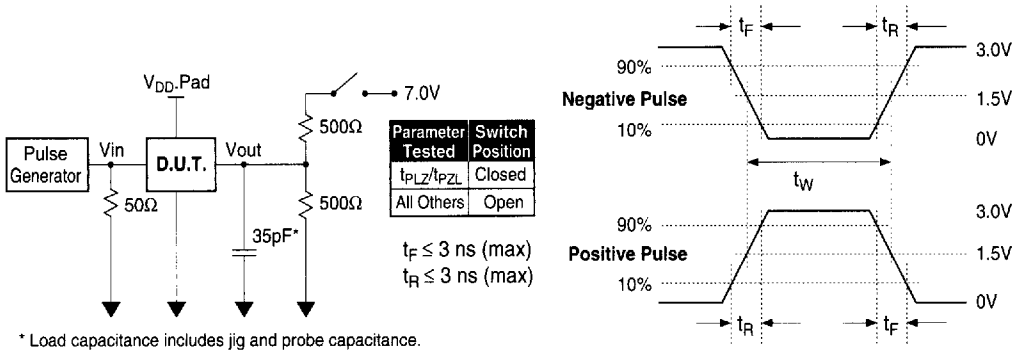
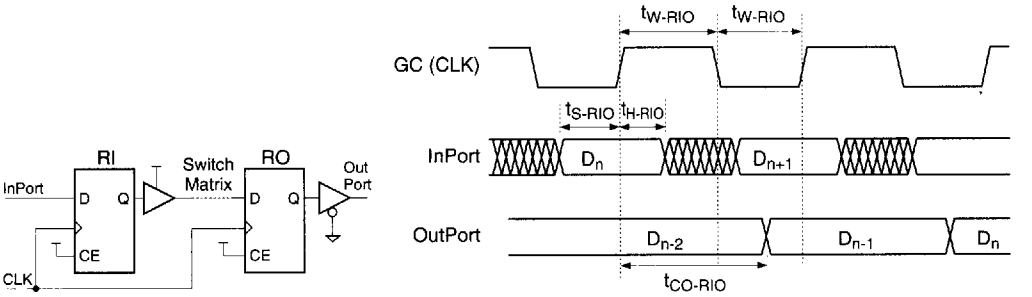
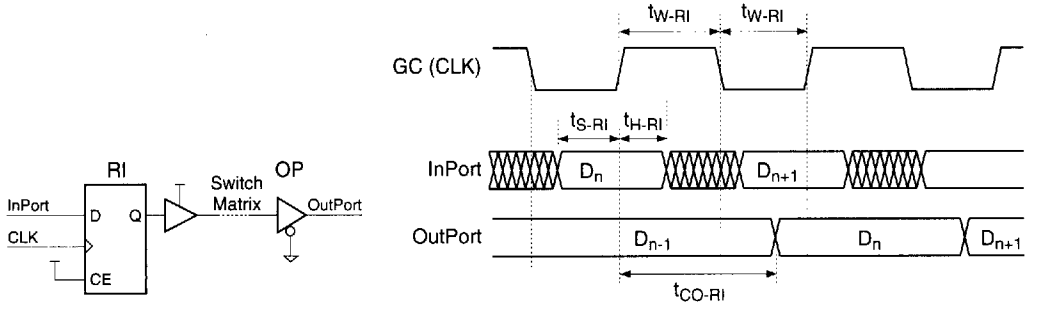


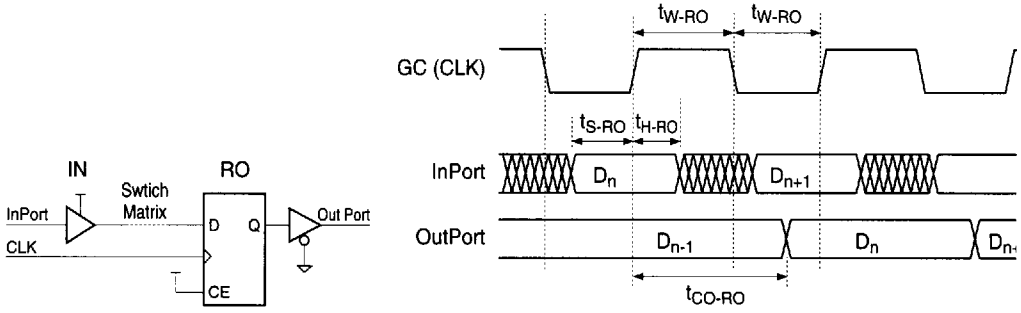
Figure 15: Test Circuit and Waveform Definition



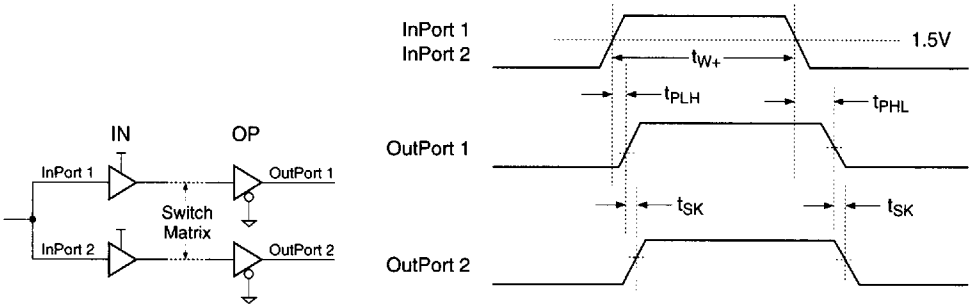
Timing Diagram 1: Registered Input and Registered Output Mode Timing (ICLK and OCLK are Synchronized)



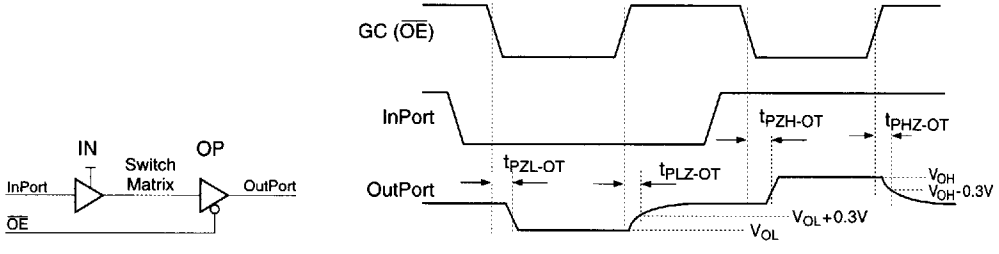
Timing Diagram 2: Registered Input Mode Timing



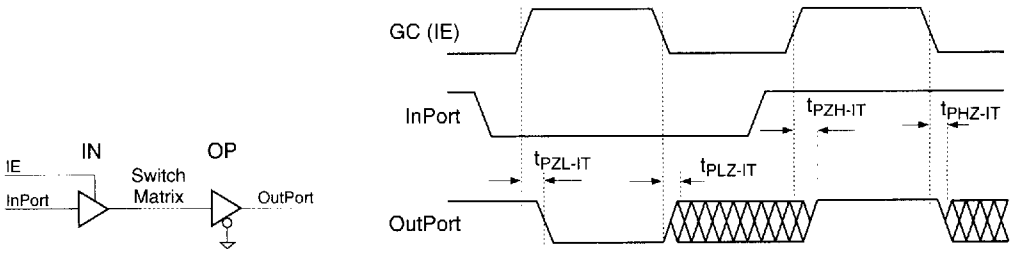
Timing Diagram 3: Registered Output Mode Timing



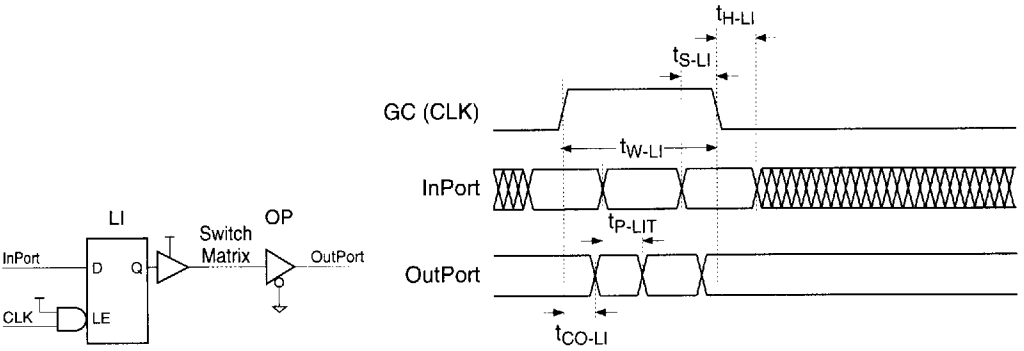
Timing Diagram 4: I/O Port Timing (Flow-through Mode)



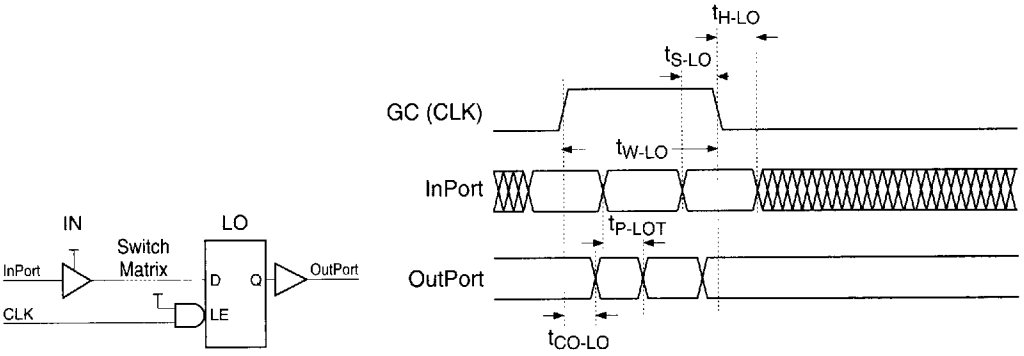
Timing Diagram 5: Output Enable Timing (Flow-through Mode)



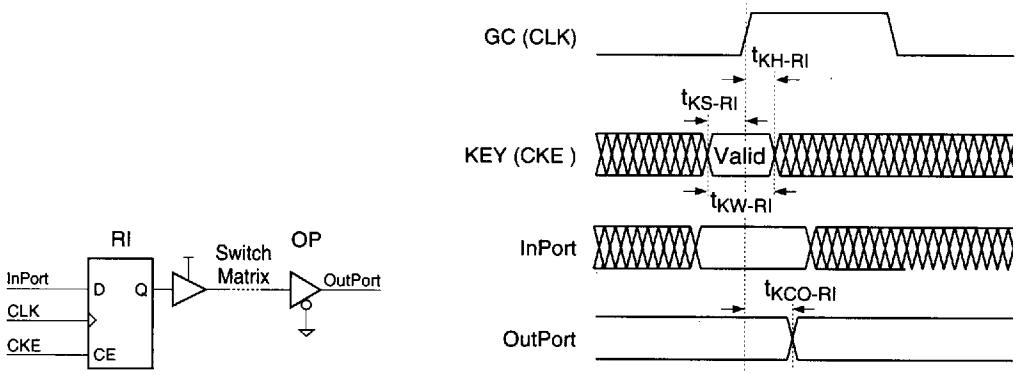
Timing Diagram 6: Input Enable Timing (Flow-through Mode)



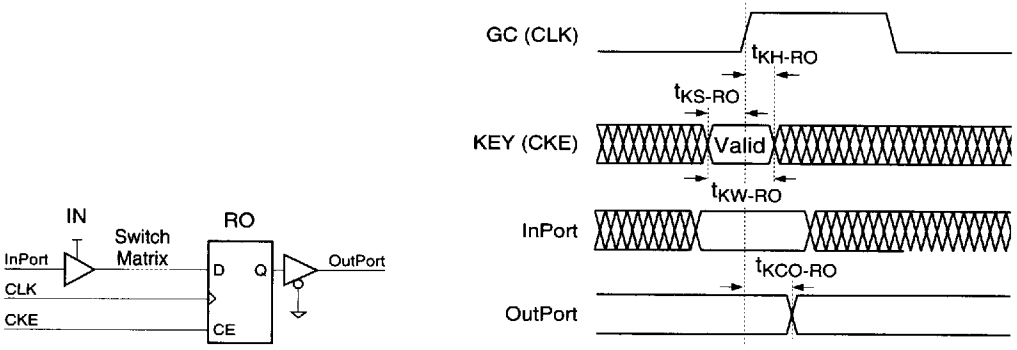
Timing Diagram 7: Latched Input Mode Timing



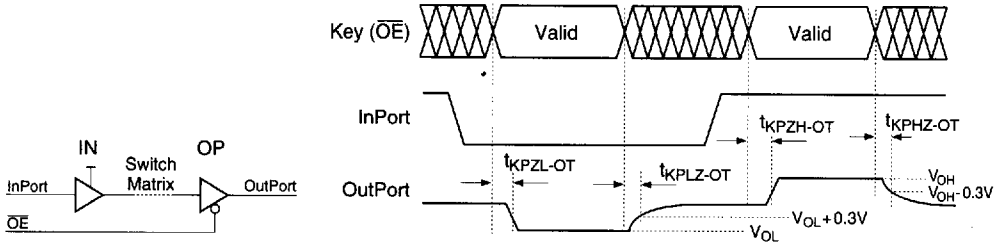
Timing Diagram 8: Latched Output Mode Timing



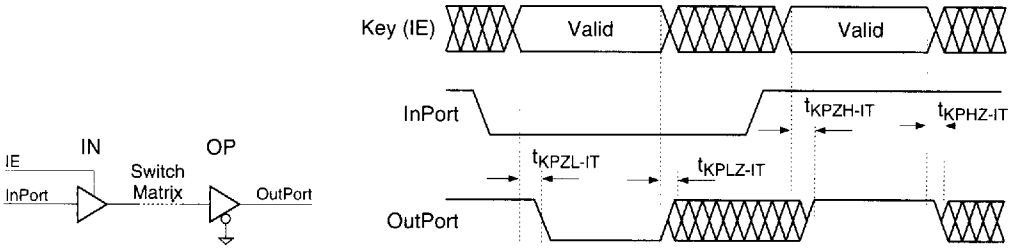
Timing Diagram 9: Key Timing for Register Input, Clock Enable (CKE)



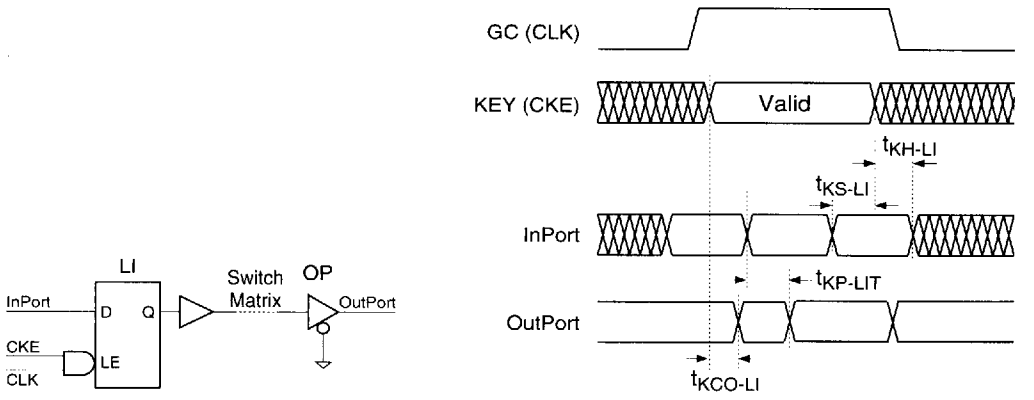
Timing Diagram 10: Key Timing for Register Output, Clock Enable (CKE)



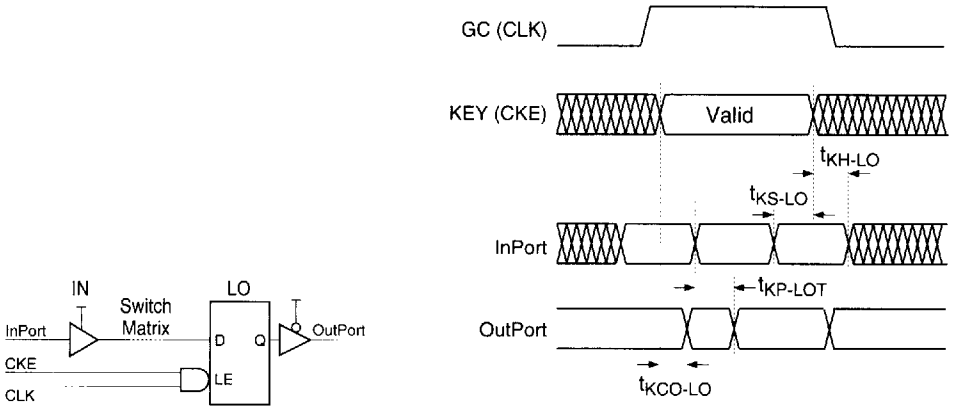
Timing Diagram 11: Key Timing for Output Enable



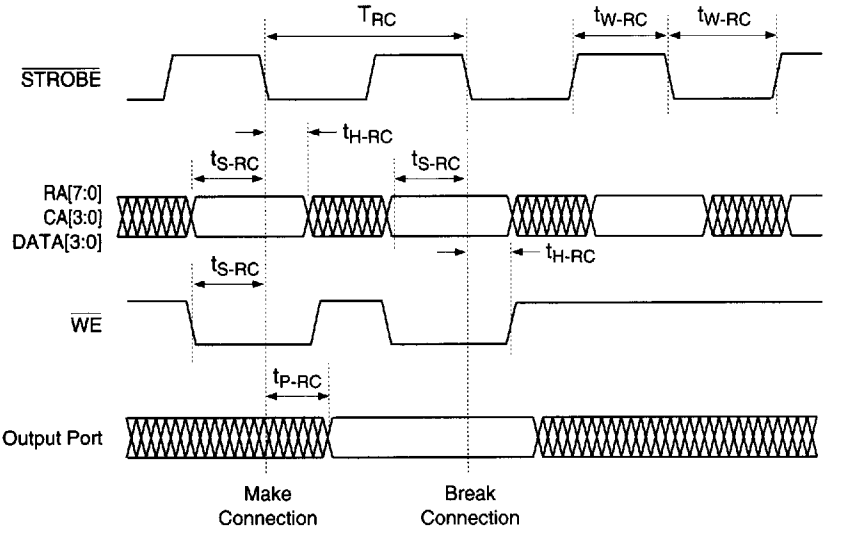
Timing Diagram 12: Key Timing for Input Enable



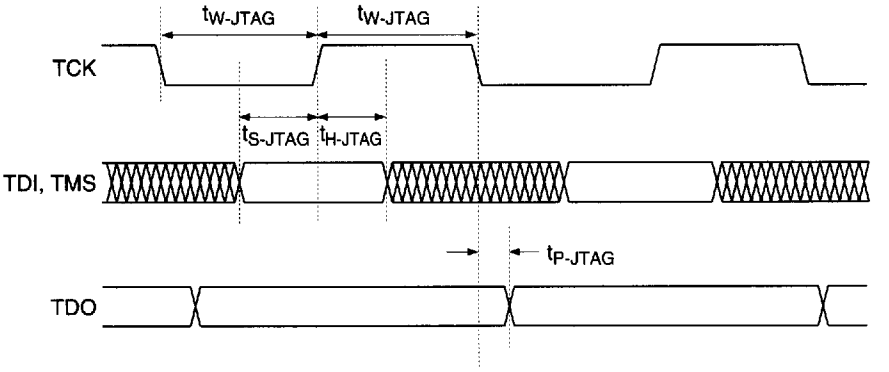
Timing Diagram 13: Key Timing for Latch Input, Enable (CKE)



Timing Diagram 14: Key Timing for Latch Output, Enable (CKE)



Timing Diagram 15: RapidConnect Timing



Timing Diagram 16: JTAG Timing

External AC Timing Characteristics as Functions of Internal AC Timing Characteristics

The following table shows the relationship between external and internal timing parameters described in the next section.

Symbol	Equation
t_{PLH}, t_{PHL}	Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o + Tp_otsb
$t_{P\Delta}$	ΔTp_sw
$t_{PZL\text{-}OT}$, $t_{PZH\text{-}OT}$	Tp_gc + Tz_otsb
$t_{PLZ\text{-}OT}$, $t_{PHZ\text{-}OT}$	Tp_gc + Tz_otsb
$t_{PZL\text{-}IT}$, $t_{PZH\text{-}IT}$	Tp_gc + Tz_itsb
$t_{PLZ\text{-}IT}$, $t_{PHZ\text{-}IT}$	Tp_gc + Tz_itsb
$t_{S\text{-}RI}$	Tp_ipad + Ts_r - Tp_gc
$t_{H\text{-}RI}$	Tp_gc + Th_r - Tp_ipad
$t_{CO\text{-}RI}$	Tp_gc + Tco_ri + Tp_sw + Tp_a_o + Tp_otsb
$t_{S\text{-}RO}$	(Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o) + Ts_r - Tp_gc
$t_{H\text{-}RO}$	Tp_gc + Th_r - (Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o)
$t_{CO\text{-}RO}$	Tp_gc + Tco_ro
$t_{S\text{-}RIO}$	Tp_ipad + Ts_r - Tp_gc
$t_{H\text{-}RIO}$	Tp_gc + Th_r - Tp_ipad
$t_{CO\text{-}RIO}$	Tp_gc + Tco_ro
$t_{S\text{-}LI}$	Tp_ipad + Ts_l - Tp_gc
$t_{H\text{-}LI}$	Tp_gc + Th_l - Tp_ipad
t_{CO_LI}	Tp_gc + Tco_li + Tp_sw + Tp_a_o + Tp_otsb
$t_{P\text{-}LIT}$	Tp_ipad + Tco_li + Tp_sw + Tp_a_o + Tp_otsb
$t_{S\text{-}LO}$	(Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o) + Ts_l - Tp_gc
$t_{H\text{-}LO}$	Tp_gc + Th_l - (Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o)
$t_{CO\text{-}LO}$	Tp_gc + Tco_lo
$t_{P\text{-}LOT}$	Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o + Tco_lo
$t_{KPZL\text{-}OT}$, $t_{KPZH\text{-}OT}$	Tp_ky + Tz_otsb
$t_{KPLZ\text{-}OT}$, $t_{KPHZ\text{-}OT}$	Tp_ky + Tz_otsb
$t_{KPZL\text{-}IT}$, $t_{KPZH\text{-}IT}$	Tp_ky + Tz_itsb
$t_{KPLZ\text{-}IT}$, $t_{KPHZ\text{-}IT}$	Tp_ky + Tz_itsb
$t_{KS\text{-}RI}$	Tp_ipad + Ts_r - Tp_ky
$t_{KH\text{-}RI}$	Tp_ky + Th_r - Tp_ipad
$t_{KCO\text{-}RI}$	Tp_ky + Tco_ri + Tp_sw + Tp_a_o + Tp_otsb
$t_{KS\text{-}RO}$	(Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o) + Ts_r - Tp_ky
$t_{KH\text{-}RO}$	Tp_ky + Th_r - (Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o)
$t_{KCO\text{-}RO}$	Tp_ky + Tco_or
$t_{KS\text{-}LI}$	Tp_ipad + Ts_l - Tp_ky
$t_{KH\text{-}LI}$	Tp_ky + Th_l - Tp_ipad
$t_{KCO\text{-}LI}$	Tp_ky + Tco_li + Tp_sw + Tp_a_o + Tp_otsb
$t_{KS\text{-}LO}$	(Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o) + Ts_l - Tp_ky
$t_{KH\text{-}LO}$	Tp_ky + Th_l - (Tp_ipad + Tp_itsb + Tp_sw + Tp_a_o)
$t_{KCO\text{-}LO}$	Tp_ky + Tco_lo

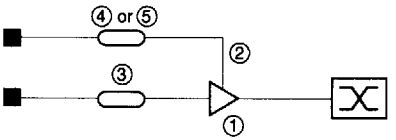
Internal AC Timing Characteristics for -133 speed grade (all times are in ns)

Internal timing parameters and corresponding circuit models are described below. The timing values are based on simulation data for a PSX160-133. The reference numbers correspond to those in the "Internal Timing Models" on the following pages.

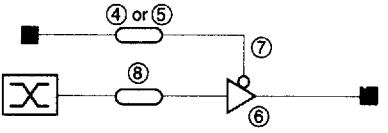
Symbol	Parameter	5.25V 0 C	4.75V 70 C	Reference Number
Tp_itsb	Input buffer delay. The propagation delay for data path through input buffer (excluding the pad buffer delay).	0.7	1.6	(1)
Tz_itsb	Input enable delay. The delay from assertion of the enable node to the time the array line is driven to an active level.	0.7	1.6	(2)
	Input tristate delay. The delay from de-assertion of the enable node to the time the array line floats to a high-Z state.			
Tp_ipad	Input pad buffer delay.	0.45	1.0	(3)
Tp_gc	Control line delay. The delay from assertion of input control pin to internal node (includes pad and mux delays).	1.8	4.0	(4)
Tp_ky	Key bus delay. The delay from a valid key value to internal node (includes pad, comparator and mux delays).	3.4	6.5	(5)
Tp_otsb	Output buffer delay. The propagation delay for data path through input buffer (includes pad delay).	0.9	2.0	(6)
Tz_otsb	Output enable delay. The delay from assertion of the enable node to the time the output pin is driven to an active level.	0.8	2.0	(7)
	Output tristate delay. The delay from de-assertion of the enable signal to the time the output pin floats to a high-Z state.			
Tp_a_o	Array to out delay. The propagation delay from output of Switch Matrix to entrance node of output stage.	0.45	1.0	(8)
Tp_li	Input latch delay. The propagation delay through a transparent input latch.	0.9	1.9	(9)
Tp_lo	Output latch delay. The propagation delay through a transparent output latch.	1.0	2.0	(10)
Ts_l	Latch setup time. The time required for a signal to be stable at the latch input before the active level of clock or clock enable.	0.5	1.0	(11)
Th_l	Latch hold time. The time required for a signal to be stable at the latch input after the active level of clock or clock enable.	0.0	0.0	(12)
Tco_li	Input latch clock to out. The time required to obtain a held output (array line) after the active level of clock or clock enable. Also, the time required to obtain a tracking output after the inactive level of clock or clock enable (excludes control line delay).	0.4	0.8	(13)
Tco_lo	Output latch clock to out. The time required to obtain a held pin output after the active level of clock or clock enable. Also, the time required to obtain a tracking pin output after the inactive level of clock or clock enable (excludes control line delay).	0.4	0.8	(14)
Ts_r	Register setup time. The time required for a signal to be stable at the register input before the active edge of clock or active level of clock enable	0.5	1.0	(15)
Th_r	Register hold time. The time required for a signal to be stable at the register input after the active edge of clock or active level of clock enable.	0.0	0.0	(16)
Tco_ri	Input register clock to out. The time required to obtain a valid output (array line) after the active edge of clock or active level of clock enable (excludes control line delay).	0.5	1.0	(17)
Tco_ro	Output register clock to out. The time required to obtain a valid pin output after the active edge of clock or active level of clock enable (excludes control line delay).	0.5	1.0	(18)
Tp_bsel	Propagation delay from bank select pin to output of preconnected output buffer	2.1	3.5	(19)
Tp_sw	Propagation delay through Switch Matrix (one load)	0.45	1.0	(20)

Circuit Models for Internal Timing

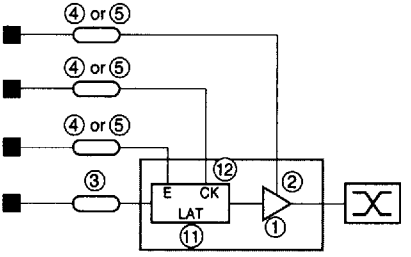
Timing models are simplified block diagrams that illustrate internal propagation delays for signal paths and control paths.



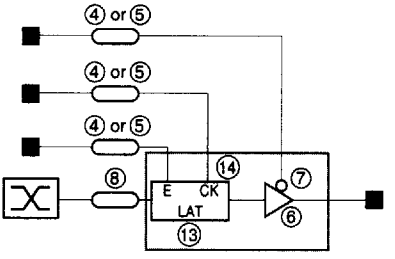
Internal Timing Model 1: Flow Through (from Input to Switch Matrix)



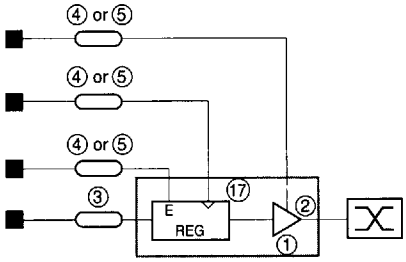
Internal Timing Model 2: Flow Through (From Switch Matrix to Output)



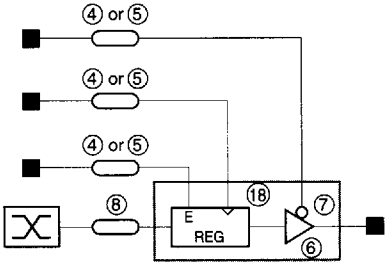
Internal Timing Model 3: Latched Input (from Input to Switch Matrix)



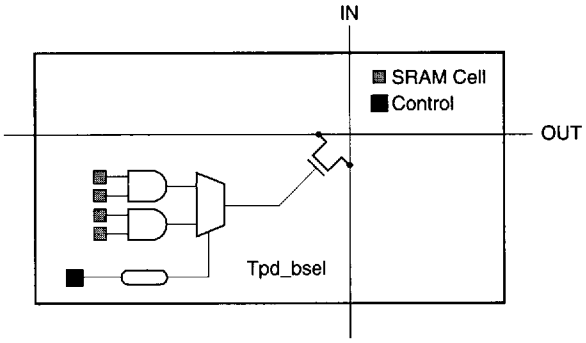
Internal Timing Model 4: Latched Output (From Switch Matrix to Output)



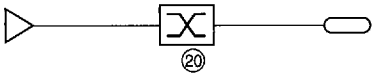
Internal Timing Model 5: Registered Input (from Input to Switch Matrix)



Internal Timing Model 6: Registered Output (From Switch Matrix to Output)

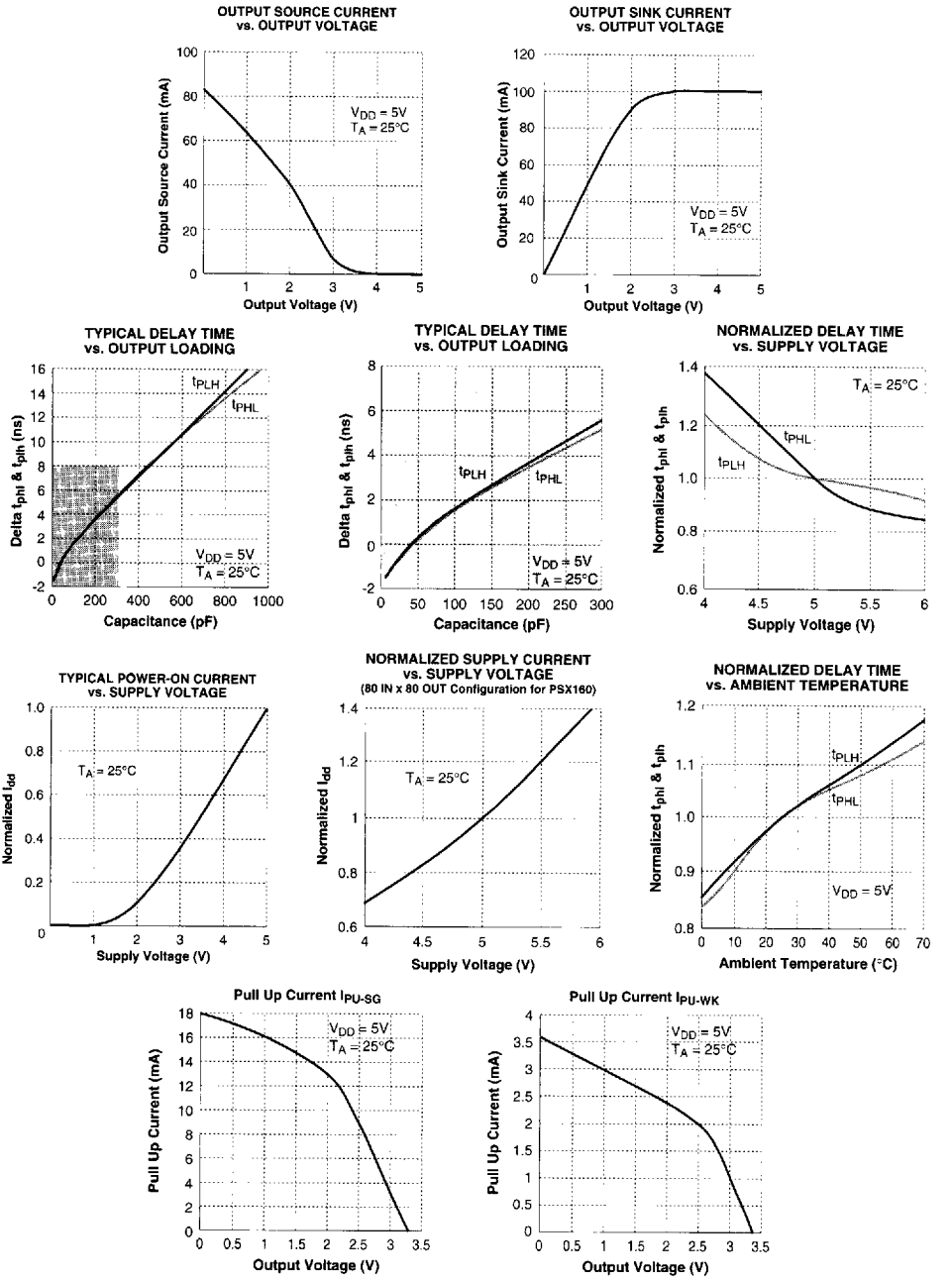


Internal Timing Model 7: Switch Matrix Delay when Switching Banks



Internal Timing Model 8: Switch Matrix Delay

Typical AC and DC Characteristics



Pinout

PSX160 [BGA Package] Pinout

Contact I-Cube Marketing for details.

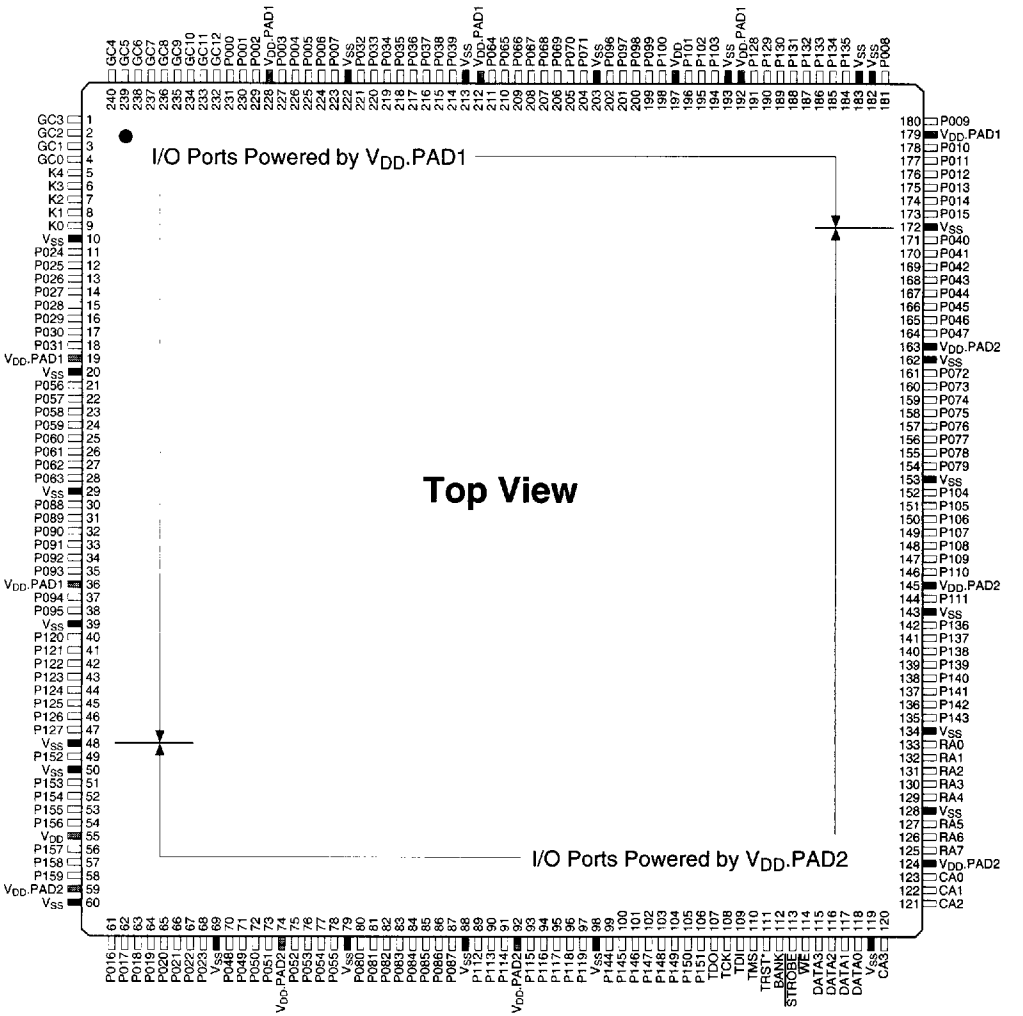
PSX160 [MQUAD/PQFP 240L Package] Pinout by Pin Location

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	GC3	41	P121	81	P081	121	CA2	161	P072	201	P097
2	GC2	42	P122	82	P082	122	CA1	162	V_{SS}	202	P096
3	GC1	43	P123	83	P083	123	CA0	163	V_{DD}.PAD2	203	V_{SS}
4	GC0	44	P124	84	P084	124	V_{DD}.PAD2	164	P047	204	P071
5	K4	45	P125	85	P085	125	RA7	165	P046	205	P070
6	K3	46	P126	86	P086	126	RA6	166	P045	206	P069
7	K2	47	P127	87	P087	127	RA5	167	P044	207	P068
8	K1	48	V_{SS}	88	V_{SS}	128	V_{SS}	168	P043	208	P067
9	K0	49	P152	89	P112	129	RA4	169	P042	209	P066
10	V_{SS}	50	V_{SS}	90	P113	130	RA3	170	P041	210	P065
11	P024	51	P153	91	P114	131	RA2	171	P040	211	P064
12	P025	52	P154	92	V_{DD}.PAD2	132	RA1	172	V_{SS}	212	V_{DD}.PAD1
13	P026	53	P155	93	P115	133	RA0	173	P015	213	V_{SS}
14	P027	54	P156	94	P116	134	V_{SS}	174	P014	214	P039
15	P028	55	V_{DD}	95	P117	135	P143	175	P013	215	P038
16	P029	56	P157	96	P118	136	P142	176	P012	216	P037
17	P030	57	P158	97	P119	137	P141	177	P011	217	P036
18	P031	58	P159	98	V_{SS}	138	P140	178	P010	218	P035
19	V_{DD}.PAD1	59	V_{DD}.PAD2	99	P144	139	P139	179	V_{DD}.PAD1	219	P034
20	V_{SS}	60	V_{SS}	100	P145	140	P138	180	P009	220	P033
21	P056	61	P016	101	P146	141	P137	181	P008	221	P032
22	P057	62	P017	102	P147	142	P136	182	V_{SS}	222	V_{SS}
23	P058	63	P018	103	P148	143	V_{SS}	183	V_{SS}	223	P007
24	P059	64	P019	104	P149	144	P111	184	P135	224	P006
25	P060	65	P020	105	P150	145	V_{DD}.PAD2	185	P134	225	P005
26	P061	66	P021	106	P151	146	P110	186	P133	226	P004
27	P062	67	P022	107	TDO	147	P109	187	P132	227	P003
28	P063	68	P023	108	TCK	148	P108	188	P131	228	V_{DD}.PAD1
29	V_{SS}	69	V_{SS}	109	TDI	149	P107	189	P130	229	P002
30	P088	70	P048	110	TMS	150	P106	190	P129	230	P001
31	P089	71	P049	111	TRST*	151	P105	191	P128	231	P000
32	P090	72	P050	112	BANK	152	P104	192	V_{DD}.PAD1	232	GC12
33	P091	73	P051	113	$\overline{\text{STROBE}}$	153	V_{SS}	193	V_{SS}	233	GC11
34	P092	74	V_{DD}.PAD2	114	$\overline{\text{WE}}$	154	P079	194	P103	234	GC10
35	P093	75	P052	115	DATA3	155	P078	195	P102	235	GC9
36	V_{DD}.PAD1	76	P053	116	DATA2	156	P077	196	P101	236	GC8
37	P094	77	P054	117	DATA1	157	P076	197	V_{DD}	237	GC7
38	P095	78	P055	118	DATA0	158	P075	198	P100	238	GC6
39	V_{SS}	79	V_{SS}	119	V_{SS}	159	P074	199	P099	239	GC5
40	P120	80	P080	120	CA3	160	P073	200	P098	240	GC4

PSX160 [MQUAD/PQFP 240L Package] Pinout by Pin Name

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
BANK	112	P013	175	P053	76	P093	35	P133	186	TRST*	111
CA0	123	P014	174	P054	77	P094	37	P134	185	V_{DD}	55
CA1	122	P015	173	P055	78	P095	38	P135	184	V_{DD}	197
CA2	121	P016	61	P056	21	P096	202	P136	142	V_{DD}.PAD1	19
CA3	120	P017	62	P057	22	P097	201	P137	141	V_{DD}.PAD1	36
DATA0	118	P018	63	P058	23	P098	200	P138	140	V_{DD}.PAD1	179
DATA1	117	P019	64	P059	24	P099	199	P139	139	V_{DD}.PAD1	192
DATA2	116	P020	65	P060	25	P100	198	P140	138	V_{DD}.PAD1	212
DATA3	115	P021	66	P061	26	P101	196	P141	137	V_{DD}.PAD1	228
GC0	4	P022	67	P062	27	P102	195	P142	136	V_{DD}.PAD2	59
GC1	3	P023	68	P063	28	P103	194	P143	135	V_{DD}.PAD2	74
GC2	2	P024	11	P064	211	P104	152	P144	99	V_{DD}.PAD2	92
GC3	1	P025	12	P065	210	P105	151	P145	100	V_{DD}.PAD2	124
GC4	240	P026	13	P066	209	P106	150	P146	101	V_{DD}.PAD2	145
GC5	239	P027	14	P067	208	P107	149	P147	102	V_{DD}.PAD2	163
GC6	238	P028	15	P068	207	P108	148	P148	103	V_{SS}	50
GC7	237	P029	16	P069	206	P109	147	P149	104	V_{SS}	128
GC8	236	P030	17	P070	205	P110	146	P150	105	V_{SS}	183
GC9	235	P031	18	P071	204	P111	144	P151	106	V_{SS}	10
GC10	234	P032	221	P072	161	P112	89	P152	49	V_{SS}	20
GC11	233	P033	220	P073	160	P113	90	P153	51	V_{SS}	29
GC12	232	P034	219	P074	159	P114	91	P154	52	V_{SS}	39
K0	9	P035	218	P075	158	P115	93	P155	53	V_{SS}	48
K1	8	P036	217	P076	157	P116	94	P156	54	V_{SS}	60
K2	7	P037	216	P077	156	P117	95	P157	56	V_{SS}	69
K3	6	P038	215	P078	155	P118	96	P158	57	V_{SS}	79
K4	5	P039	214	P079	154	P119	97	P159	58	V_{SS}	88
P000	231	P040	171	P080	80	P120	40	RA0	133	V_{SS}	98
P001	230	P041	170	P081	81	P121	41	RA1	132	V_{SS}	119
P002	229	P042	169	P082	82	P122	42	RA2	131	V_{SS}	134
P003	227	P043	168	P083	83	P123	43	RA3	130	V_{SS}	143
P004	226	P044	167	P084	84	P124	44	RA4	129	V_{SS}	153
P005	225	P045	166	P085	85	P125	45	RA5	127	V_{SS}	162
P006	224	P046	165	P086	86	P126	46	RA6	126	V_{SS}	172
P007	223	P047	164	P087	87	P127	47	RA7	125	V_{SS}	182
P008	181	P048	70	P088	30	P128	191	$\overline{\text{STROBE}}$	113	V_{SS}	193
P009	180	P049	71	P089	31	P129	190	TCK	108	V_{SS}	203
P010	178	P050	72	P090	32	P130	189	TDI	109	V_{SS}	213
P011	177	P051	73	P091	33	P131	188	TDO	107	V_{SS}	222
P012	176	P052	75	P092	34	P132	187	TMS	110	$\overline{\text{WE}}$	114

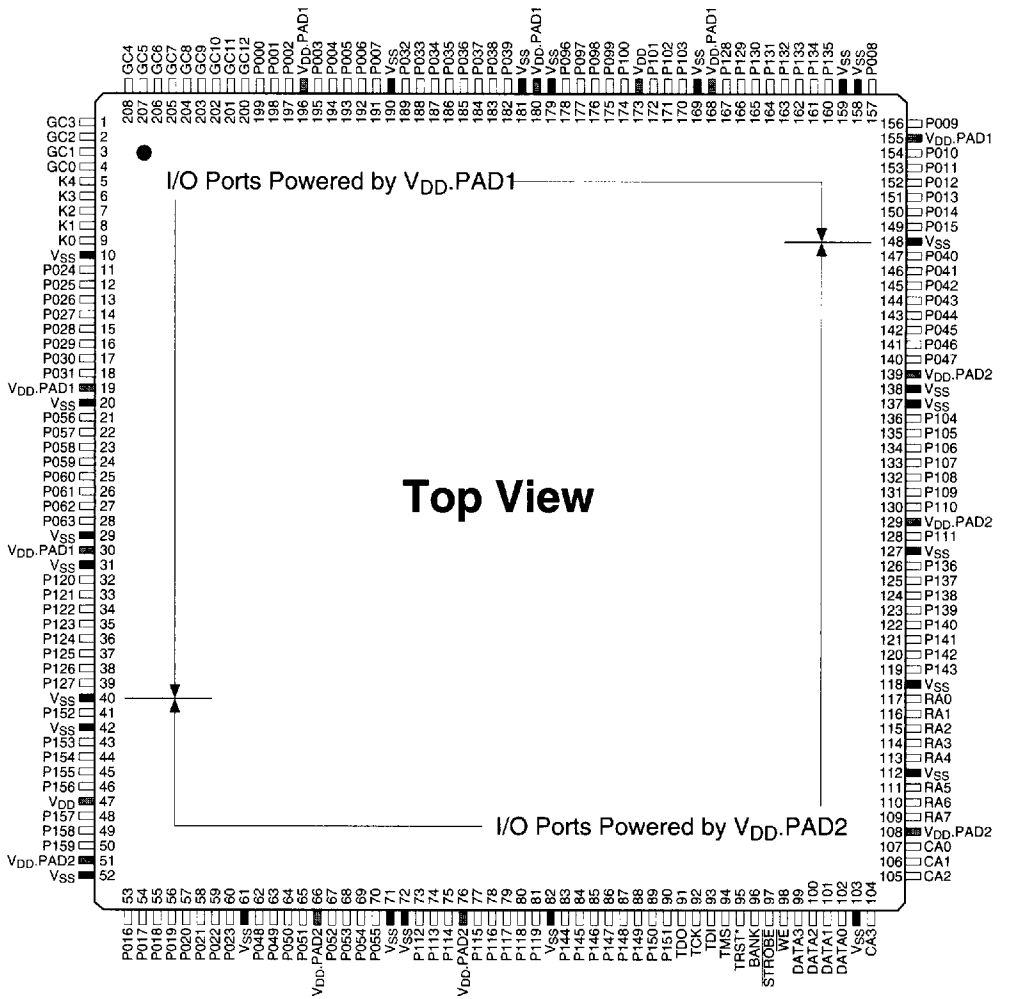
PSX160 [MQUAD/PQFP 240L Package] Pinout



PSX128B [MQUAD/PQFP 208L Package] Pinout by Pin Name

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
BANK	96	P025	12	P109	131	RA1	116
CA0	107	P026	13	P110	130	RA2	115
CA1	106	P027	14	P111	128	RA3	114
CA2	105	P028	15	P112	73	RA4	113
CA3	104	P029	16	P113	74	RA5	111
DATA0	102	P030	17	P114	75	RA6	110
DATA1	101	P031	18	P115	77	RA7	109
DATA2	100	P032	189	P116	78	$\overline{\text{STROBE}}$	97
DATA3	99	P033	188	P117	79	TCK	92
GC0	4	P034	187	P118	80	TDI	93
GC1	3	P035	186	P119	81	TDO	91
GC2	2	P036	185	P120	32	TMS	94
GC3	1	P037	184	P121	33	TRST*	95
GC4	208	P038	183	P122	34	V_{DD}	47
GC5	207	P039	182	P123	35	V_{DD}	173
GC6	206	P040	147	P124	36	V_{DD}.PAD1	19
GC7	205	P041	146	P125	37	V_{DD}.PAD1	30
GC8	204	P042	145	P126	38	V_{DD}.PAD1	155
GC9	203	P043	144	P127	39	V_{DD}.PAD1	168
GC10	202	P044	143	P128	167	V_{DD}.PAD1	180
GC11	201	P045	142	P129	166	V_{DD}.PAD1	196
GC12	200	P046	141	P130	165	V_{DD}.PAD2	51
K0	9	P047	140	P131	164	V_{DD}.PAD2	66
K1	8	P048	62	P132	163	V_{DD}.PAD2	76
K2	7	P049	63	P133	162	V_{DD}.PAD2	108
K3	6	P050	64	P134	161	V_{DD}.PAD2	129
K4	5	P051	65	P135	160	V_{DD}.PAD2	139
P000	199	P052	67	P136	126	V_{SS}	42
P001	198	P053	68	P137	125	V_{SS}	112
P002	197	P054	69	P138	124	V_{SS}	159
P003	195	P055	70	P139	123	V_{SS}	10
P004	194	P056	21	P140	122	V_{SS}	20
P005	193	P057	22	P141	121	V_{SS}	29
P006	192	P058	23	P142	120	V_{SS}	31
P007	191	P059	24	P143	119	V_{SS}	40
P008	157	P060	25	P144	83	V_{SS}	52
P009	156	P061	26	P145	84	V_{SS}	61
P010	154	P062	27	P146	85	V_{SS}	71
P011	153	P063	28	P147	86	V_{SS}	72
P012	152	P096	178	P148	87	V_{SS}	82
P013	151	P097	177	P149	88	V_{SS}	103
P014	150	P098	176	P150	89	V_{SS}	118
P015	149	P099	175	P151	90	V_{SS}	127
P016	53	P100	174	P152	41	V_{SS}	137
P017	54	P101	172	P153	43	V_{SS}	138
P018	55	P102	171	P154	44	V_{SS}	148
P019	56	P103	170	P155	45	V_{SS}	158
P020	57	P104	136	P156	46	V_{SS}	169
P021	58	P105	135	P157	48	V_{SS}	179
P022	59	P106	134	P158	49	V_{SS}	181
P023	60	P107	133	P159	50	V_{SS}	190
P024	11	P108	132	RA0	117	$\overline{\text{WE}}$	98

PSX128B [MQUAD/PQFP 208L Package] Pinout



PSX128B [MQUAD/PQFP 208L Package] Pinout by Pin Location

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	GC3	53	P016	105	CA2	157	P008
2	GC2	54	P017	106	CA1	158	V_{SS}
3	GC1	55	P018	107	CA0	159	V_{SS}
4	GC0	56	P019	108	V_{DD}.PAD2	160	P135
5	K4	57	P020	109	RA7	161	P134
6	K3	58	P021	110	RA6	162	P133
7	K2	59	P022	111	RA5	163	P132
8	K1	60	P023	112	V_{SS}	164	P131
9	K0	61	V_{SS}	113	RA4	165	P130
10	V_{SS}	62	P048	114	RA3	166	P129
11	P024	63	P049	115	RA2	167	P128
12	P025	64	P050	116	RA1	168	V_{DD}.PAD1
13	P026	65	P051	117	RA0	169	V_{SS}
14	P027	66	V_{DD}.PAD2	118	V_{SS}	170	P103
15	P028	67	P052	119	P143	171	P102
16	P029	68	P053	120	P142	172	P101
17	P030	69	P054	121	P141	173	V_{DD}
18	P031	70	P055	122	P140	174	P100
19	V_{DD}.PAD1	71	V_{SS}	123	P139	175	P099
20	V_{SS}	72	V_{SS}	124	P138	176	P098
21	P056	73	P112	125	P137	177	P097
22	P057	74	P113	126	P136	178	P096
23	P058	75	P114	127	V_{SS}	179	V_{SS}
24	P059	76	V_{DD}.PAD2	128	P111	180	V_{DD}.PAD1
25	P060	77	P115	129	V_{DD}.PAD2	181	V_{SS}
26	P061	78	P116	130	P110	182	P039
27	P062	79	P117	131	P109	183	P038
28	P063	80	P118	132	P108	184	P037
29	V_{SS}	81	P119	133	P107	185	P036
30	V_{DD}.PAD1	82	V_{SS}	134	P106	186	P035
31	V_{SS}	83	P144	135	P105	187	P034
32	P120	84	P145	136	P104	188	P033
33	P121	85	P146	137	V_{SS}	189	P032
34	P122	86	P147	138	V_{SS}	190	V_{SS}
35	P123	87	P148	139	V_{DD}.PAD2	191	P007
36	P124	88	P149	140	P047	192	P006
37	P125	89	P150	141	P046	193	P005
38	P126	90	P151	142	P045	194	P004
39	P127	91	TDO	143	P044	195	P003
40	V_{SS}	92	TCK	144	P043	196	V_{DD}.PAD1
41	P152	93	TDI	145	P042	197	P002
42	V_{SS}	94	TMS	146	P041	198	P001
43	P153	95	TRST*	147	P040	199	P000
44	P154	96	BANK	148	V_{SS}	200	GC12
45	P155	97	$\overline{\text{STROBE}}$	149	P015	201	GC11
46	P156	98	$\overline{\text{WE}}$	150	P014	202	GC10
47	V_{DD}	99	DATA3	151	P013	203	GC9
48	P157	100	DATA2	152	P012	204	GC8
49	P158	101	DATA1	153	P011	205	GC7
50	P159	102	DATA0	154	P010	206	GC6
51	V_{DD}.PAD2	103	V_{SS}	155	V_{DD}.PAD1	207	GC5
52	V_{SS}	104	CA3	156	P009	208	GC4

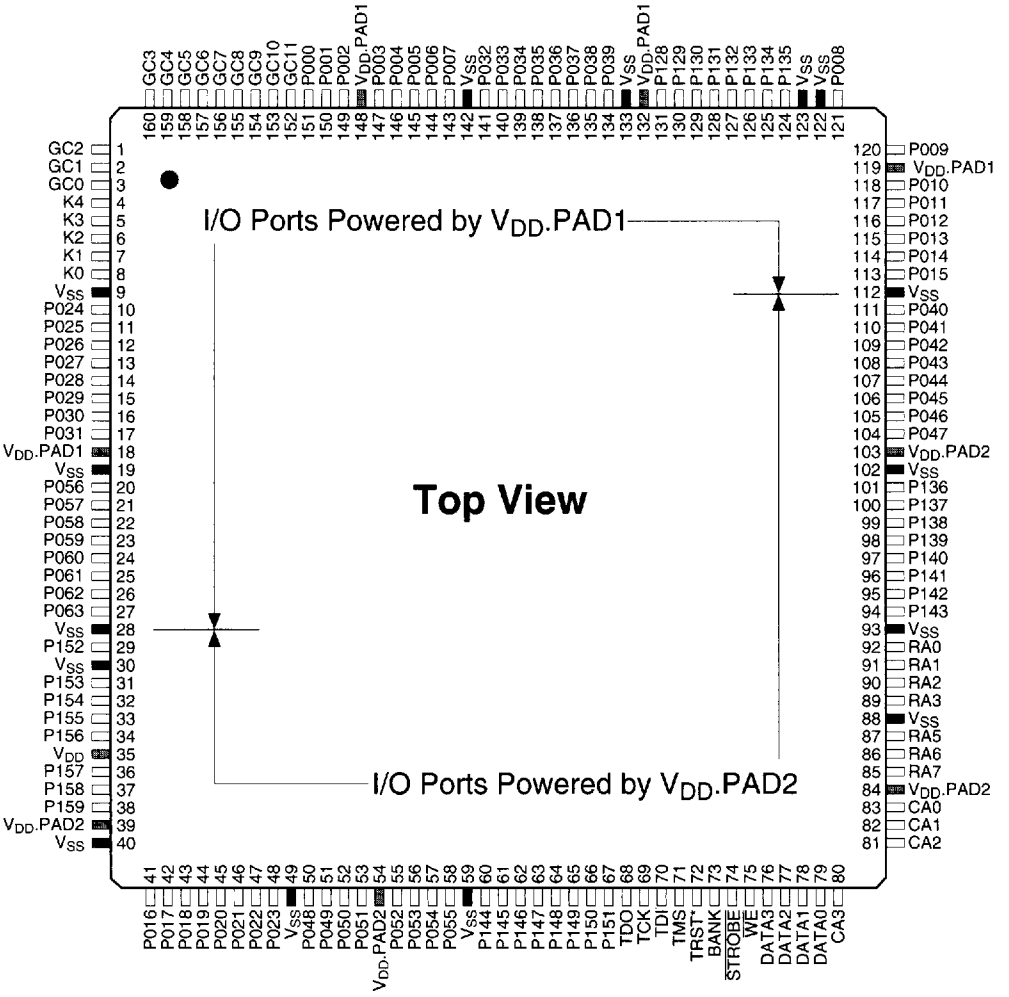
PSX96B [MQUAD/PQFP 160L Package] Pinout by Pin Location

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	GC2	41	P016	81	CA2	121	P008
2	GC1	42	P017	82	CA1	122	V_{SS}
3	GC0	43	P018	83	CA0	123	V_{SS}
4	K4	44	P019	84	V_{DD}.PAD2	124	P135
5	K3	45	P020	85	RA7	125	P134
6	K2	46	P021	86	RA6	126	P133
7	K1	47	P022	87	RA5	127	P132
8	K0	48	P023	88	V_{SS}	128	P131
9	V_{SS}	49	V_{SS}	89	RA3	129	P130
10	P024	50	P048	90	RA2	130	P129
11	P025	51	P049	91	RA1	131	P128
12	P026	52	P050	92	RA0	132	V_{DD}.PAD1
13	P027	53	P051	93	V_{SS}	133	V_{SS}
14	P028	54	V_{DD}.PAD2	94	P143	134	P039
15	P029	55	P052	95	P142	135	P038
16	P030	56	P053	96	P141	136	P037
17	P031	57	P054	97	P140	137	P036
18	V_{DD}.PAD1	58	P055	98	P139	138	P035
19	V_{SS}	59	V_{SS}	99	P138	139	P034
20	P056	60	P144	100	P137	140	P033
21	P057	61	P145	101	P136	141	P032
22	P058	62	P146	102	V_{SS}	142	V_{SS}
23	P059	63	P147	103	V_{DD}.PAD2	143	P007
24	P060	64	P148	104	P047	144	P006
25	P061	65	P149	105	P046	145	P005
26	P062	66	P150	106	P045	146	P004
27	P063	67	P151	107	P044	147	P003
28	V_{SS}	68	TDO	108	P043	148	V_{DD}.PAD1
29	P152	69	TCK	109	P042	149	P002
30	V_{SS}	70	TDI	110	P041	150	P001
31	P153	71	TMS	111	P040	151	P000
32	P154	72	TRST*	112	V_{SS}	152	GC11
33	P155	73	BANK	113	P015	153	GC10
34	P156	74	$\overline{\text{STROBE}}$	114	P014	154	GC9
35	V_{DD}	75	$\overline{\text{WE}}$	115	P013	155	GC8
36	P157	76	DATA3	116	P012	156	GC7
37	P158	77	DATA2	117	P011	157	GC6
38	P159	78	DATA1	118	P010	158	GC5
39	V_{DD}.PAD2	79	DATA0	119	V_{DD}.PAD1	159	GC4
40	V_{SS}	80	CA3	120	P009	160	GC3

PSX96B [MQUAD/PQFP 160L Package] Pinout by Pin Name

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
BANK	73	P014	114	P054	57	P158	37
CA0	83	P015	113	P055	58	P159	38
CA1	82	P016	41	P056	20	RA0	92
CA2	81	P017	42	P057	21	RA1	91
CA3	80	P018	43	P058	22	RA2	90
DATA0	79	P019	44	P059	23	RA3	89
DATA1	78	P020	45	P060	24	RA5	87
DATA2	77	P021	46	P061	25	RA6	86
DATA3	76	P022	47	P062	26	RA7	85
GC0	3	P023	48	P063	27	$\overline{\text{STROBE}}$	74
GC1	2	P024	10	P128	131	TCK	69
GC2	1	P025	11	P129	130	TDI	70
GC3	160	P026	12	P130	129	TDO	68
GC4	159	P027	13	P131	128	TMS	71
GC5	158	P028	14	P132	127	TRST*	72
GC6	157	P029	15	P133	126	V_{DD}	35
GC7	156	P030	16	P134	125	V_{DD}.PAD1	18
GC8	155	P031	17	P135	124	V_{DD}.PAD1	119
GC9	154	P032	141	P136	101	V_{DD}.PAD1	132
GC10	153	P033	140	P137	100	V_{DD}.PAD1	148
GC11	152	P034	139	P138	99	V_{DD}.PAD2	39
K0	8	P035	138	P139	98	V_{DD}.PAD2	54
K1	7	P036	137	P140	97	V_{DD}.PAD2	84
K2	6	P037	136	P141	96	V_{DD}.PAD2	103
K3	5	P038	135	P142	95	V_{SS}	30
K4	4	P039	134	P143	94	V_{SS}	88
P000	151	P040	111	P144	60	V_{SS}	123
P001	150	P041	110	P145	61	V_{SS}	9
P002	149	P042	109	P146	62	V_{SS}	19
P003	147	P043	108	P147	63	V_{SS}	28
P004	146	P044	107	P148	64	V_{SS}	40
P005	145	P045	106	P149	65	V_{SS}	49
P006	144	P046	105	P150	66	V_{SS}	59
P007	143	P047	104	P151	67	V_{SS}	93
P008	121	P048	50	P152	29	V_{SS}	102
P009	120	P049	51	P153	31	V_{SS}	112
P010	118	P050	52	P154	32	V_{SS}	122
P011	117	P051	53	P155	33	V_{SS}	133
P012	116	P052	55	P156	34	V_{SS}	142
P013	115	P053	56	P157	36	$\overline{\text{WE}}$	75

PSX96B [MQUAD/PQFP 160L Package] Pinout



Mechanical Specification

Package Dimensions

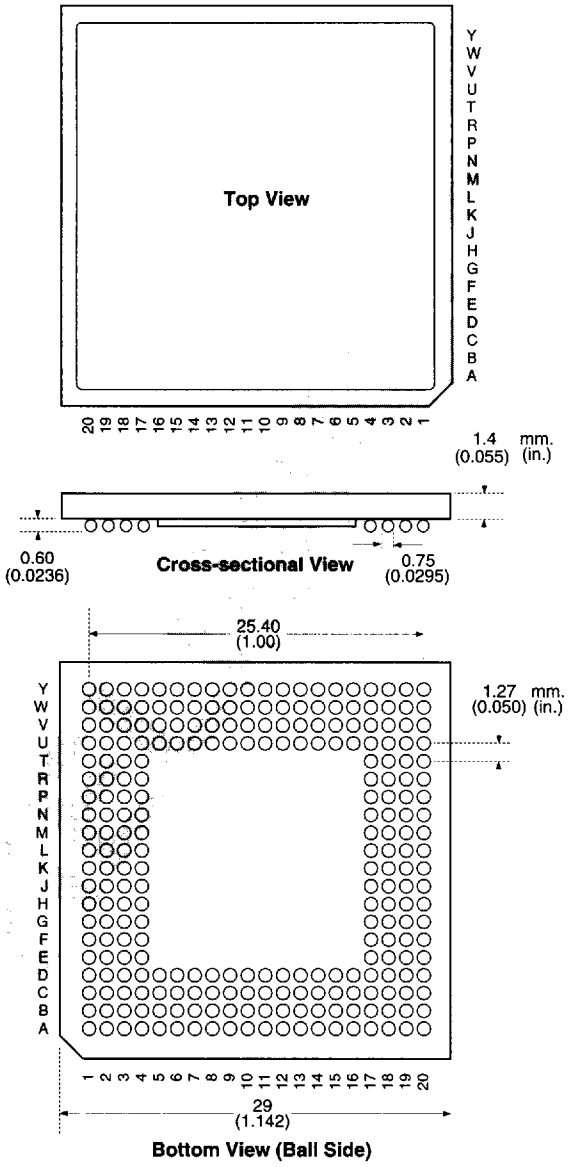


Figure 16: BGA Package Dimensions

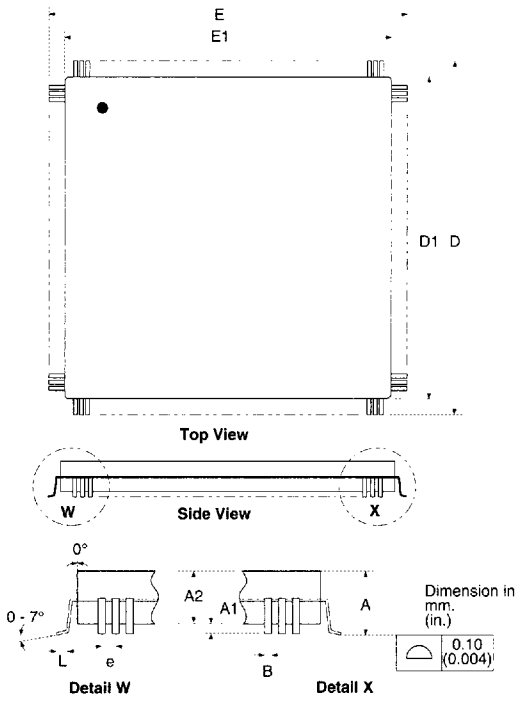


Figure 17: MQUAD Package

Package Dimension Table		MQUAD/240L		MQUAD/208L		MQUAD/160L	
		inch	mm	inch	mm	inch	mm
A	max	0.158	4.01	0.156	3.96	0.156	3.96
A1	min	0.012	0.3	0.014	0.35	0.014	0.35
	max	0.024	0.6	0.021	0.53	0.021	0.53
A2	min	0.124	3.15	0.125	3.18	0.125	3.17
	max	0.134	3.41	0.135	3.43	0.135	3.43
D	min	1.354	34.4	1.197	30.45	1.219	30.95
	max	1.370	34.8	1.213	30.86	1.238	31.45
D1	min	1.244	31.6	1.086	27.63	1.086	27.59
	max	1.248	31.7	1.094	27.83	1.094	27.79
E	min	1.354	34.4	1.197	30.45	1.219	30.95
	max	1.370	34.8	1.213	30.86	1.238	31.45
E1	min	1.244	31.6	1.086	27.63	1.086	27.59
	max	1.248	31.7	1.094	27.83	1.094	27.79
L	min	0.020	0.5	0.020	0.51	0.029	0.73
	max	0.030	0.75	0.030	0.76	0.041	1.03
B	min	0.007	0.18	0.006	0.15	0.009	0.22
	max	0.011	0.27	0.011	0.28	0.014	0.35
e	BSC.	0.0197	0.50	0.0197	0.50	0.0256	0.65

Table 7: MQUAD Package Dimensions

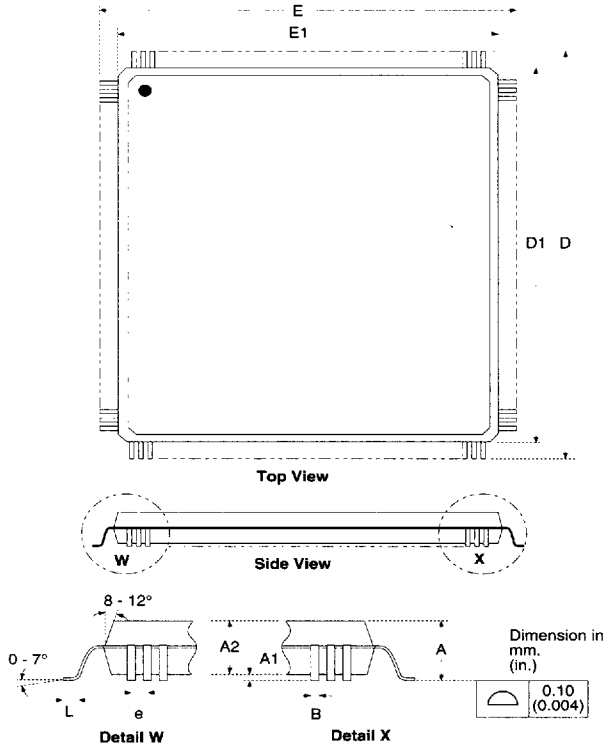


Figure 18: PQFP Package

Package Dimension Table		PQFP/240L		PQFP/208L		PQFP/160L	
		inch	mm	inch	mm	inch	mm
A	max	0.155	3.93	0.157	3.99	.160	4.07
A1	min	0.010	0.25	0.010	0.25	.010	0.25
	max	0.017	0.43	0.017	0.43	.018	0.47
A2	min	0.130	3.30	0.135	3.43	.126	3.20
	max	0.138	3.50	0.140	3.56	.142	3.60
D	min	1.354	34.40	1.195	34.40	1.219	30.95
	max	1.370	34.80	1.215	30.91	1.238	31.45
D1	min	1.256	31.90	1.098	27.93	1.098	27.90
	max	1.264	32.10	1.106	28.14	1.106	28.10
E	min	1.354	34.40	1.195	34.40	1.219	30.95
	max	1.370	34.80	1.215	30.91	1.238	31.45
E1	min	1.256	31.90	1.098	27.93	1.098	27.90
	max	1.264	32.10	1.106	28.14	1.106	28.10
L	min	0.019	0.50	0.018	0.46	0.029	0.73
	max	0.030	0.75	0.030	0.76	0.041	1.03
B	min	0.007	0.17	0.006	0.15	0.009	0.22
	max	0.011	0.27	0.011	0.28	0.014	0.35
e	BSC.	0.0197	0.50	0.0197	0.50	0.0256	0.65

Table 8: PQFP Package Dimensions

Package Thermal Resistance

Package	Pin Count	θ_{JC} (°C/W)	θ_{JA} (°C/W) Still Air	θ_{JA} (°C/W) 200 lfpm	θ_{JA} (°C/W) 400 lfpm	θ_{JA} (°C/W) 600 lfpm
PQFP	160	6.7	38.0	29.2	24.4	21.7
	208	6.6	36.6	27.4	24.0	21.4
	240	6.5	35.5	26.2	23.7	21.6
MQUAD	160	2.0	19.4	13.2	10.9	9.0
	208	3.0	14.7	11.9	10.7	9.7
	240	2.1	19.1	11.9	9.6	7.7

Table 9: Thermal Resistance of PSX Packages

Note:
Thermal performance values are based on simulation data.

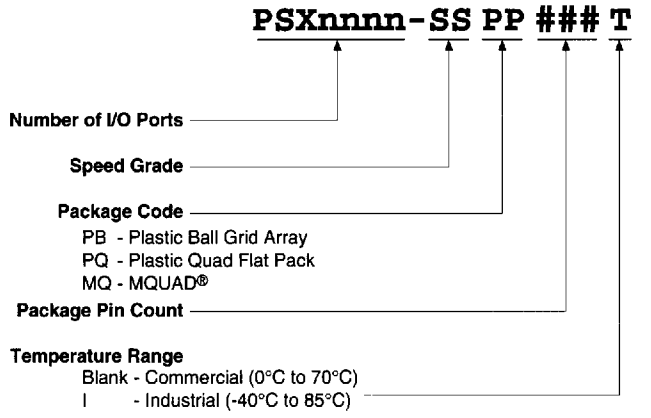
Component Availability and Ordering Information

The following table lists the PSX devices and the different package options, speed grades and operating temperature ranges that are currently available. Contact I-Cube Marketing for more up-to-date information on product availability.

Package	Pins	160		208		240		TBD
	Type	PQFP	MQUAD	PQFP	MQUAD	PQFP	MQUAD	BGA(1)
	Code	PQ160	MQ160	PQ208	MQ208	PQ240	MQ240	
PSX160	-66					C, I	C, I	C, I
	-80					C, I	C, I	C, I
	-100					C, I	C, I	C, I
	-133					C	C	C
PSX128B	-66			C, I	C, I			
	-80			C, I	C, I			
	-100			C, I	C, I			
	-133			C	C			
PSX96B	-66	C, I	C, I					
	-80	C, I	C, I					
	-100	C, I	C, I					
	-133	C	C					

Table 10: Current Component Availability

(1) Contact I-Cube Marketing for details.



PSX Family At A Glance

Device	PSX160	PSX128B	PSX96B
Number of Usable I/O	160	128	96
Switch Matrix Size	160	128	96
Pin-to-Pin Delay (ns)	7.0	7.0	7.0
NRZ Data Rate (Mbs)	160	160	160
Clock Frequency (MHz)	133	133	133
Bus Widths (bits) Number of Buses	4 8 16 32 40 20 10 5	4 8 16 32 32 16 8 4	4 8 16 32 24 12 6 3
I/O Current Drive (mA)	16	16	16
Number of General Control (GC) and Key Control Pins	13 GC 5 Key	13 GC 5 Key	12 GC 5 Key
I/O Port Modes	In/Out/Bus Repeater Registered In/Out/Bidirectional Latched In/Out/Bidirectional Tristate In/Out/Bidirectional	In/Out/Bus Repeater Registered In/Out/Bidirectional Latched In/Out/Bidirectional Tristate In/Out/Bidirectional	In/Out/Bus Repeater Registered In/Out/Bidirectional Latched In/Out/Bidirectional Tristate In/Out/Bidirectional
Process (µm)	0.6	0.6	0.6
Core Voltage (V)	5	5	5
I/O Voltage (V)	3 and 5	3 and 5	3 and 5
Package(s)	240 MQUAD 240PQFP BGA	208 MQUAD 208PQFP	160 MQUAD 160PQFP

I-Cube, Inc.

2328-C Walsh Avenue
Santa Clara, CA 95051, USA

Phone: ++ (408) 986-1077
Fax: ++ (408) 986-1629
email: marketing@icube.com
Internet: http://www.icube.com

PSX Family Data Sheet
[v 2.0]
February 1996
Document #D-11-013