MOS INTEGRATED CIRCUIT
μPD42S16900L,42S17900L

16M BIT DYNAMIC RAM
(3.3V FAST PAGE MODE)
PRELIMINARY

DESCRIPTION

The NEC μPD42S16900L and μPD42S17900L are 2 097 152 words by 9 bits dynamic CMOS RAM with optional fast page mode. CMOS sense amplifier, peripheral circuits and 1 transistor memory cell technique realize high speed access, cycle time and low power dissipation.

Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles or normal read or write cycles on the 4096 address combinations of A0 to A11 (for μPD42S16900L) or 2048 address combinations of A0 to A10 (for μPD42S17900L) during a 256 ms period.

The μPD42S16900L and μPD42S17900L are packaged in 32-pin plastic SOJ and 32-pin plastic ZIP and 32-pin plastic TSOP.

FEATURES

- 2 097 152 words by 9 bits organization
- 4 performance ranges

DEVICE	ACCESS TIME (MAX.)	R/W CYCLE (MIN.)	PAGE MODE CYCLE (MIN.)	Low power dissipation	
				Active (MAX.)	Standby
μPD42S16900L-A60	60 ns	110 ns	40 ns	324 mW	0.36 mW (MAX.) (CMOS level)
μPD42S17900L-A60				396 mW	
μPD42S16900L-A70	70 ns	130 ns	45 ns	288 mW	
μPD42S17900L-A70				360 mW	
μPD42S16900L-A80	80 ns	150 ns	50 ns	252 mW	
μPD42S17900L-A80				324 mW	

- Single +3.3V±0.3V power supply
- On-chip substrate bias generator
- Multiplexed address inputs

DEVICE	Row Address	Column Address	Refresh cycle
μPD42S16900L	A0 to A11	A0 to A8	4096 cycles/256 ms
μPD42S17900L	A0 to A10	A0 to A9	2048 cycles/256 ms

- Non latched I/O, TTL-compatible
- Read-modify-write, Fast Page Mode capability
- $\overline{RAS}$ only refresh, hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ internal address refresh
- $\overline{CAS}$ before $\overline{RAS}$ self refresh

ORDERING INFORMATION

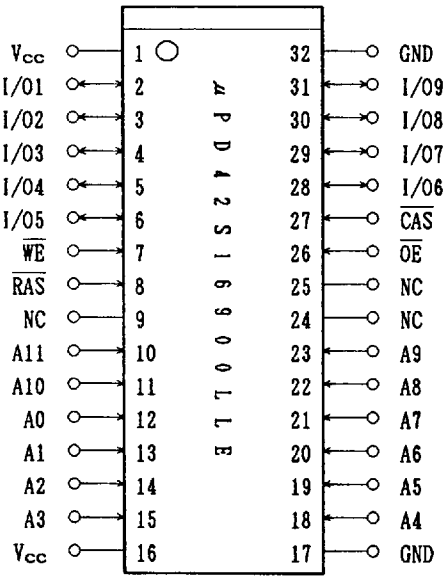
PART NUMBER	ACCESS TIME (MAX.)	PACKAGE	QUALITY GRADE
μPD42S16900LLE-A60	60ns	32-pin Plastic SOJ	STANDARD
μPD42S17900LLE-A60			
μPD42S16900LLE-A70	70ns		
μPD42S17900LLE-A70			
μPD42S16900LLE-A80	80ns		
μPD42S17900LLE-A80			
μPD42S16900LV-A60	60ns	32-pin Plastic ZIP (under development)	
μPD42S17900LV-A60			
μPD42S16900LV-A70	70ns		
μPD42S17900LV-A70			
μPD42S16900LV-A80	80ns		
μPD42S17900LV-A80			
μPD42S16900LG5-A60-7JD	60ns	32-pin Plastic TSOP	
μPD42S17900LG5-A60-7JD			
μPD42S16900LG5-A70-7JD	70ns		
μPD42S17900LG5-A70-7JD			
μPD42S16900LG5-A80-7JD	80ns		
μPD42S17900LG5-A80-7JD			
μPD42S16900LG5-A60-7KD	60ns	32-pin Plastic TSOP (Reverse bent)	
μPD42S17900LG5-A60-7KD			
μPD42S16900LG5-A70-7KD	70ns		
μPD42S17900LG5-A70-7KD			
μPD42S16900LG5-A80-7KD	80ns		
μPD42S17900LG5-A80-7KD			

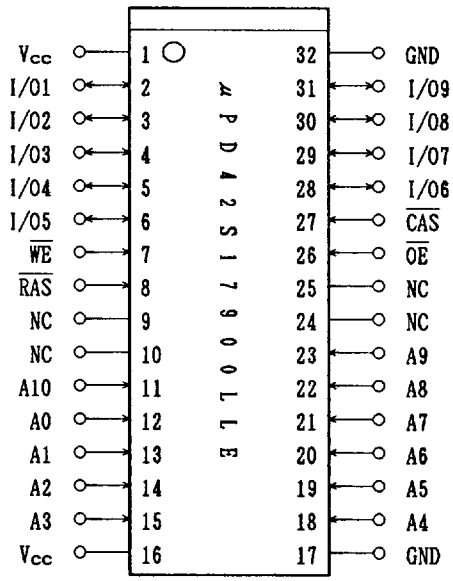
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATION (Marking Side)

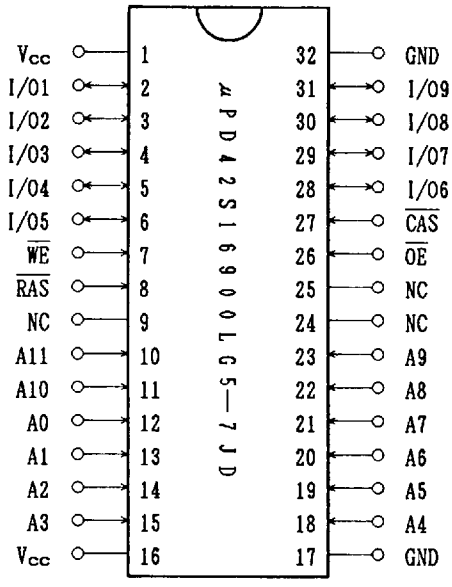
A0 to A10(A11)	: Address Inputs
I/O1 to I/O9	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{CAS}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
V_{CC}	: Supply Voltage
GND	: Ground
NC	: No Connection

32-pin Plastic SOJ (400 mil)

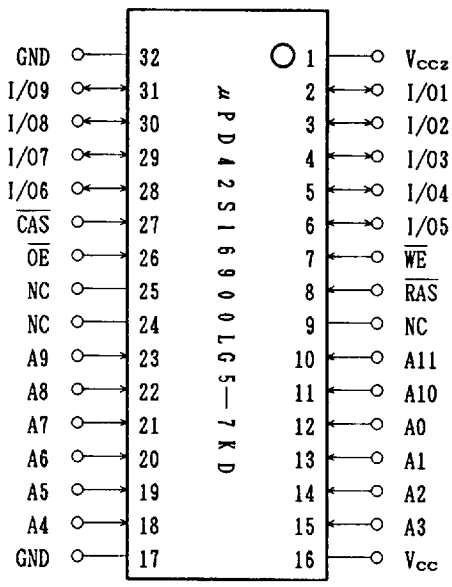


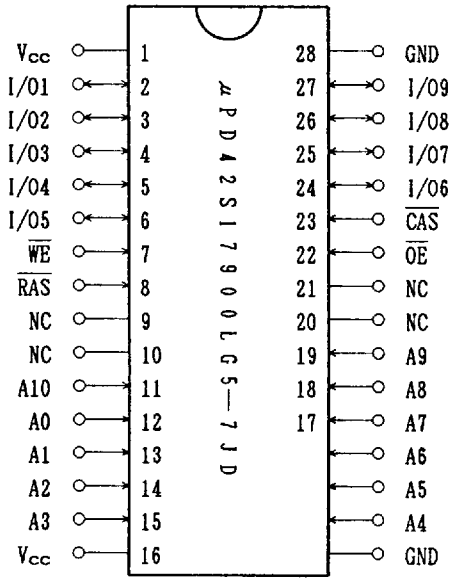


32-pin Plastic TSOP (400 mil)

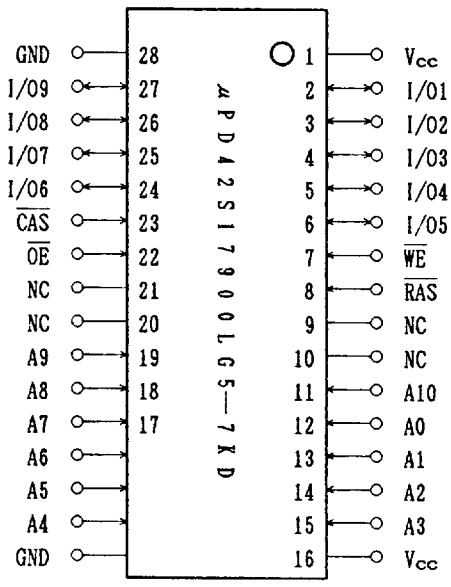


Reverse bent

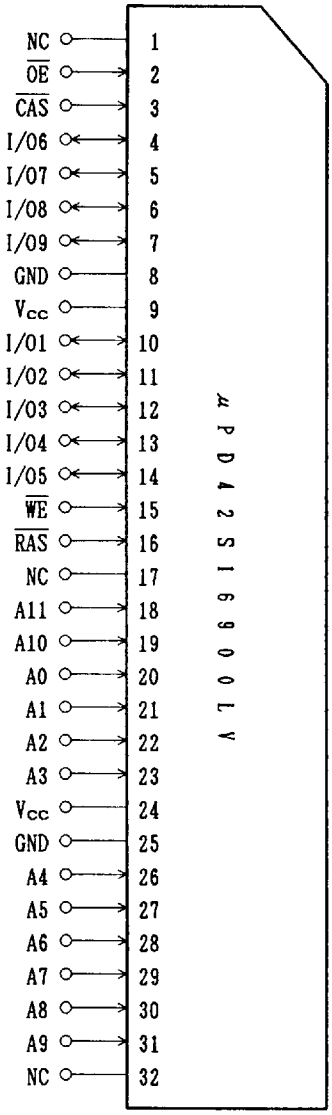


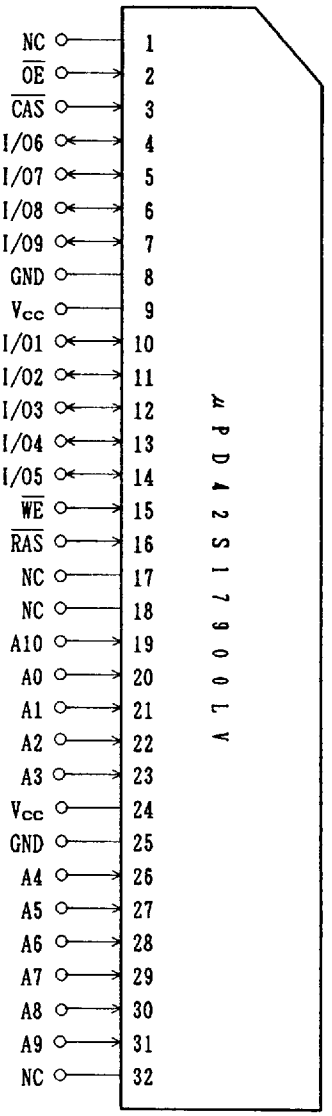


Reverse bent



32-pin Plastic ZIP (475 mil)





ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	TEST CONDITION	RATING	UNIT
Voltage on Any Pin Relative to GND	V_T		-0.5 to +4.6	V
Short Circuit Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to 70	℃
Storage Temperature	T_{stg}		-55 to +125	℃

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS NOTES:1,2

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		V_{CC}+0.3	V
Low Level Input Voltage	V_{IL}		-0.3		0.8	V
Ambient Temperature	Ta		0		70	℃

CAPACITANCE (T_a=25 °C, f=1 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_{I1}	A0 to A10(A11)			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	C_D	I/O1 to I/O9			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless Otherwise noted)

【μPD42S16900L】

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	NOTES
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}$, I_O=0mA	μPD42S16900L-A60			90	mA	3
			μPD42S16900L-A70			80		
			μPD42S16900L-A80			70		
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}\geq V_{IH(MIN.)}$, I_O=0mA				0.5	mA	
		$\overline{RAS}$, $\overline{CAS}\geq V_{CC}$-0.2V, I_O=0mA				0.1		
Refresh Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}\geq V_{IH(MIN.)}$ $t_{RC}=t_{RC(MIN.)}$, I_O=0mA	μPD42S16900L-A60			90	mA	3
			μPD42S16900L-A70			80		
			μPD42S16900L-A80			70		
Operating Current (Fast Page Mode)	I_{CC4}	$\overline{CAS}$ Cycling, $\overline{RAS}\leq V_{IL(MAX.)}$ $t_{PC}=t_{PC(MIN.)}$, I_O=0mA	μPD42S16900L-A60			70	mA	3
			μPD42S16900L-A70			60		
			μPD42S16900L-A80			50		
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC}=t_{RC(MIN.)}$, I_O=0mA	μPD42S16900L-A60			90	mA	3
			μPD42S16900L-A70			80		
			μPD42S16900L-A80			70		
Battery back-up Current (Standby with $\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	Standby: V_{CC}-0.2V≦$\overline{RAS}$, $\overline{CAS}$ before $\overline{RAS}$ Refresh: 4096 Cycle/256 ms $\overline{RAS}$, $\overline{CAS}$: 0V≦V_{IL}≦0.2V V_{CC}-0.2V≦V_{IH}≦V_{IH} MAX. $\overline{WE}$, $\overline{OE}$: V_{IH} Address: Don't care Output: OPEN	t_{RAS}≦300ns			140	μA	
			t_{RAS}≦1μs			140		
Self Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: 0V≦V_{IL}≦0.2V V_{CC}-0.2V≦V_{IH}≦V_{IH} MAX. I_O=0mA				80	μA	
Input Leakage Current	$I_{I(L)}$	V_I=0 to 3.6V, all other pins= 0V		-5		5	μA	
Output Leakage Current	$I_{O(L)}$	D_{OUT} is disabled, V_O=0 to 3.6V		-5		5	μA	
Output High Voltage	V_{OH}	I_O=-2mA		2.4			V	
Output Low Voltage	V_{OL}	I_O=2mA				0.4	V	

【μPD42S17900L】

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	NOTES
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}$, I_O=0mA	μPD42S17900L-A60			110	mA	3
			μPD42S17900L-A70			100		
			μPD42S17900L-A80			90		
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}\geq V_{IH(MIN.)}$, I_O=0mA				0.5	mA	
		$\overline{RAS}$, $\overline{CAS}\geq V_{CC}$-0.2V, I_O=0mA				0.1		
Refresh Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}\geq V_{IH(MIN.)}$ $t_{RC}=t_{RC(MIN.)}$, I_O=0mA	μPD42S17900L-A60			110	mA	3
			μPD42S17900L-A70			100		
			μPD42S17900L-A80			90		
Operating Current (Fast Page Mode)	I_{CC4}	$\overline{CAS}$ Cycling, $\overline{RAS}\leq V_{IL(MAX.)}$ $t_{PC}=t_{PC(MIN.)}$, I_O=0mA	μPD42S17900L-A60			70	mA	3
			μPD42S17900L-A70			60		
			μPD42S17900L-A80			50		
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC}=t_{RC(MIN.)}$, I_O=0mA	μPD42S17900L-A60			110	mA	3
			μPD42S17900L-A70			100		
			μPD42S17900L-A80			90		
Battery back-up Current (Standby with $\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	Standby: V_{CC}-0.2V≦$\overline{RAS}$, $\overline{CAS}$ before $\overline{RAS}$ Refresh: 4096 Cycle/256 ms $\overline{RAS}$, $\overline{CAS}$: 0V≦V_{IL}≦0.2V V_{CC}-0.2V≦V_{IH}≦V_{IH} MAX. $\overline{WE}$, $\overline{OE}$: V_{IH} Address: Don't care Output: OPEN	$t_{RAS}\leq$300ns			120	μA	
			$t_{RAS}\leq$1μs			120		
Self Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: 0V≦V_{IL}≦0.2V V_{CC}-0.2V≦V_{IH}≦V_{IH} MAX. I_O=0mA				80	μA	
Input Leakage Current	$I_{I(L)}$	V_I=0 to 3.6V, all other pins= 0V		-5		5	μA	
Output Leakage Current	$I_{O(L)}$	D_{OUT} is disabled, V_O=0 to 3.6V		-5		5	μA	
Output High Voltage	V_{OH}	I_O=-2mA		2.4			V	
Output Low Voltage	V_{OL}	I_O=2mA				0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless Otherwise noted) **NOTES:2,4,5**

(1/2)

PARAMETER	SYMBOL	μPD42S16900L-A60 μPD42S17900L-A60		μPD42S16900L-A70 μPD42S17900L-A70		μPD42S16900L-A80 μPD42S17900L-A80		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	110		130		150		ns	6
Read Write Cycle Time	t_{RWC}	160		180		200		ns	6
Fast Page Mode Cycle Time(Read or Write)	t_{PC}	40		45		50		ns	6
Read Modify Write Cycle Time(Fast Page Mode)	t_{PRWC}	85		90		100		ns	6
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	7,8
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		15		18		20	ns	7,8
Access Time from Column Address	t_{AA}		30		35		40	ns	7,8
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	7
Access Time from $\overline{OE}$	t_{OEA}		15		18		20	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	8
$\overline{CAS}$-Data Set-up Time	t_{CLZ}	0		0		0		ns	7
$\overline{OE}$-Data Set-up Time	t_{OLZ}	0		0		0		ns	7
Output Buffer Turn-off Delay ($\overline{CAS}$)	t_{OFF}	0	13	0	15	0	15	ns	9
$\overline{OE}$ Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay ($\overline{OE}$)	t_{OEZ}	0	13	0	15	0	15	ns	9
$\overline{OE}$ Command Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Set-up Time	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width (Random Read,Write Cycle)	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125000	70	125000	80	125000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	18	10000	20	10000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	10
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Set-up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	

(2/2)

PARAMETER	SYMBOL	μPD42S16900L-A60 μPD42S17900L-A60		μPD42S16900L-A70 μPD42S17900L-A70		μPD42S16900L-A80 μPD42S17900L-A80		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Column Address Set-up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Set-up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	11
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	11
Write Command Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	12
Write Command Pulse Width	t_{WP}	10		10		15		ns	12
Data-in Set-up Time	t_{DS}	0		0		0		ns	13
Data-in Hold Time	t_{DH}	10		15		15		ns	13
$\overline{WE}$ Command Set-up Time	t_{WCS}	0		0		0		ns	14
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	38		43		45		ns	15
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	83		95		105		ns	15
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	53		60		65		ns	15
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20		20		20		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Set-up Time for CBR Refresh	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time for CBR Refresh	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time (Self Refresh Cycle)	t_{CHS}	-50		-50		-50		ns	
$\overline{WE}$ Set-up Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Period	t_{REF}		256		256		256	ms	16

NOTES:

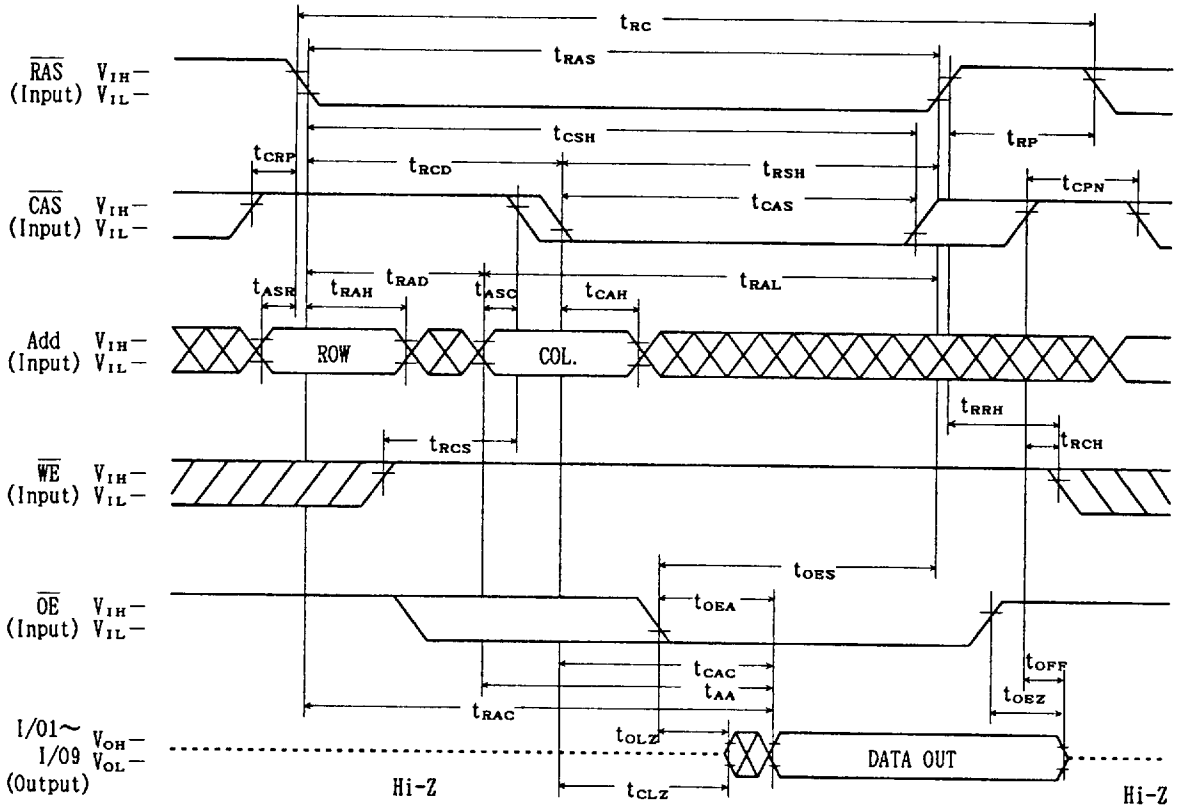
1. All voltages referenced to GND.
2. An initial pause of 100μs required after power-on followed by 8 refresh ($\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) cycles before proper device operation is achieved.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC3} is measured on condition that column addresses in $\overline{RAS}$ only cycle are held high or low level and I_{CC4} is measured on condition that column addresses in fast page mode are changed only one time during $t_{PC(MIN.)}$.
4. AC measurements assume t_T=5ns
5. $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (Ta=0 to 70℃) is assured.
7. Load = 1 TTL loads and 100pF (V_{OH}=2.0V, V_{OL}=0.8V)
8. The access time is determined by $\overline{RAS}$ access time t_{RAC}, address access time t_{AA}, and $\overline{CAS}$ address time t_{CAC}. The relationship between these access time and t_{RCD}, t_{RAD} is as follows.

CONDITION	ACCESS TIME
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} \geqq t_{RAD(MAX.)}$	$t_{AA(MAX.)}$
$t_{RCD} \geqq t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$

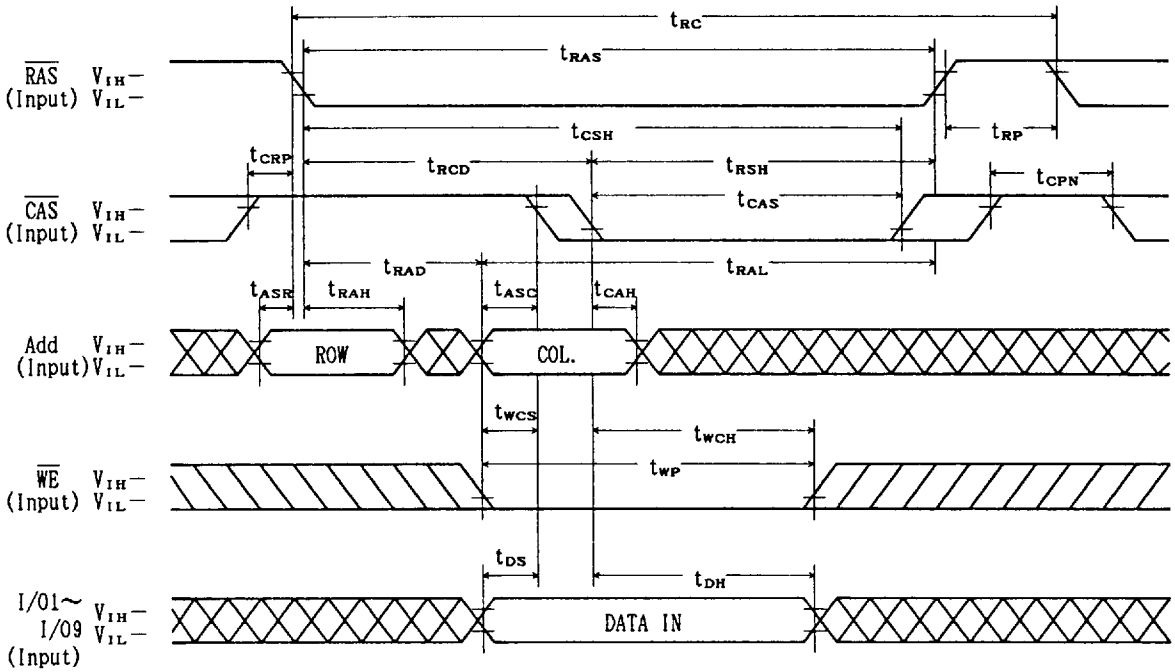
9. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
10. t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycles.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. t_{WP} is applicable for late write cycle. If the cycle is early write, it should be satisfied value of t_{WCH}.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in late write or read-modify-write cycles.
14. If $t_{WCS} \geqq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle.
15. If $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$ the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
16. How to enter into $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.
    - In case of using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh
      Refresh 2048 or 4096 times during a 256ms (Before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode, and after reset).
    - In case of using burst $\overline{CAS}$ before $\overline{RAS}$ refresh
      Refresh 2048 times during a 32ms (μPD42S17900L) or 4096 times during a 64ms (μPD42S16900L) (Before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode, and after reset).
    - In case of use $\overline{RAS}$ only refresh
      Refresh against all refresh address during 32ms (μPD42S17900L) or 64ms (μPD42S16900L) (Before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode, and after reset).

TIMING DIAGRAMS

READ CYCLE

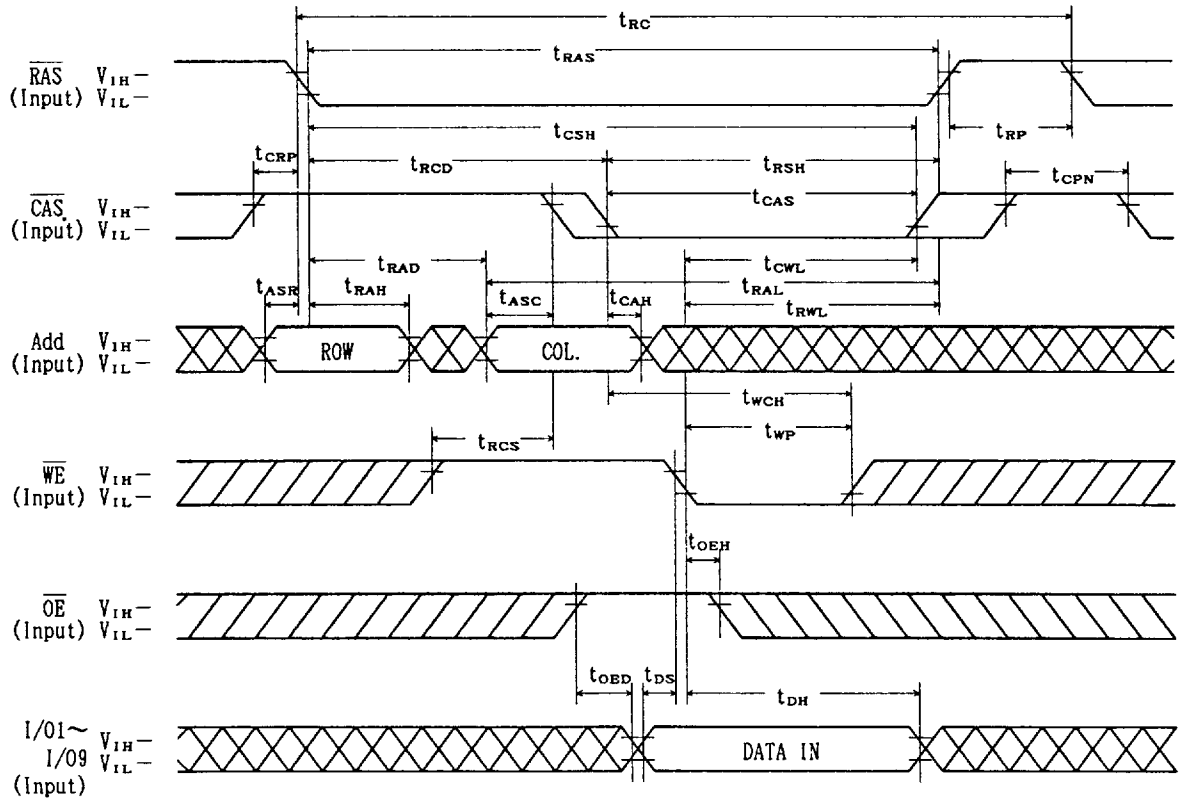


EARLY WRITE CYCLE

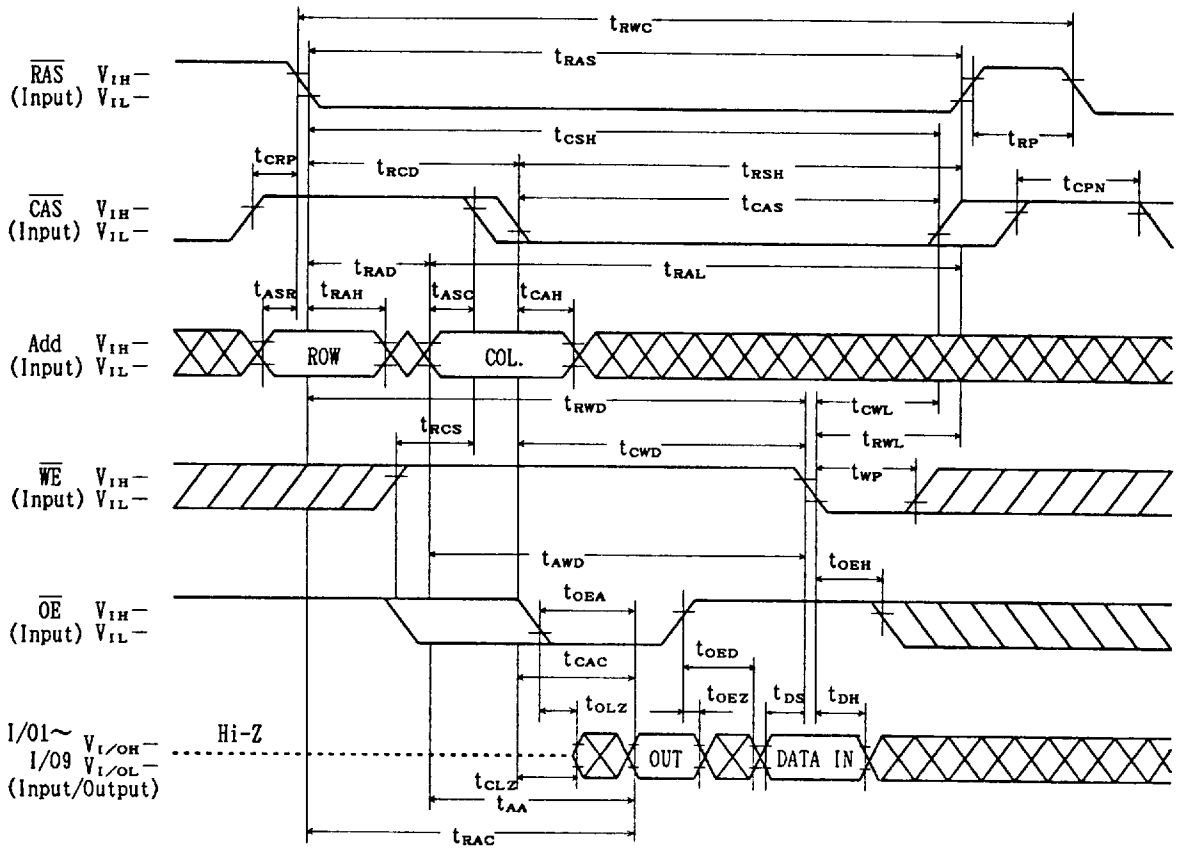


Note : $\overline{OE}$ = Don't care

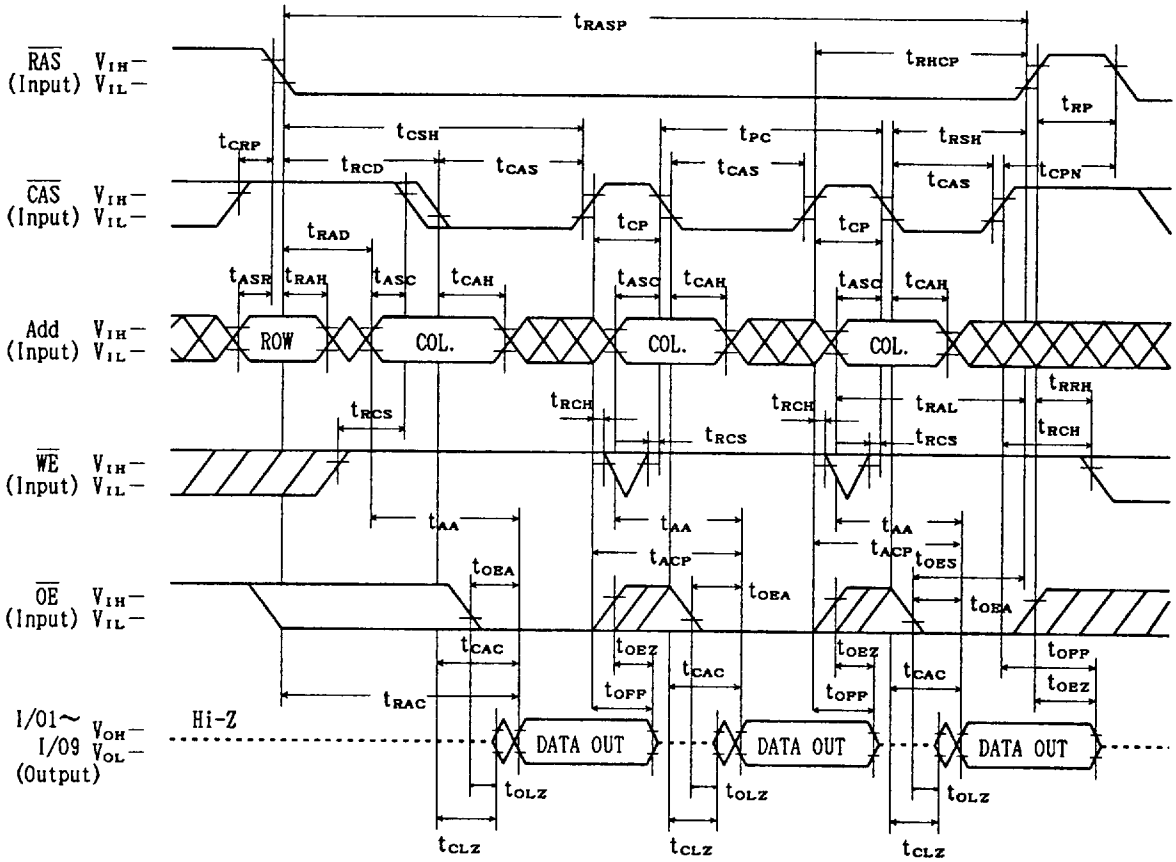
LATE WRITE CYCLE



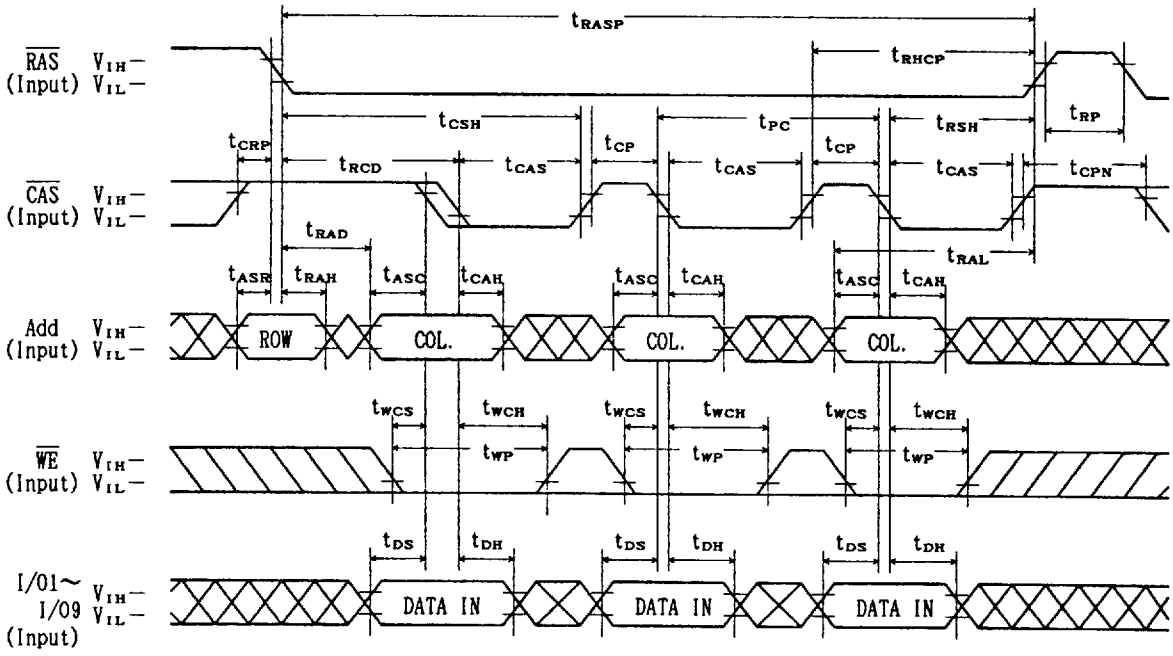
READ MODIFY WRITE CYCLE



FAST PAGE MODE READ CYCLE

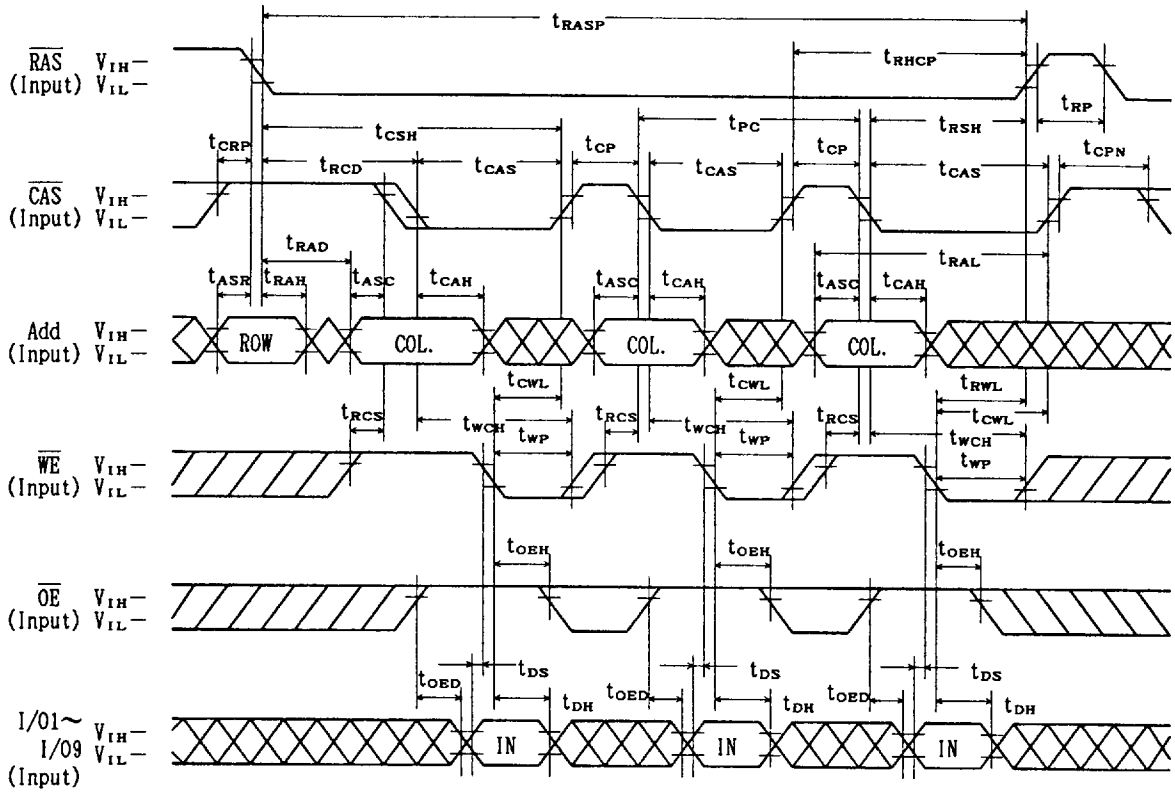


FAST PAGE MODE EARLY WRITE CYCLE

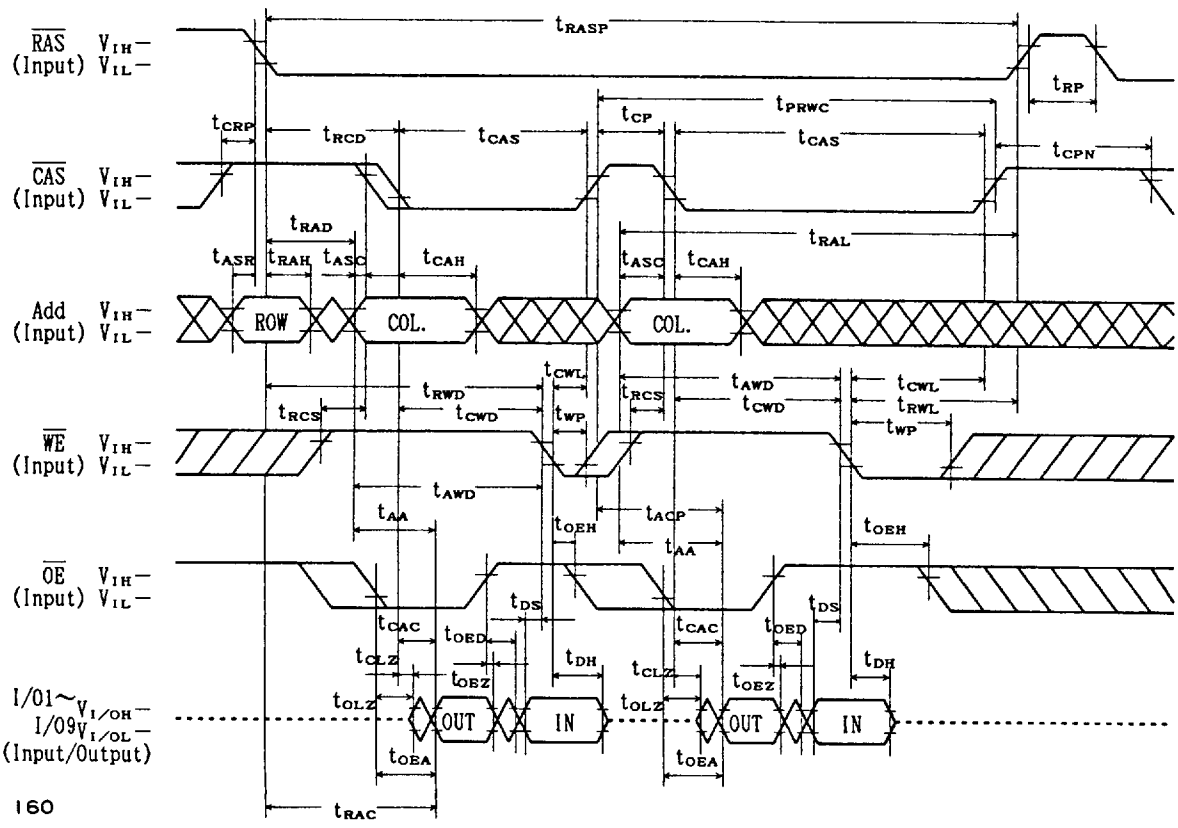


Note : $\overline{OE}$ = Don't care

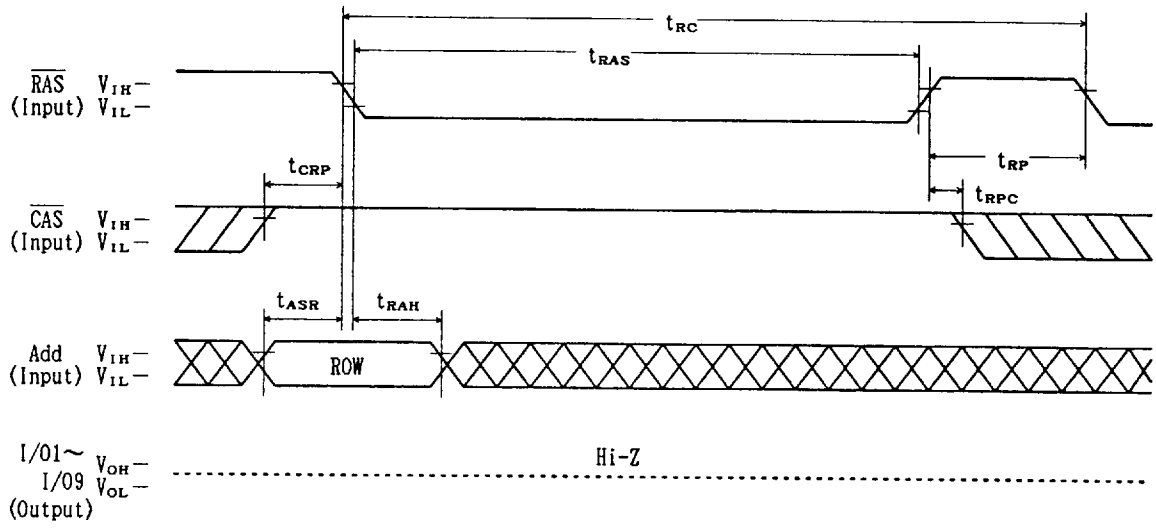
FAST PAGE MODE LATE WRITE CYCLE



FAST PAGE MODE READ MODIFY WRITE CYCLE

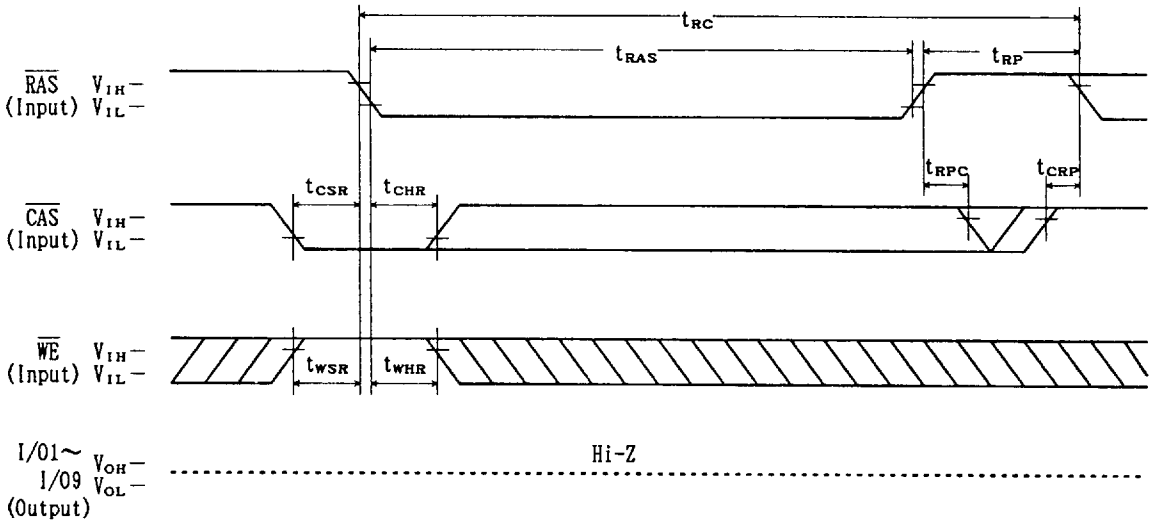


$\overline{RAS}$ ONLY REFRESH CYCLE



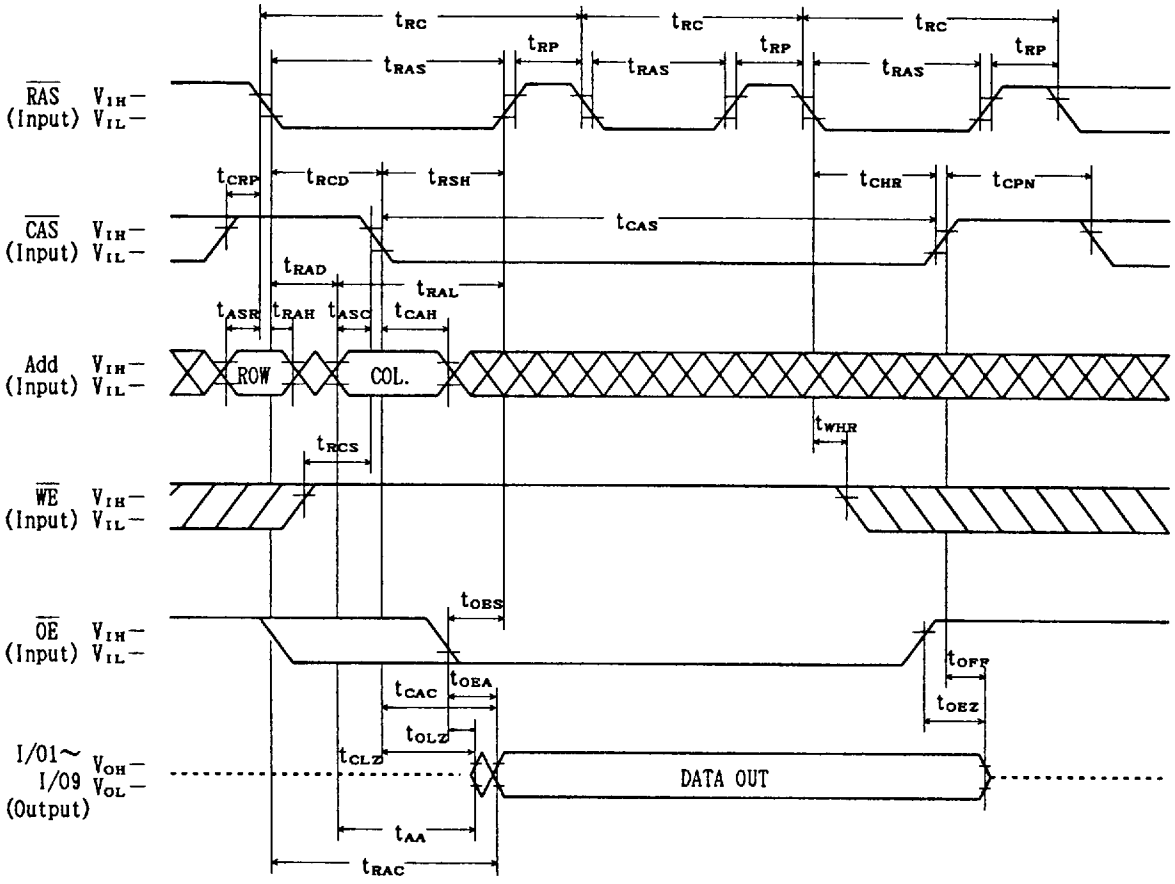
Note : $\overline{WE}$, $\overline{OE}$ = Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

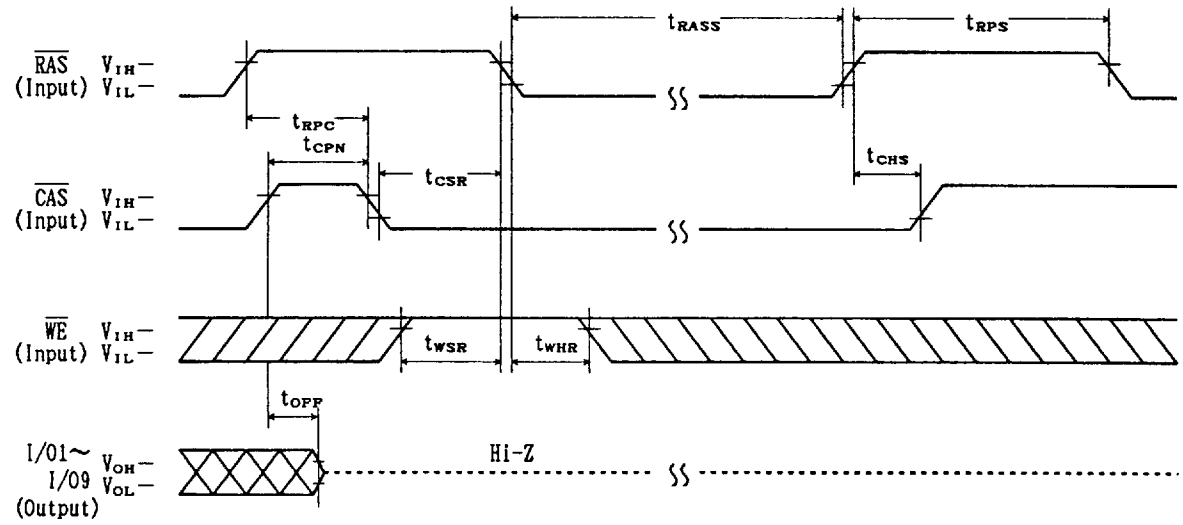


Note : $\overline{OE}$ = Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ HIDDEN REFRESH CYCLE

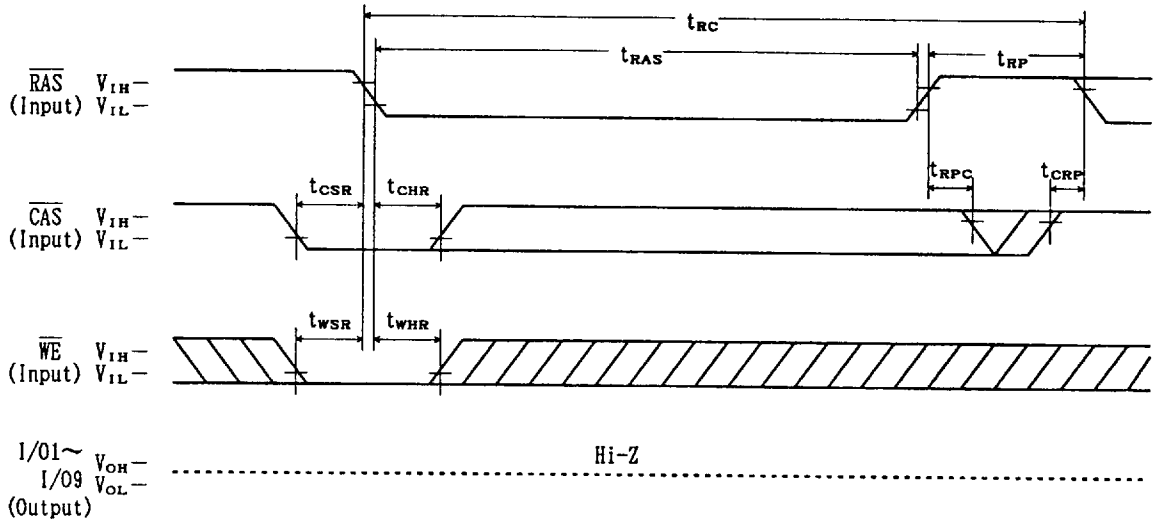


$\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE



TEST MODE SET CYCLE

(WE AND CAS BEFORE RAS REFRESH CYCLE)



TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/2. In this TEST MODE, internal organization is 1M words by 18-bit apparentry. The input levels of the CAS input A0 are Don't care.

1. How to enter into TEST MODE

Through TEST MODE SET CYCLE (WE and CAS before RAS refresh cycle), the device is entered into TEST MODE.

2. Write/Read in TEST MODE

Write data "1" or "0" through I/01 to I/09 by controlling address except for above-mentioned adress. Each input data through each I/O (I/01, I/02, I/03, I/04, I/05, I/06, I/07, I/08, I/09) write 2 bits at once. And read through I/01 to I/08 to check written data. In case of writing each 2 bits rightly, each I/O data is "1". But wrong, each I/O data is "0".

3. Refresh in TEST MODE

Use normal read cycle or WE and CAS before RAS refresh cycle.

4. How to reset TEST MODE

Through RAS only refresh cycle or CAS before RAS refresh cycle, the device is reset TEST MODE.

3. PACKAGE DRAWINGS

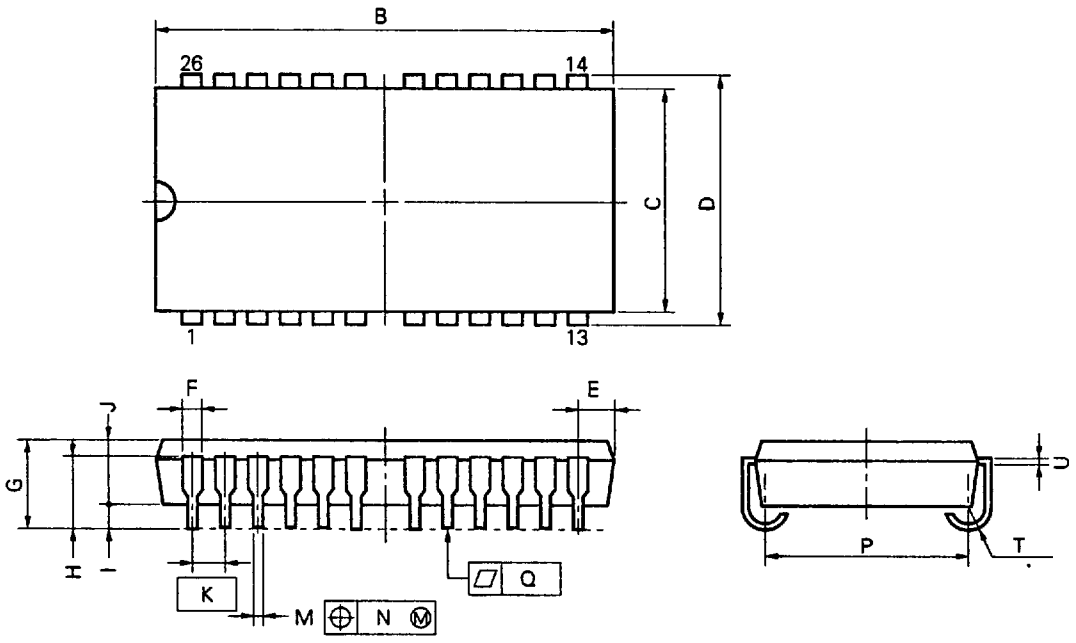
* : under development

PAGE(S) INTENTIONALLY BLANK

26 PIN PLASTIC SOJ (300mil)

24 Leads

NEC Cord:S26LA-300A



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

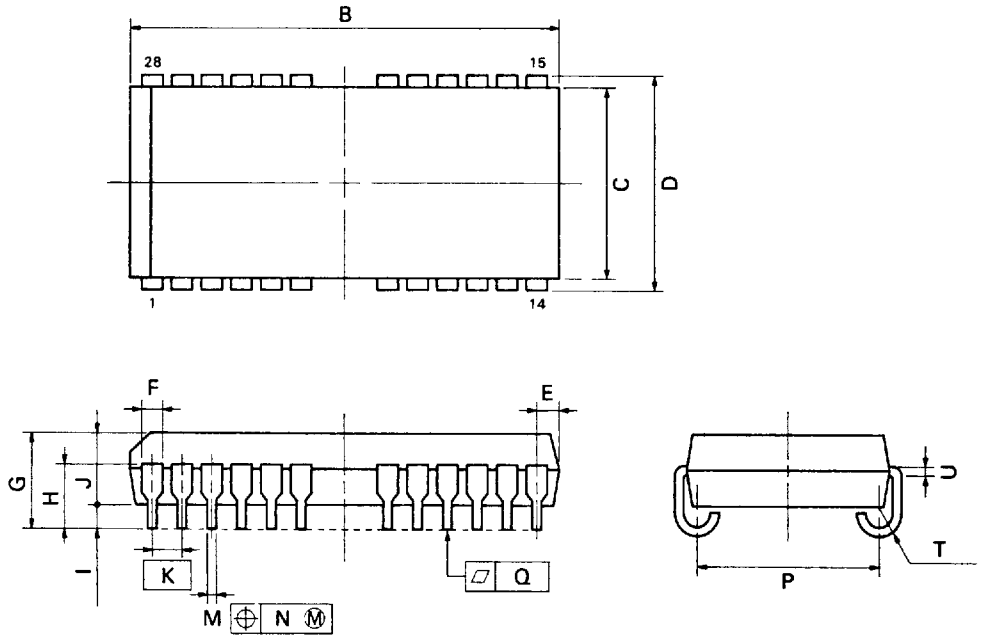
S26LA-300A

ITEM	MILLIMETERS	INCHES
B	$17.1^{+0.25}_{-0.05}$	$0.673^{+0.010}_{-0.002}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

28 PIN PLASTIC SOJ (400mil)

24 Leads

NEC Cord:P28LE-400A



P28LE-400A

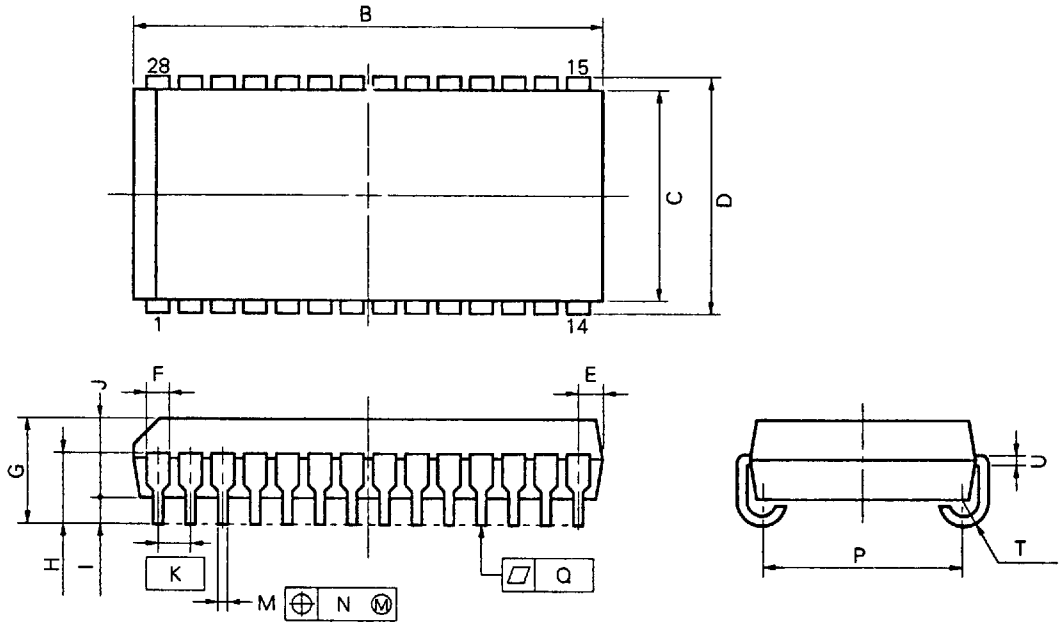
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	18.67 $^{+0.2}_{-0.35}$	0.735 $^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18 $^{\pm 0.2}$	0.440 $^{+0.008}_{-0.007}$
E	1.08 $^{\pm 0.15}$	0.043 $^{+0.006}_{-0.007}$
F	0.7	0.028
G	3.5 $^{\pm 0.2}$	0.138 $^{+0.008}_{-0.007}$
H	2.4 $^{\pm 0.2}$	0.094 $^{+0.009}_{-0.008}$
I	0.8 MIN	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 $^{\pm 0.10}$	0.016 $^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40 $^{\pm 0.20}$	0.370 $^{+0.008}_{-0.007}$
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 $^{+0.10}_{-0.05}$	0.008 $^{+0.004}_{-0.002}$

28 PIN PLASTIC SOJ (400mil)
28 Leads

NEC Cord:P28LE-400A1



NOTE

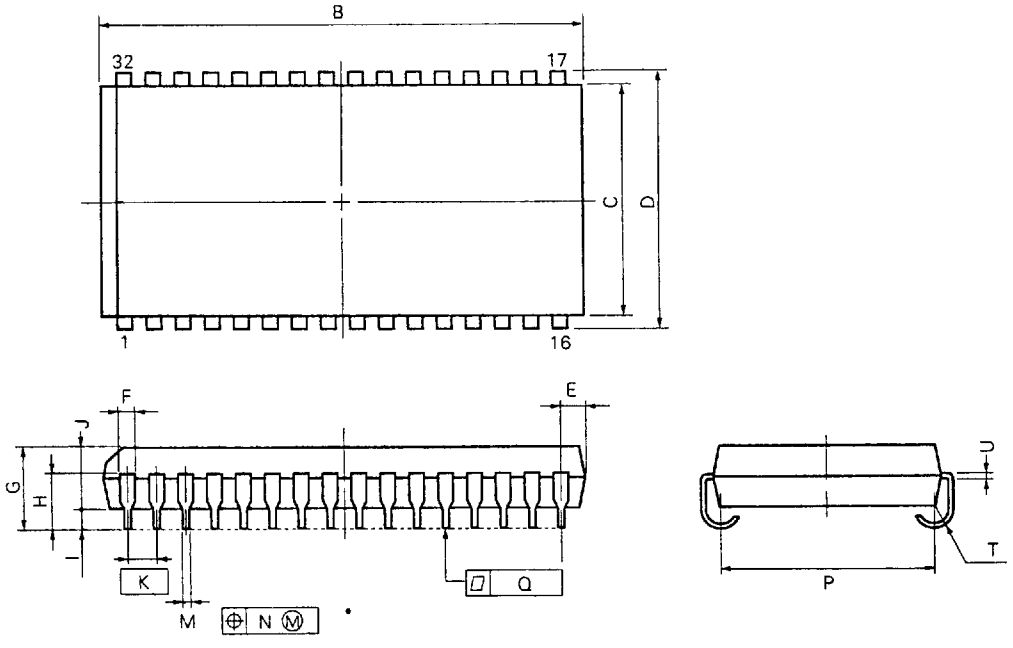
Each lead centerline is located within 0.12 mm (0 005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0\ 2}_{-0\ 35}$	$0.735^{+0\ 008}_{-0\ 013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0\ 008}_{-0\ 007}$
E	1.08±0.15	$0.043^{+0\ 006}_{-0\ 007}$
F	0.74	0.029
G	3.5±0.2	$0.138^{+0\ 008}_{-0\ 007}$
H	2.545±0.2	0.100±0.008
I	0.8 MIN	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P)	0 050 (T.P.)
M	0 40±0.10	$0.016^{+0\ 004}_{-0\ 005}$
N	0.12	0.005
P	9 40±0.20	$0.370^{+0\ 008}_{-0\ 007}$
Q	0.10	0.004
T	R 0 85	R 0.033
U	$0\ 20^{+0\ 10}_{-0\ 05}$	$0\ 008^{+0\ 004}_{-0\ 002}$

32 PIN PLASTIC SOJ (400mil)

NEC Cord:P32LE-400A



NOTE

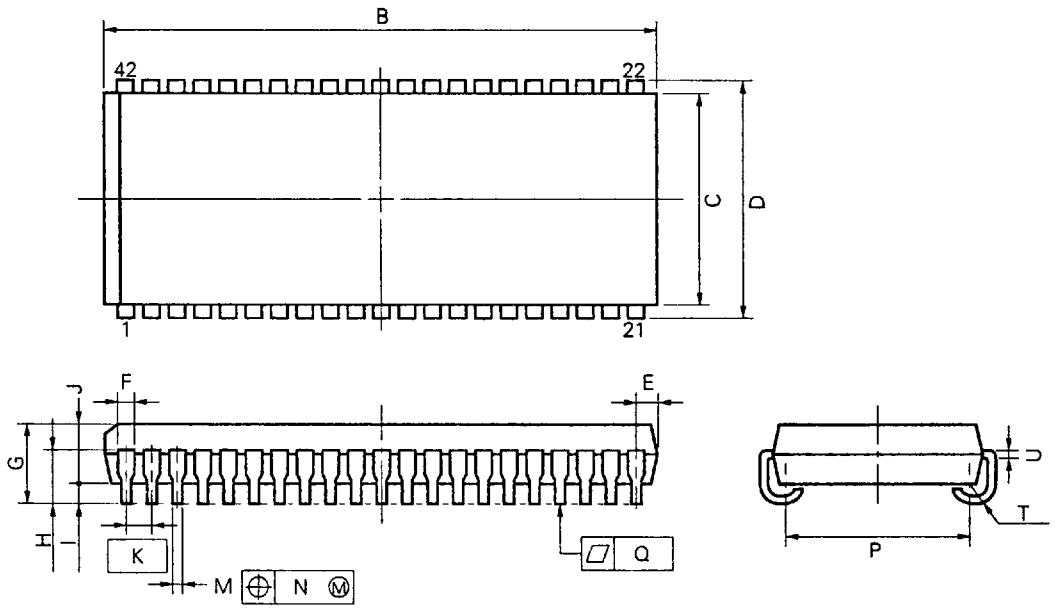
Each lead centerline is located within 0 12 mm (0 005 inch) of its true position (T P) at maximum material condition

P32LE-400A

ITEM	MILLIMETERS	INCHES
B	21.06±0 2	0 829±0 008
C	10 16	0 400
D	11 18±0 2	0.440±0 008
E	1 005±0.1	$0\ 040^{+0\ 004}_{-0\ 005}$
F	0.74	0 029
G	3.5±0.2	0 138±0 008
H	2 545±0 2	0 100±0.008
I	0 8 MIN	0 031 MIN
J	2 6	0.102
K	1 27 (T.P.)	0 050 (T P.)
M	0 40±0 10	$0\ 016^{+0\ 004}_{-0\ 005}$
N	0.12	0 005
P	9 4±0 20	0 370±0 008
Q	0.1	0.004
T	R 0 85	R 0.033
U	$0.20^{+0\ 10}_{-0\ 05}$	$0\ 008^{+0\ 004}_{-0\ 002}$

42 PIN PLASTIC SOJ (400mil)

NEC Cord:P42LE-400A



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

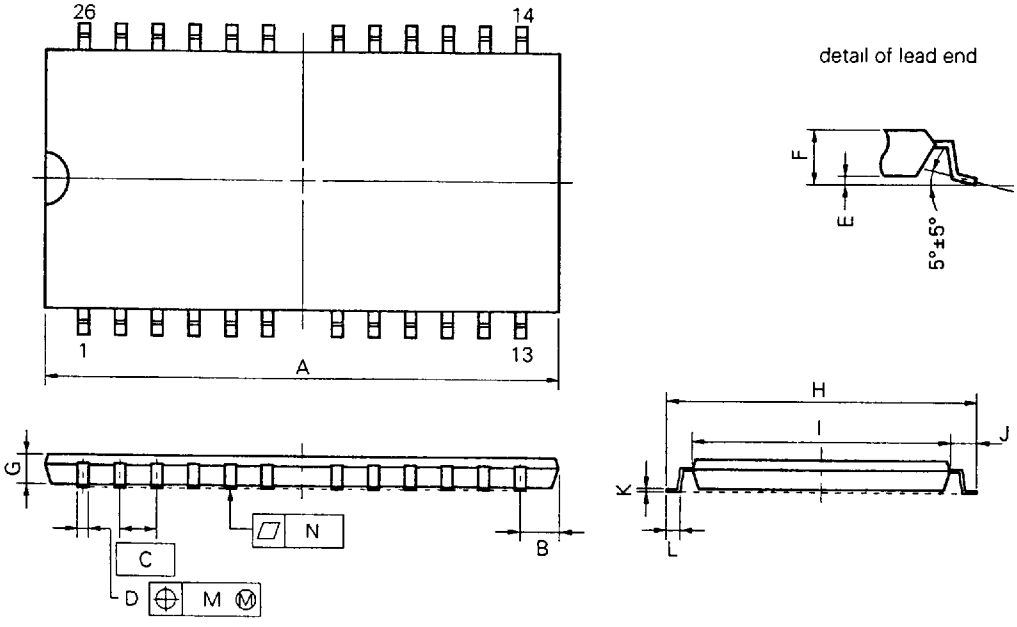
P42LE-400A

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0 033
U	$0\ 20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

26 PIN PLASTIC TSOP (300mil) *
24 Leads

* : under development

NEC Cord:S26G3-50-7JD



NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

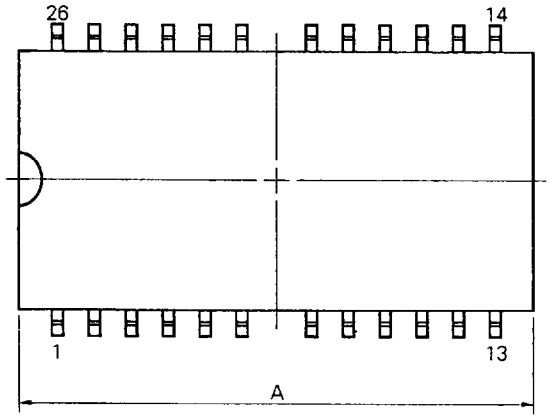
S26G3-50-7JD

ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.005}$
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	$0.8^{+0.2}_{-0.1}$	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

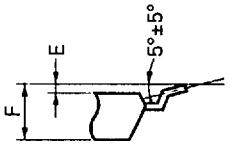
26 PIN PLASTIC TSOP (300mil) *
24 Leads Reverse bent

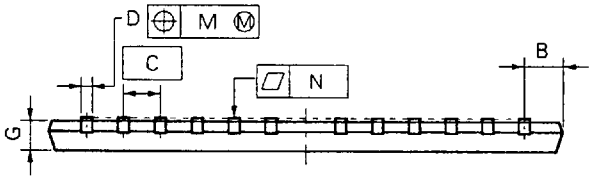
* : under development

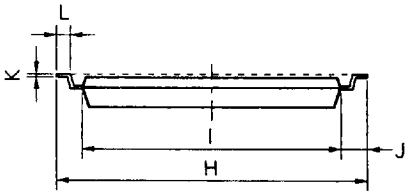
NEC Cord:S26G3-50-7KD



detail of lead end







S26G3-50-7KD

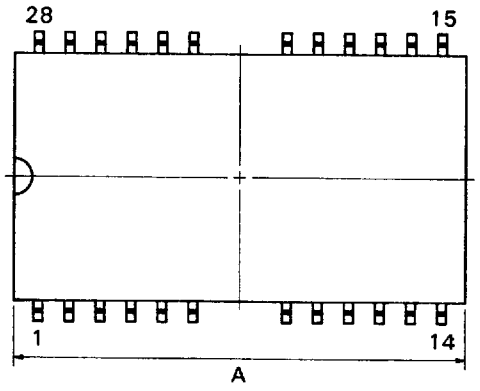
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition

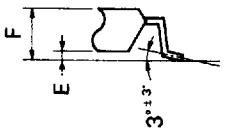
ITEM	MILLIMETERS	INCHES
A	17.40 MAX.	0.685 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T P)	0.050 (T.P.)
D	0 40±0.10	$0.016^{+0.004}_{-0.005}$
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0 044 MAX.
G	0 97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0 2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0 5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0 10	0 004

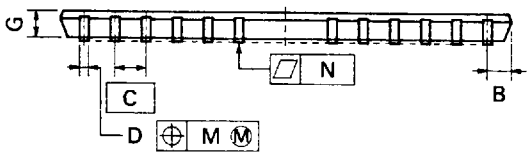
28 PIN PLASTIC TSOP (400mil)
24 Leads

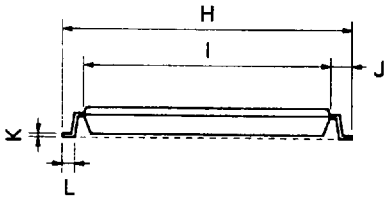
NEC Cord:S28G5-50-7JD1



detail of lead end







NOTE

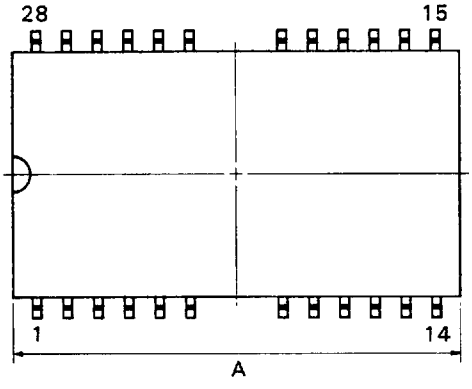
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD1

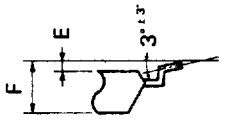
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
E	$0.05^{\pm 0.05}$	$0.002^{\pm 0.002}$
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	$11.76^{\pm 0.2}$	$0.463^{\pm 0.008}$
I	$10.16^{\pm 0.1}$	$0.400^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.008}_{-0.009}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

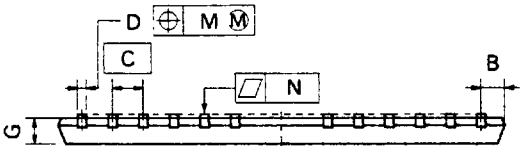
28 PIN PLASTIC TSOP (400mil)
24 Leads Reverse bent

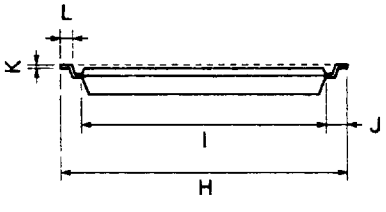
NEC Cord:S28G5-50-7KD1



detail of lead end







S28G5-50-7KD1

NOTE

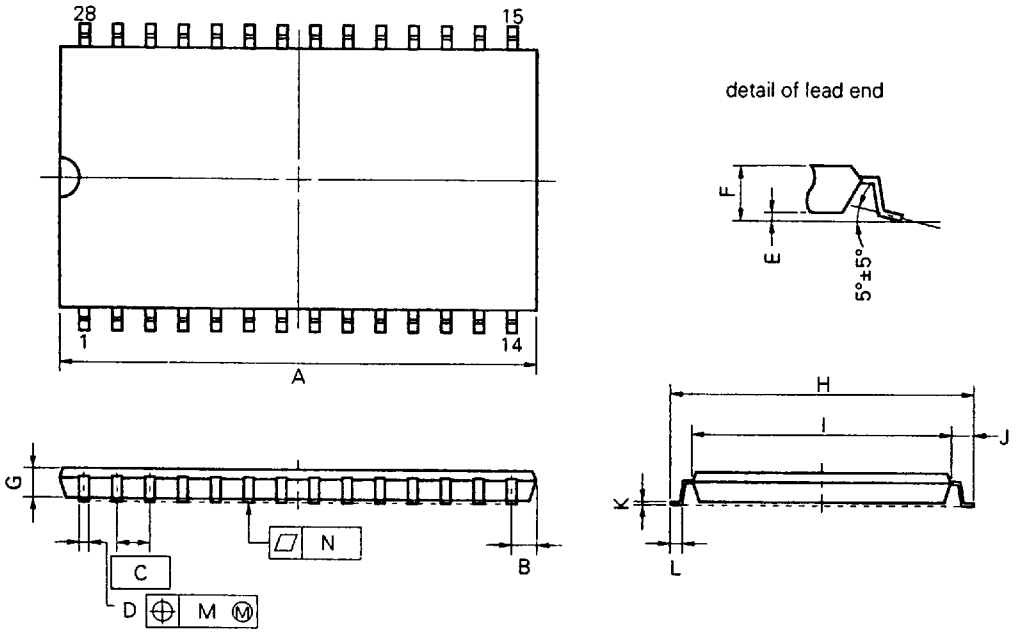
Each lead centerline is located within 0 21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{\pm 0\ 10}$	$0.016^{-0\ 004}_{-0\ 005}$
E	$0\ 05^{\pm 0\ 05}$	$0.002^{\pm 0\ 002}$
F	1 1 MAX.	0 044 MAX.
G	0 97	0.038
H	$11\ 76^{\pm 0\ 2}$	$0.463^{\pm 0\ 008}$
I	$10.16^{\pm 0\ 1}$	$0.400^{\pm 0\ 004}$
J	$0.8^{\pm 0\ 2}$	$0.031^{-0\ 009}_{-0\ 008}$
K	$0.125^{+0\ 10}_{-0\ 05}$	$0.005^{-0\ 004}_{-0\ 002}$
L	$0\ 5^{\pm 0\ 1}$	$0.020^{-0\ 004}_{-0\ 005}$
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP (400mil)

28 Leads

NEC Cord:S28G5-50-7JD2



S28G5-50-7JD2

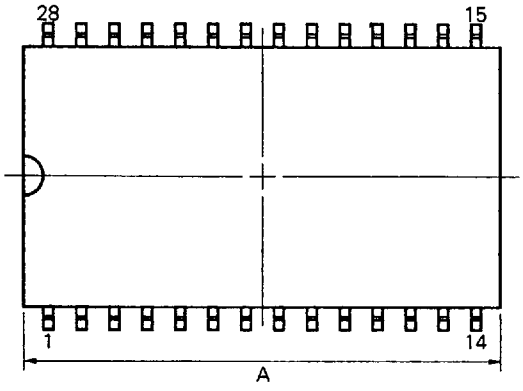
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T P.)	0.050 (T.P.)
D	0.40±0.10	$0.016^{+0\ 004}_{-0\ 005}$
E	0 05±0.05	0.002±0.002
F	1.1 MAX.	0 044 MAX.
G	0.97	0.038
H	11.76±0.2	0 463±0.008
I	10 16±0.1	0 400±0 004
J	0.8±0 2	$0.031^{+0\ 009}_{-0\ 008}$
K	$0.125^{+0\ 10}_{-0\ 05}$	$0\ 005^{+0\ 004}_{-0\ 002}$
L	0.5±0 15	$0.020^{+0\ 006}_{-0\ 007}$
M	0.21	0.009
N	0.10	0.004

NOTE

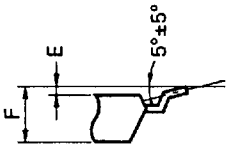
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

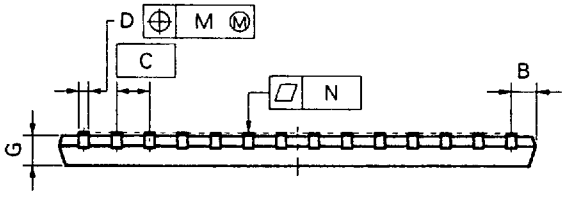
28 PIN PLASTIC TSOP (400mil)
28 Leads Reverse bent

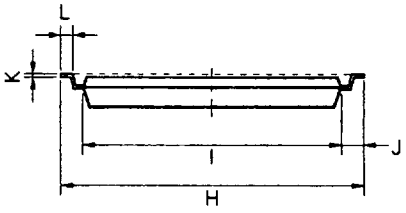
NEC Cord:S28G5-50-7KD2



detail of lead end







S28G5-50-7KD2

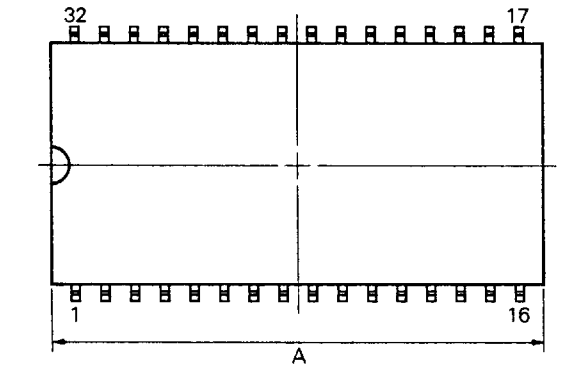
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0 40±0.10	$0.016^{+0\ 004}_{-0\ 005}$
E	0 05±0.05	0.002±0 002
F	1 1 MAX.	0.044 MAX.
G	0.97	0.038
H	11 76±0 2	0.463±0.008
I	10.16±0.1	0.400±0 004
J	0 8±0 2	$0\ 031^{+0\ 009}_{-0\ 008}$
K	$0.125^{+0\ 10}_{-0\ 05}$	$0.005^{+0\ 004}_{-0\ 002}$
L	0 5±0 15	$0\ 020^{+0\ 006}_{-0\ 007}$
M	0.21	0 009
N	0 10	0.004

NOTE

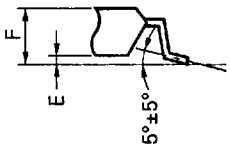
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

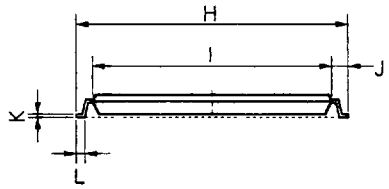
32 PIN PLASTIC TSOP (400mil)

NEC Cord:S32G5-50-7JD1



detail of lead end





S32G5-50-7JD1

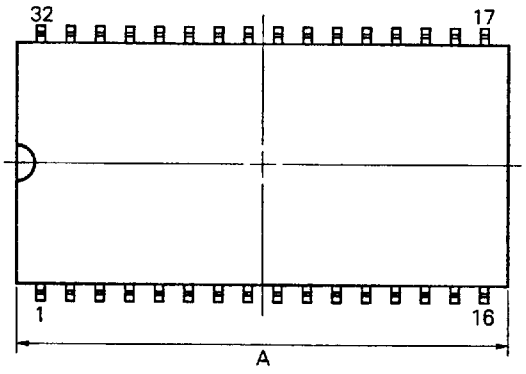
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

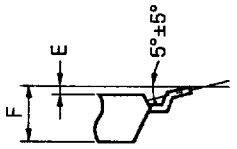
ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.15	$0.020^{+0.006}_{-0.007}$
M	0.21	0.009
N	0.10	0.004

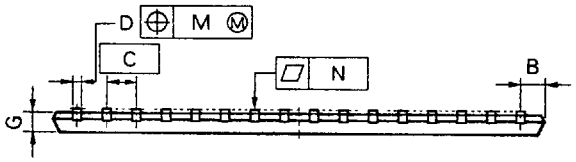
32 PIN PLASTIC TSOP (400mil)
Reverse bent

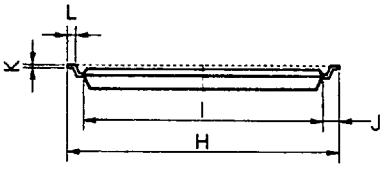
NEC Cord:S32G5-50-7KD1



detail of lead end







NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

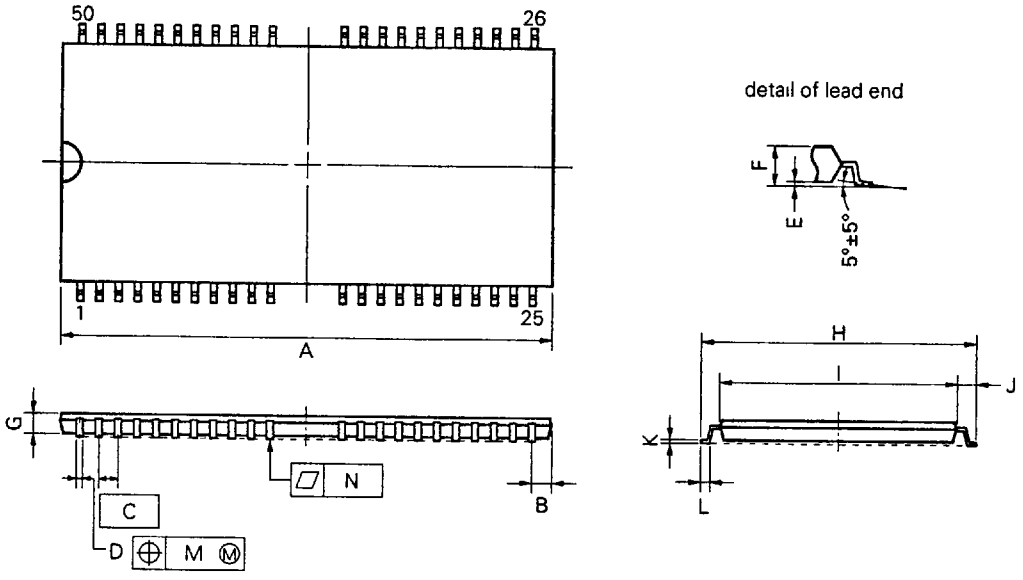
S32G5-50-7KD1

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.15	$0.020^{+0.006}_{-0.007}$
M	0.21	0.009
N	0.10	0.004

50 PIN PLASTIC TSOP (400mil)

44 Leads

NEC Cord:S50G5-80-7JF



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

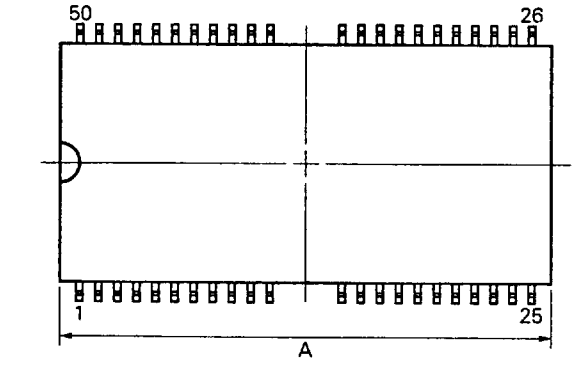
S50G5-80-7JF

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	$0.012^{+0.004}_{-0.005}$
E	0.05±0 05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0 97	0.038
H	11.76±0 2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.15	$0.020^{+0.006}_{-0.007}$
M	0.13	0.005
N	0.10	0.004

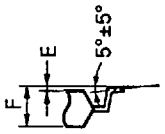
50 PIN PLASTIC TSOP (400mil)

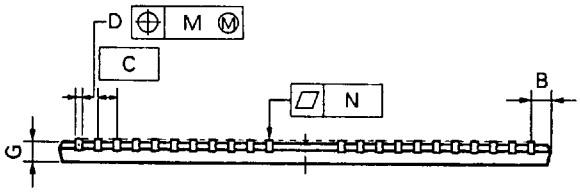
44 Leads Reverse bent

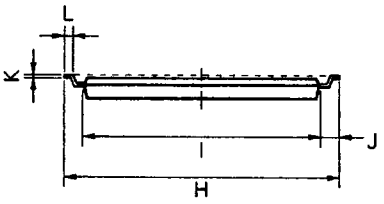
NEC Cord:S50G5-80-7KF



detail of lead end







NOTE

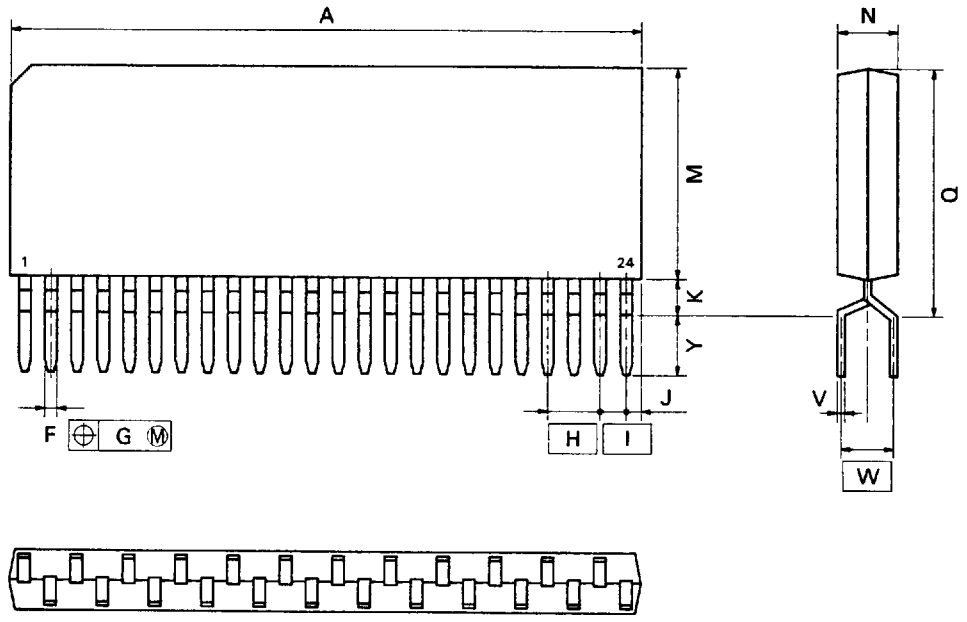
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7KF

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30 ± 0.10	$0.012^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.15	$0.020^{+0.006}_{-0.007}$
M	0.13	0.005
N	0.10	0.004

24 PIN PLASTIC ZIP (475mil)

NEC Cord:P24V-100-475A



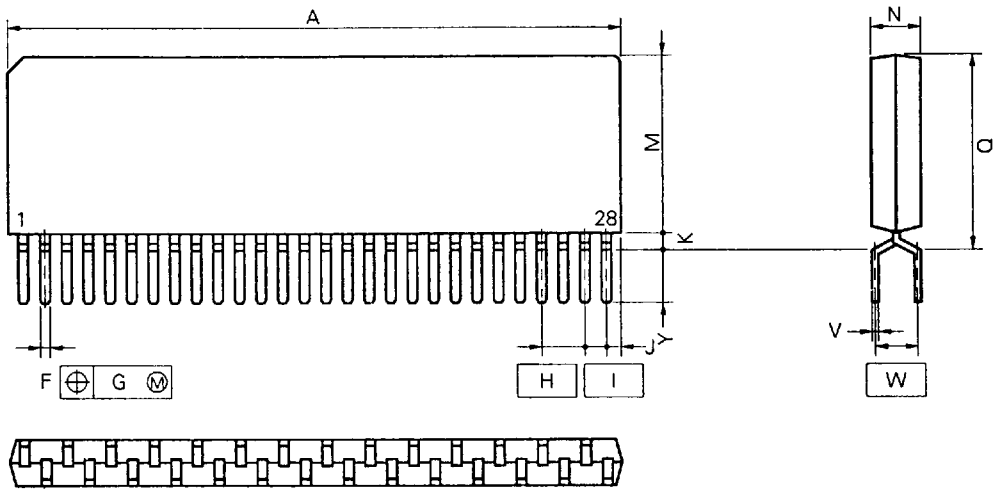
NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P24V-100-475A

ITEM	MILLIMETERS	INCHES
A	31.75 MAX.	1.250 MAX.
F	$0.50^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
G	ϕ0 25	ϕ0.010
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1 0 MIN	0.039 MIN.
M	10 8 MAX	0 426 MAX
N	$2\ 8^{\pm 0.2}$	$0.110^{+0.009}_{-0.008}$
Q	12.07 MAX.	0.476 MAX
V	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
W	2.54	0.100
Y	$3.3^{+0.5}$	$0.130^{\pm 0.02}$

28 PIN PLASTIC ZIP (475mil)

NEC Cord:P28VF-100-475A



NOTE

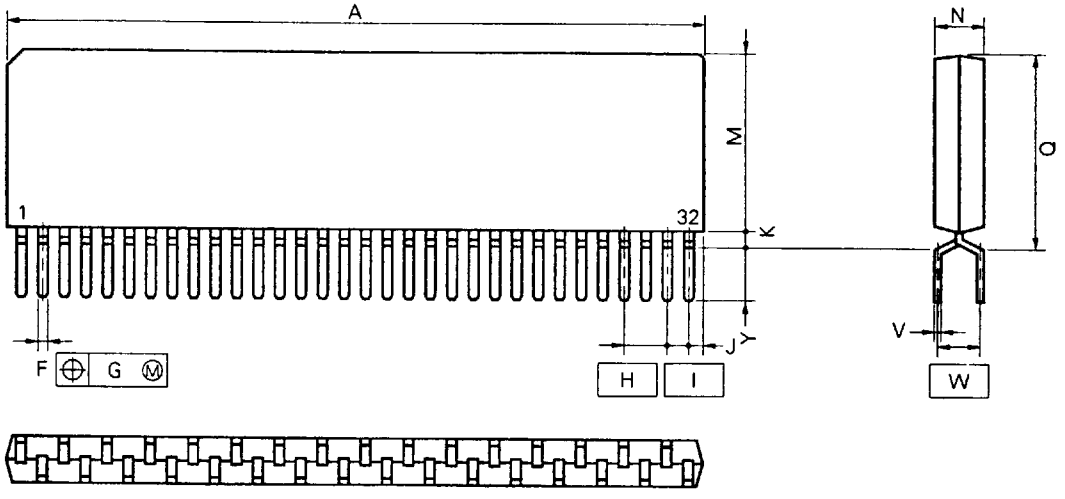
Each lead centerline is located within 0 25 mm (0.010 inch) of its true position (T.P) at maximum material condition.

P28VF-100-475A

ITEM	MILLIMETERS	INCHES
A	36.83 MAX.	1 450 MAX.
F	0 5±0 10	$0.020^{+0\ 004}_{-0\ 005}$
G	0.25	0.010
H	2 54 (T.P.)	0.100 (T P)
I	1 27 (T P.)	0.050 (T P.)
J	1 27 MAX.	0 050 MAX
K	0 9 MIN	0.035 MIN.
M	10 8 MAX.	0 426 MAX
N	2 8±0 2	$0.110^{+0\ 009}_{-0\ 008}$
Q	12 07 MAX	0 475 MAX.
V	$0\ 25^{+0\ 10}_{-0\ 05}$	$0.010^{+0\ 004}_{-0\ 003}$
W	2 54 (T.P.)	0.100 (T.P)
Y	3 25±0.2	0.128±0 008

32 PIN PLASTIC ZIP (475mil)

NEC Cord:P32VF-100-475A



NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P32VF-100-475A

ITEM	MILLIMETERS	INCHES
A	41.91 MAX.	1.650 MAX
F	0.5±0.10	$0.020^{+0.004}_{-0.005}$
G	0.25	0.010
H	2.54 (T.P.)	0.100 (T.P.)
I	1 27 (T.P)	0.050 (T.P.)
J	1.27 MAX.	0.050 MAX.
K	0 9 MIN.	0.035 MIN.
M	10.8 MAX.	0.426 MAX.
N	2 8±0.2	$0.110^{+0.009}_{-0.008}$
Q	12.07 MAX.	0.475 MAX.
V	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
W	2.54 (T.P.)	0 100 (T P.)
Y	3.25±0.2	0.128±0.008