System-on-Chip

Product Letter

System-on-Chip Lite

Gate Array with ARM7TDMI® subsystem

Description

System-on-Chip Lite (SoCLite) is NEC's new approach to low- to mid-volume system-on-chip projects. SoCLite is based on standard ASIC technology and consists of two blocks: an ARM7TDMI® based subsystem and a sea-of-gates area. The ARM® subsystem is fully designed and verified as a supermacro. It frees the user from the task of developing a complete RISC computer system. The sea-of-gates area allows the user to implement custom logic or special peripheral functions.

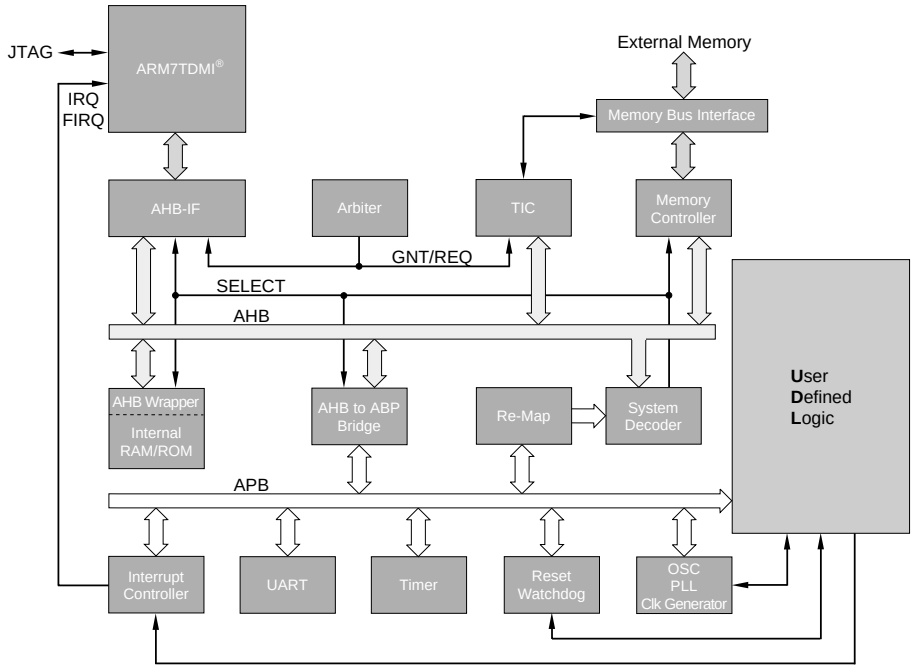
Applications

SoCLite is designed for embedded control applications. To maintain flexibility, SoCLite is not realized as an ASSP (application-specific standard product); this means that it can be used for a wide range of different applications. Once the customer functions are implemented into the sea-of-gates, it becomes a custom SoC. The SoCLite concept is especially interesting for the industrial and telecommunication market. Target applications are factory automation, industrial bus systems, card readers, business phones, terminals and home communication. Because of its low unit cost, low NRE cost and short prototyping turnaround times, SoCLite is also an ideal solution for emerging applications with uncertain market acceptance.

Features

- ARM7TDMI® core
- 32-bit ARM® and 16-bit Thumb® instruction set
- 32-bit x 8-bit Multiplier
- RAM: 8 Kbytes
- Bootstrap ROM: 2 Kbytes
- Memory controller supporting: Flash, SRAM and ROM
- Programmable interrupt controller: 32 interrupts, 8 priority levels
- Peripherals: UART, timer, reset, watchdog, PLL, oscillator
- JTAG test and debug interface
- Sea-of-gates: up to 190K raw gates available for User Defined Logic
- APB interconnection to the UDL
- Operating frequency: 35 MHz
- Operating voltage: 3.3 V ± 0.3 V
- Temperature range: -40 to +85°C
- 256-pin PBGA package

Block Diagram



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Functional Block Description

CPU

The SoCLite CPU is the popular ARM7TDMI®, an ARM7™ 32-bit RISC processor core with the Thumb®extension, on-chip debugging and 32 x 8 multiplier. Thumb®offers 32-bit RISC performance at 16-bit system cost through “compression” of the original ARM®instruction set, resulting in excellent code density and thus saving memory space. The Thumb® instructions are “decompressed” on the fly into full 32-bit ARM®instructions. It is also possible to select between ARM®and Thumb®modes during instruction execution.

Bus System

The ARM7TDMI®subsystem includes a fully AMBA™ compliant bus system structure. Two main buses – AHB and APB – connect the different macros. The AHB is a high-speed multimaster bus for connection to high-speed macros like CPU and memory controller. The APB is a lower speed bus for peripherals like UART, timer, etc. Both buses are 32 bits wide. The APB and any additional signals required for interrupts and reset are made available to the UDL.

Clock Generation

SoCLite clock generation has three parts: an oscillator, a programmable PLL and a programmable clock divisor. The recommended operating frequency is selectable between 15 and 35 MHz.

Memory

The memory subsystem features an internal 8-Kbyte RAM and a small 2-Kbyte ROM. The ROM contains a bootstrap loader program, selectable via an external pin, for device start-up.

Memory Controller

The SoCLite memory controller supports static memory-mapped devices including SRAM, ROM, Flash and burst ROM. The address range per chip select is 64 Mbytes with a 32-bit external memory data path.

Interrupt Controller

The interrupt controller supports up to 32 interrupts: 29 interrupts from the UDL and 3 from the ARM®subsystem. All interrupts are priority controlled, individually or globally maskable and selectable by triggering the IRQ of the ARM®core.

Peripherals

The subsystem contains a simple UART and a timer consisting of a 32-bit down counter with load registers. A configurable prescaler generates the timer clock frequency. A second timer is used as a watchdog timer, generating a reset on overflow.

UDL

The sea-of-gates area for the User Defined Logic has a size of 190K raw gates. The UDL area is connected via the APB bus with the ARM®subsystem. The UDL is for user-developed functions. These can be additional peripheral blocks or hardwired logic functions for reducing the CPU load. The custom logic is implemented into the SoCLite chip using the NEC Gate Array design flow. In addition NEC supports FPGA conversion services for customers not familiar with standard ASIC design flow. For further information refer to the product letters “SoCLite Development Board” and “SoCLite Design Flow”.

Ordering Information

Devices

Part Number	Package	Brand Name
µPD65977S1-xxx-B6	256-pin PBGA	System-on-Chip Lite

Note: Three digits (xxx) are used for the customer suffix number

Documentation

Doc Number	Topic	Type
A15046EE2V0PL00	Development Board	Product Letter
A15047EE1V0PL00	Design Flow	Product Letter
To be defined	Development Board	User's Manual
To be defined	System-on-Chip Lite	Data Sheet
To be defined	Design Flow	Design Manual

Tools

Order Number	Vendor	Description
EB-SoCLite-XI-2000E-6	NEC	Development Board (feat. Xilinx®FPGA)
EB-SoCLite-AI-1000E-2x	NEC	Development Board (feat. Altera®FPGA)
See www.arm.com	ARM Ltd.*	ARM Developer Suite (ADS) v1.1 and Debugging Tools
See www.lauterbach.de	Lauterbach*	In-Circuit Debugger/In-Circuit Emulator
See www.agilent.com	Agilent*	Debug System

* Contact vendor directly

For further information on NEC products visit our European website at **www.nec.de**

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With compliments