1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16-bit fixed-point DSP microcomputer.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	ADSP-2101TG/883B-40
−2	ADSP-2101TG/883B-50

NOTE
[1]See Paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
G	G-68A	68-Lead Pin Grid Array

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage ..... −0.3 V to +7 V
Input Voltage ..... −0.3 V to V_{DD} +0.3 V
Output Voltage Swing ..... −0.3 V to V_{DD} +0.3 V
Operating Temperature Range (Ambient) ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (10 sec) PGA ..... +300°C
Lead Temperature (5 sec) PLCC and PQFP ..... +280°C

1.5 Thermal Characteristics.

Ambient Temperature Rating:
$T_{AMB} = T_{case} - (PD \times \theta_{CA})$
T_{CASE} = Case temperature in °C
PD = Power dissipation in W
θ_{CA} = Thermal resistance (case-to-ambient)
θ_{JA} = Thermal resistance (junction-to-ambient)
θ_{JC} = Thermal resistance (junction-to-case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	18°C/W	9°C/W	9°C/W

Table 1.

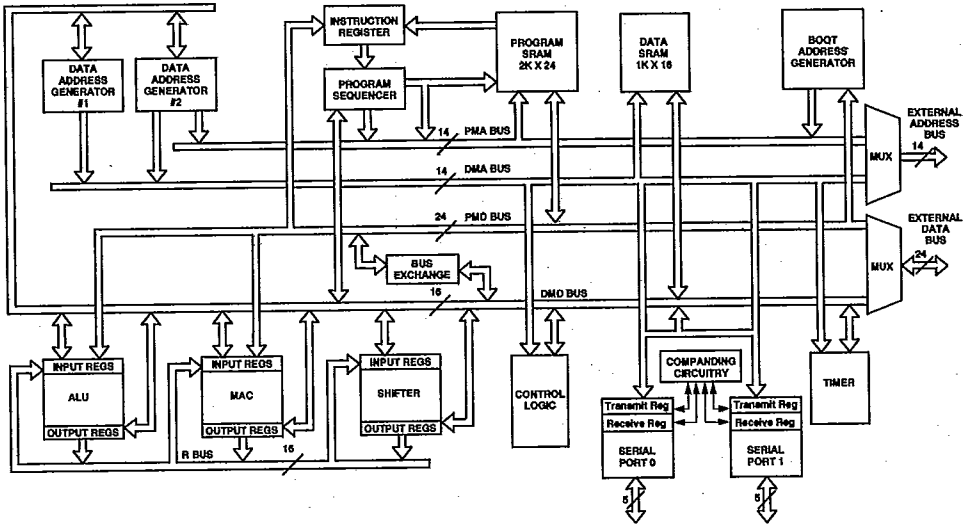
Test	Symbol	Device	Sub Group 1, 2, 3	Sub Group 4	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
ELECTRICAL CHARACTERISTICS								
Hi-Level Input Voltage[2, 3]	V_{IH}	−1, 2	2.0				@ V_{DD} = max	V min
Hi-Level CLKIN Voltage	V_{IH}	−1, 2	2.2				@ V_{DD} = max	V min
Lo-Level Input Voltage[1, 2]	V_{IL}	−1, 2	0.8				@ V_{DD} = min	V max
Hi-Level Output Voltage[2, 4, 5]	V_{OH}	−1, 2	2.4				@ V_{DD} = min, I_{OH} = −0.5 mA	V min
			V_{DD}−0.3				@ V_{DD} = min, I_{OH} = −100 μA[6]	
Lo-Level Output Voltage[2, 4, 5]	V_{OL}	−1, 2	0.4				@ V_{DD} = min, I_{OL} = 2 mA	V max
Hi-Level Input Current[1]	I_{IH}	−1, 2	10				@ V_{DD} = max, V_{IN} = V_{DD} max	μA max
Lo-Level Input Current[1]	I_L	−1, 2	10				@ V_{DD} = max, V_{IN} = 0 V	μA max
Tristate Leakage Current[1]	I_{OZL}	−1, 2	10				@ V_{DD} = max, V_{IN} = V_{DD} max[7]	μA max
Supply Current (Idle)[8, 9]	I_{DD}	−1, 2	14				@ V_{DD} = max	mA max
Supply Current (Dynamic)[9]	I_{DD}	−1, 2	81				@ V_{DD} = max, t_{CK} = 60 ns[10]	mA max
			64				@ V_{DD} = max, t_{CK} = 80 ns[10]	mA max
			55				@ V_{DD} = max, t_{CK} = 97.6 ns[10]	mA max
Input Pin Capacitance[1, 6, 11]	C_I	−1, 2		8			@ V_{IN} = +2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = +25°C	pF max
Output Pin Capacitance[6, 11, 12, 13]	C_O	−1, 2		8			@ V_{IN} = +2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = +25°C	pF max
CLOCK SIGNALS								
Timing Requirements								
CLKIN Period (ADSP-2101-40)	t_{CK}[14]	−1, 2			97.6	97.6		ns min
					200	200		ns max
CLKIN Period (ADSP-2101-50)	t_{CK}[14]	−1, 2			80	80		ns min
					200	200		ns max
CLKIN Period (ADSP-2101-66)	t_{CK}[14]	−1, 2			60	60		ns min
					200	200		ns max
CLKIN Width Low	t_{CKL}	−1, 2			20	20		ns min
CLKIN Width High	t_{CKH}	−1, 2			20	20		ns min
Switching Characteristic								
CLKOUT Width Low	t_{CPL}	−1, 2			$0.5t_{CK}$−10			ns min
CLKOUT Width High	t_{CPH}	−1, 2			$0.5t_{CK}$−10			ns min
CLKIN High to CLKOUT High	t_{CKOH}	−1, 2			0	0		ns min
					20	20		ns max
Timing Requirements								
$\overline{\text{RESET}}$ Width Low	t_{RSP}	−1, 2			$5t_{CK}$[15]	$5t_{CK}$[15]		ns min
INTERRUPTS AND FLAGS								
Timing Requirements								
IRZx or FI Setup before CLKOUT Low[16, 17]	t_{IFS}	−1, 2			$0.25t_{CK}$+15			ns min
IRQx or FI Hold after CLKOUT High[16, 17]	t_{IFH}	−1, 2			$0.25t_{CK}$			ns min
IRQx = $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$								
Switching Characteristics								
FO Hold after CLKOUT High	t_{FOH}	−1, 2			−5	−5		ns min
FO Delay from CLKOUT High	t_{FOD}	−1, 2			15	15		ns max

Test	Symbol	Device	Sub Group 1, 2, 3	Sub Group 4	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
BUS REQUEST/GRANT								
Timing Requirements								
$\overline{BR}$ Hold after CLKOUT High[18]	t_{BH}	−1, 2			$0.25t_{CK}+5$	$25t_{CK}+15$		ns min
$\overline{BR}$ Setup before CLKOUT Low[18]	t_{BS}	−1, 2			$0.25t_{CK}+20$	$25t_{CK}+20$		ns min
Switching Characteristics								
CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable	t_{SD}	−1, 2			$0.25t_{CK}+20$	$25t_{CK}+20$		ns max
$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$, Disable to $\overline{BG}$ Low	t_{SDB}	−1, 2			0	0		ns min
$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	t_{SE}	−1, 2			0	0		ns min
$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	t_{SEC}	−1, 2			$0.25t_{CK}-10$	$0.25t_{CK}-10$		ns min
MEMORY READ [w = Wait States × (t_{CK})]								
Timing Requirements								
$\overline{RD}$ Low to Data Valid	t_{RDD}	−1, 2			$0.5_{CK}-15+w$			ns max
A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid	t_{AA}	−1, 2			$0.75t_{CK}-20+w$[19]			ns max
Data Hold from RD High	t_{RDH}	−1, 2			0	0		ns min
Switching Characteristics								
$\overline{RD}$ Pulse Width	t_{RP}	−1, 2			$0.5t_{CK}-5+w$			ns min
CLKOUT High to $\overline{RD}$ Low	t_{CRD}	−1, 2			$0.25t_{CK}-5+w$			ns min
					$0.25t_{CK}+10$			ns max
A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	t_{ASR}	−1, 2			$0.25t_{CK}-12$			ns min
A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	t_{RDA}	−1, 2			$0.25t_{CK}-10$			ns min
$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	t_{RWR}	−1, 2			$0.5t_{CK}-5$			ns min
Data Setup before $\overline{WR}$ High	t_{DW}	−1, 2			$0.5t_{CK}-10+w$			ns min
Data Hold after $\overline{WR}$ High	t_{DH}	−1, 2			$0.25t_{CK}-10$			ns min
$\overline{WR}$ Low to Data Enabled	t_{WDE}	−1, 2			0	0		ns min
A0–A13, $\overline{DMS}$, $\overline{PMW}$ Hold after $\overline{WR}$ Low	t_{ASW}	−1, 2			$0.25t_{CK}-12$			ns min
Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	t_{DDR}	−1, 2			$0.25t_{CK}-10$			ns min
CLKOUT High to $\overline{WR}$ Low	t_{CWR}	−1, 2			$0.25t_{CK}-5$			ns min
					$0.25t_{CK}+10$			ns max
A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted	t_{AW}	−1, 2			$0.75t_{CK}-15+w$			ns min
A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	t_{WRA}	−1, 2			$0.25t_{CK}-10$			ns min
$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	t_{WWR}	−1, 2			$0.5t_{CK}-5$			ns min
SERIAL PORTS								
Timing Requirement								
SCLK Period	t_{SCK}	−1			97.6	97.6		ns min
		−2			80	80		ns min
DR/TFS/RFS Setup before SCLK Low	t_{SCS}	−1			10	10		ns min
		−2			8	8		ns min
DR/TFS/RFS Hold after SCLK Low	t_{SCH}	−1			10	10		ns min
		−2			10	10		ns min
$SCLK_{IN}$ Width	t_{SCP}	−1			38	38		ns min
		−2			30	30		ns min

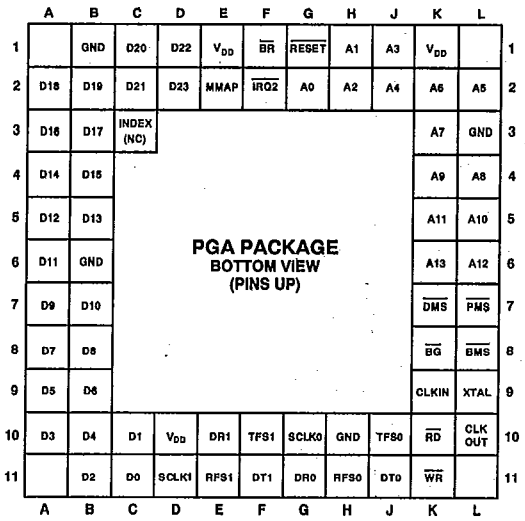
Test	Symbol	Device	Sub Group 1, 2, 3	Sub Group 4	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Switching Characteristics								
CLKOUT High to $SCLK_{OUT}$	t_{CC}	−1			$0.25t_{CK}$	$0.25t_{CK}$		ns min
					$0.25t_{CK}+15$	$0.25t_{CK}+15$		ns max
		−2			$0.25t_{CK}$	$0.25t_{CK}$		ns min
					$0.25t_{CK}+15$	$0.25t_{CK}+15$		ns max
SCLK High to DT Enable	t_{SCDE}	−1, 2			0	0		ns min
SCLK High to DT Valid	t_{SCDV}	−1			25	25		ns max
		−2			20	20		ns max
TFS/RFS_{OUT} Hold after SCLK High	t_{RH}	−1			0	0		ns min
		−2			0	0		ns min
TFS/RFS_{OUT} Delay from SCLK High	t_{RD}	−1			25	25		ns max
		−2			20	20		ns max
DT Hold after SCLK High	t_{SCDK}	−1			0	0		ns min
		−2			0	0		ns min
TFS_{IN} (alt) to DT Enable	t_{TDE}	−1			0	0		ns min
		−2			0	0		ns min
TFS_{IN} (alt) to DT Valid	t_{TDV}	−1			20	20		ns max
		−2			18	18		ns max
SCLK High to DT Disable	t_{SCDD}	−1			30	30		ns max
		−2			25	25		ns max
RFS_{IN} (Multichannel, Frame Delay Zero) to DT Valid	t_{RDV}	−1			25	25		ns max
		−2			20	20		ns max

NOTES
[1]Input only pins: CLKIN, $\overline{RESET}$, $\overline{IRQ2}$, $\overline{BR}$, MMAP, DR0, DR1.
[2]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1.
[3]$\overline{RESET}$, $\overline{IRQ2}$, $\overline{BR}$, MMAP, DR1, DR0 input pins.
[4]Output pins: $\overline{BG}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$, A0–A13, DT0, DT1, SCLK0, TFS0, TFS1, RFS0, RFS1.
[5]Although specified for TTL outputs, all ADSP-2101 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[6]Guaranteed but not tested.
[7]0 V on $\overline{BR}$, CLKIN active (to force tristate condition).
[8]Idle refers to ADSP-2101 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[9]Current reflects device operating with no output loads.
[10]V_{IN} = 0.4 V and 2.4 V.
[11]Applies to PGA, PLCC, and PQFP package types.
[12]Tristatable pins: A0–A13, D0–D23, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$, DT0, DT1, SLCK0, SLCK1, TFS0, TFS1, RFS0, RFS1.
[13]Output pin capacitance is the capacitive load for any tristated output pin.
[14]t_{CK} values within the range of CLKIN period should be substituted for all relevant timing paramters to obtain specification value. Example: $t_{CPH} + 0.5t_{CK} - 10$ ns = 0.5(60)−10 ns = 20 ns.
[15]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 1000 processor cycles assuming stable CLKIN (not in start-up time).
[16]If IRQx and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the user's manual for further information on interrupt.)
[17]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[18]$\overline{BR}$ is a synchronous signal which must meet setup/hold time requirements. Refer to the user's manual for $\overline{BR}/\overline{BG}$ cycle relationships.
[19]t_{AA} (max) = 0.75 t_{CK} − 25 + w for ADSP-2101BG-66, ADSP-2101BP-66, ADSP-2101BS-66.

3.2.1 Functional Block Diagram and Terminal Assignments.



PIN CONFIGURATIONS

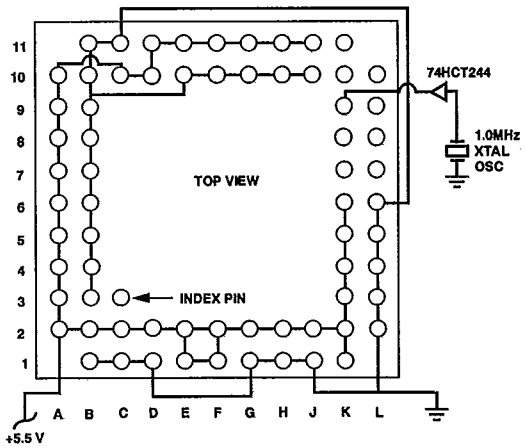


3.2.4 Microcircuit Technology Group

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



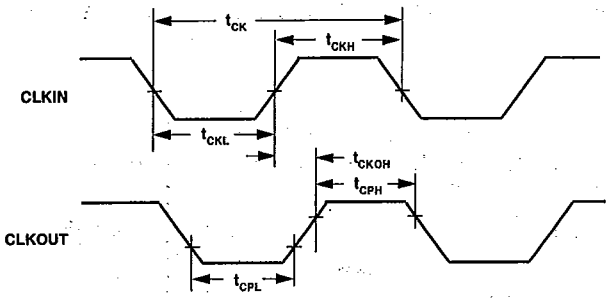


Figure 1. Clock Signals

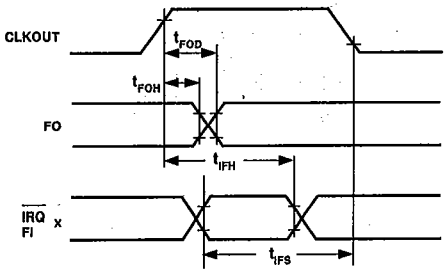


Figure 2. Interrupts and Flags

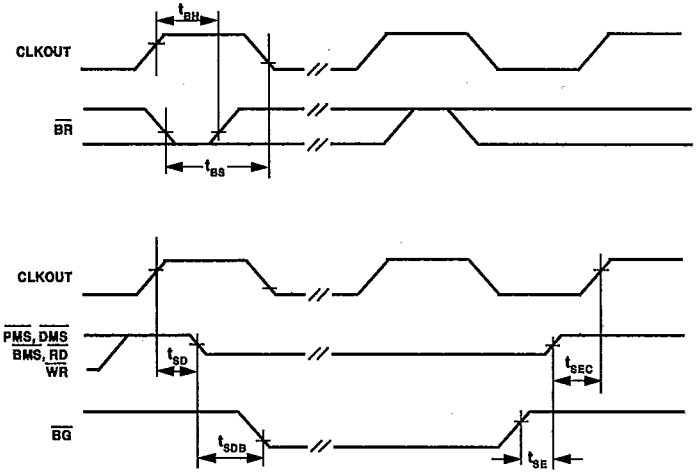


Figure 3. Bus Request–Bus Grant

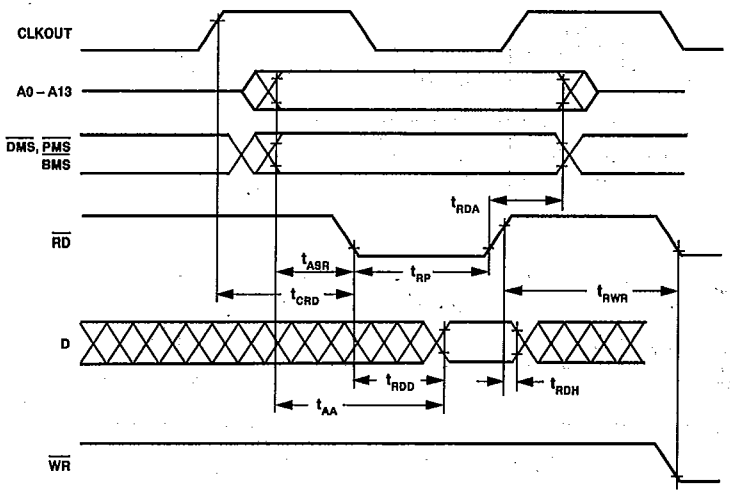


Figure 4. Memory Read

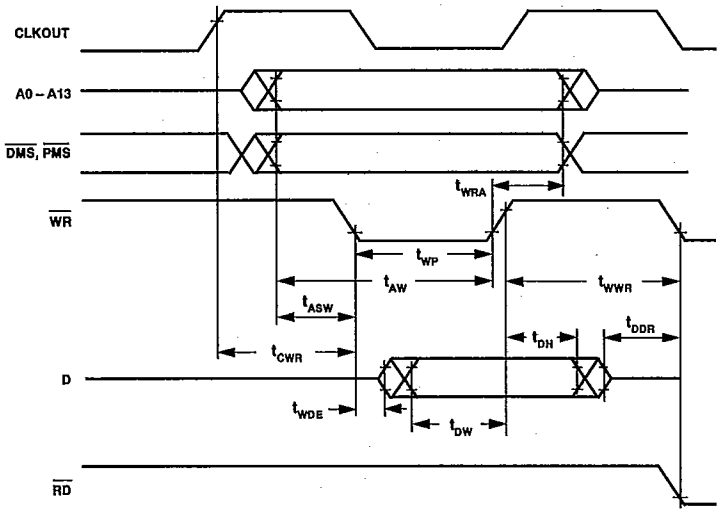


Figure 5. Memory Write

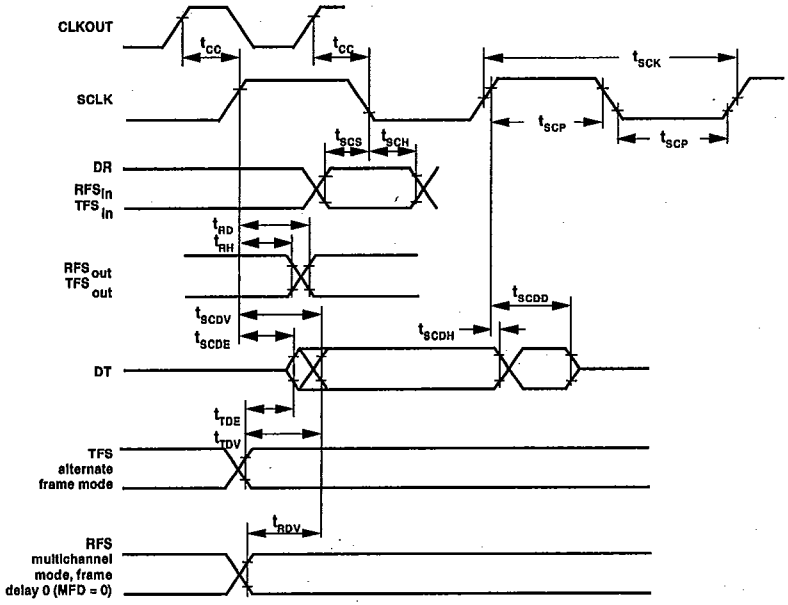


Figure 6. Serial Ports