Am81C451/458

CMOS Color Palette

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Plug-in Replacement for Bt451 (Bt458)
- Available in 80-, 110-, 125-, 165-MHz versions
- Typical Power Dissipation: 1.0 W
- Available in PGA and PLCC packages
- Multiplexed TTL Pixel Ports
- Triple 4-Bit (8-Bit) Digital-to-Analog Converters (DACs)
- 256 x 12(24) Dual-Port Color Palette RAM
- 4 x 12(24) Dual-Port Overlay RAM
- RS-343A-Compatible RGB Outputs
- Read and Blink Masks for each bit-plane
- Standard MPU Interface
- Single +5-V Power Supply
- Full military range specifications

GENERAL DESCRIPTION

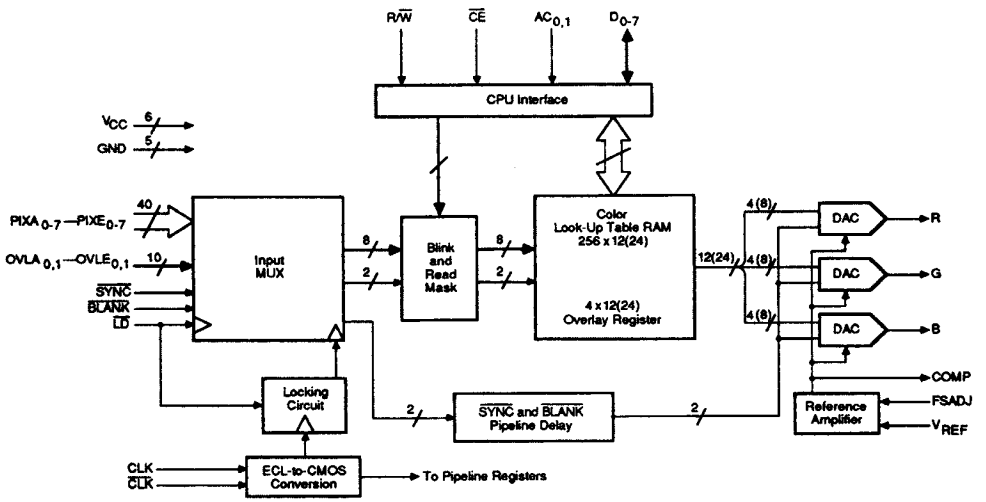
The Am81C451/458 CMOS Color Palette drives all three guns of a standard RS-343A color monitor. It is designed specifically for the high-resolution color graphics market for applications such as image processing, CAE/CAD/CAM, solid modeling, and animation. The Am81C451/458 operates at speeds sufficient to support monitor resolutions up to 1600 x 1280 pixels, and can simultaneously display 259 colors out of an available set of 4K colors for the Am81C451 and 16.8 million colors for the Am81C458.

The Am81C451/458 includes an input buffer, an input multiplexer, a 256 x 12(24) Look-Up Table, a 4 x 12(24) Overlay Table, and three 4-bit (8-bit) RS-343A-compatible DACs. It is available in versions with pixel rates as high as 165 MHz. It also contains programmable bit-plane Read and Blink Masks. Proprietary DAC decoding techniques minimize glitch energy and skew.

The Am81C451/458 minimizes the need for high-speed ECL signals on the PC board since there are only two inputs (CLK, $\overline{CLK}$) that need to operate at pixel rate. Multiple pixel ports and internal multiplexing enables TTL-compatible interfacing to the Display Memory while maintaining the high pixel data rates on-chip.

The Am81C451/458 is fabricated using AMD's state-of-the-art 1.2-micron CMOS process. The device is available in an 84-lead PGA package as well as a lower cost 84-pin PLCC package.

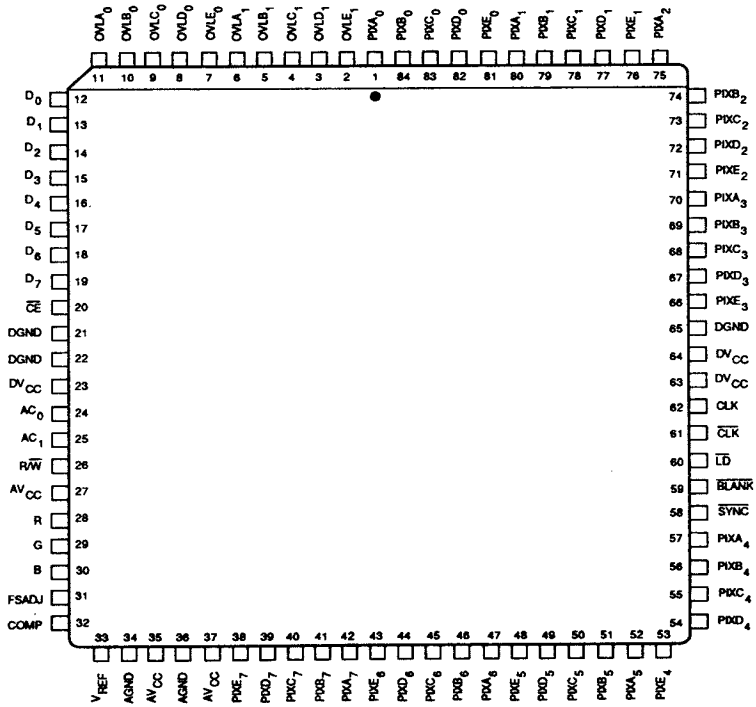
BLOCK DIAGRAM



Publication # 10451 Rev. B Amendment /0
Issue Date: October 1988

CONNECTION DIAGRAMS

PLCC
(Top View)



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CD011570

Note: Pin 1 is marked for orientation.

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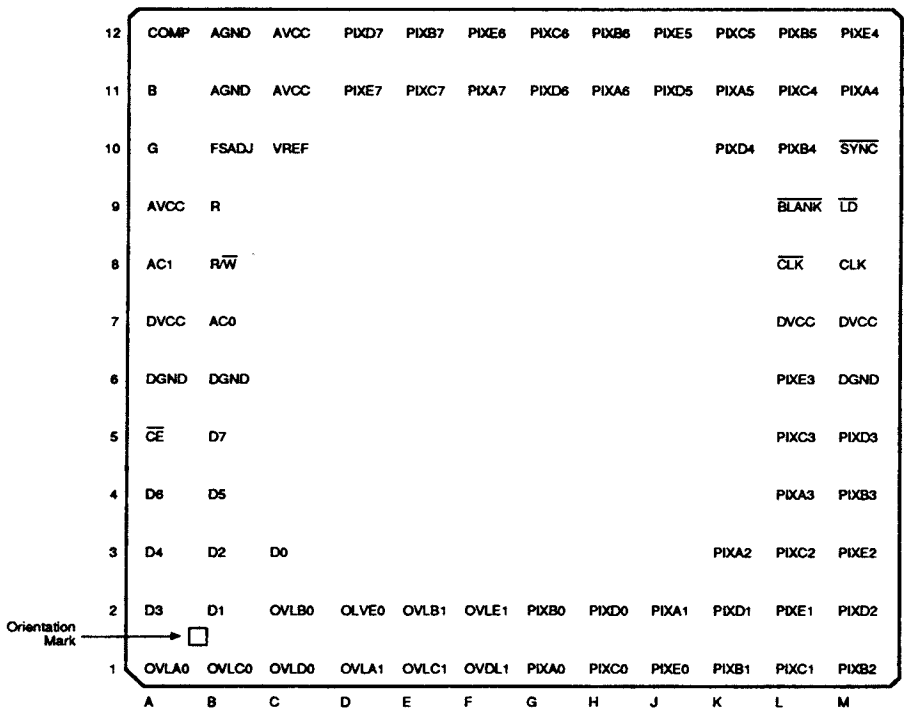
CONNECTION DIAGRAMS (Cont'd.)

PGA*
Top View
(Pins Facing Down)



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Please see PGA Pin Designations for pinout sorted by both Pin Names and Pin Numbers.

PGA PIN DESIGNATIONS

(Sorted by Pin Name)

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
B-7	AC_0	B-6	DGND	K-3	$PIXA_2$	E-11	$PIXC_7$
A-8	AC_1	M-6	DGND	L-4	$PIXA_3$	H-2	$PIXD_0$
B-12	AGND	A-6	DGND	M-11	$PIXA_4$	K-2	$PIXD_1$
B-11	AGND	L-7	DV_{CC}	K-11	$PIXA_5$	M-2	$PIXD_2$
C-12	AV_{CC}	A-7	DV_{CC}	H-11	$PIXA_6$	M-5	$PIXD_3$
C-11	AV_{CC}	M-7	DV_{CC}	F-11	$PIXA_7$	K-10	$PIXD_4$
A-9	AV_{CC}	B-10	FSADJ	G-2	$PIXB_0$	J-11	$PIXD_5$
A-11	B	A-10	G	K-1	$PIXB_1$	G-11	$PIXD_6$
L-9	$\overline{BLANK}$	M-9	$\overline{LD}$	M-1	$PIXB_2$	D-12	$PIXD_7$
A-5	$\overline{CE}$	A-1	$OVLA_0$	M-4	$PIXB_3$	J-1	$PIXE_0$
L-8	$\overline{CLK}$	D-1	$OVLA_1$	L-10	$PIXB_4$	L-2	$PIXE_1$
M-8	CLK	C-2	$OVLB_0$	L-12	$PIXB_5$	M-3	$PIXE_2$
A-12	COMP	E-2	$OVLB_1$	H-12	$PIXB_6$	L-6	$PIXE_3$
C-3	D_0	B-1	$OVLC_0$	E-1	$PIXB_7$	M-12	$PIXE_4$
B-2	D_1	E-1	$OVLC_1$	H-1	$PIXC_0$	J-12	$PIXE_5$
B-3	D_2	C-1	$OVLD_0$	L-1	$PIXC_1$	F-12	$PIXE_6$
A-2	D_3	F-1	$OVLD_1$	L-3	$PIXC_2$	D-11	$PIXE_7$
A-3	D_4	D-2	$OVLE_0$	L-5	$PIXC_3$	B-9	R
B-4	D_5	F-2	$OVLE_1$	L-11	$PIXC_4$	B-8	$R/\overline{W}$
A-4	D_6	G-1	$PIXA_0$	K-12	$PIXC_5$	M-10	$\overline{SYNC}$
B-5	D_7	J-2	$PIXA_1$	G-12	$PIXC_6$	C-10	V_{REF}

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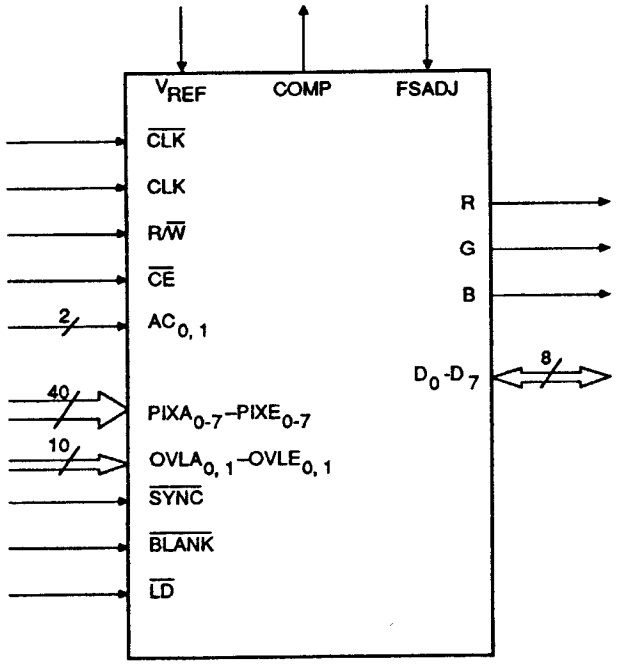
PGA PIN DESIGNATIONS (Cont'd.)

(Sorted by Pin Number)

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A-1	$OVLA_0$	B-10	FSADJ	G-1	$PIXA_0$	L-4	$PIXA_3$
A-2	D_3	B-11	AGND	G-2	$PIXB_0$	L-5	$PIXC_3$
A-3	D_4	B-12	AGND	G-11	$PIXD_6$	L-6	$PIXE_3$
A-4	D_6	C-1	$OVLD_0$	G-12	$PIXC_6$	L-7	DV_{CC}
A-5	$\overline{CE}$	C-2	$OVLB_0$	H-1	$PIXC_0$	L-8	$\overline{CLK}$
A-6	DGND	C-3	D_0	H-2	$PIXD_0$	L-9	$\overline{BLANK}$
A-7	DV_{CC}	C-10	V_{REF}	H-11	$PIXA_6$	L-10	$PIXB_4$
A-8	AC_1	C-11	AV_{CC}	H-12	$PIXB_6$	L-11	$PIXC_4$
A-9	AV_{CC}	C-12	AV_{CC}	J-1	$PIXE_0$	L-12	$PIXB_5$
A-10	G	D-1	$OVLA_1$	J-2	$PIXA_1$	M-1	$PIXB_2$
A-11	B	D-2	$OVLE_0$	J-11	$PIXD_5$	M-2	$PIXD_2$
A-12	COMP	D-11	$PIXE_7$	J-12	$PIXE_5$	M-3	$PIXE_2$
B-1	$OVLC_0$	D-12	$PIXD_7$	K-1	$PIXB_1$	M-4	$PIXB_3$
B-2	D_1	E-1	$OVLC_1$	K-2	$PIXD_1$	M-5	$PIXD_3$
B-3	D_2	E-2	$OVLB_1$	K-3	$PIXA_2$	M-6	DGND
B-4	D_5	E-11	$PIXC_7$	K-10	$PIXD_4$	M-7	DV_{CC}
B-5	D_7	E-12	$PIXB_7$	K-11	$PIXA_5$	M-8	CLK
B-6	DGND	F-1	$OVLD_1$	K-12	$PIXC_5$	M-9	$\overline{LD}$
B-7	AC_0	F-2	$OVLE_1$	L-1	$PIXC_1$	M-10	$\overline{SYNC}$
B-8	$R/\overline{W}$	F-11	$PIXA_7$	L-2	$PIXE_1$	M-11	$PIXA_4$
B-9	R	F-12	$PIXE_6$	L-3	$PIXC_2$	M-12	$PIXE_4$

LOGIC SYMBOL



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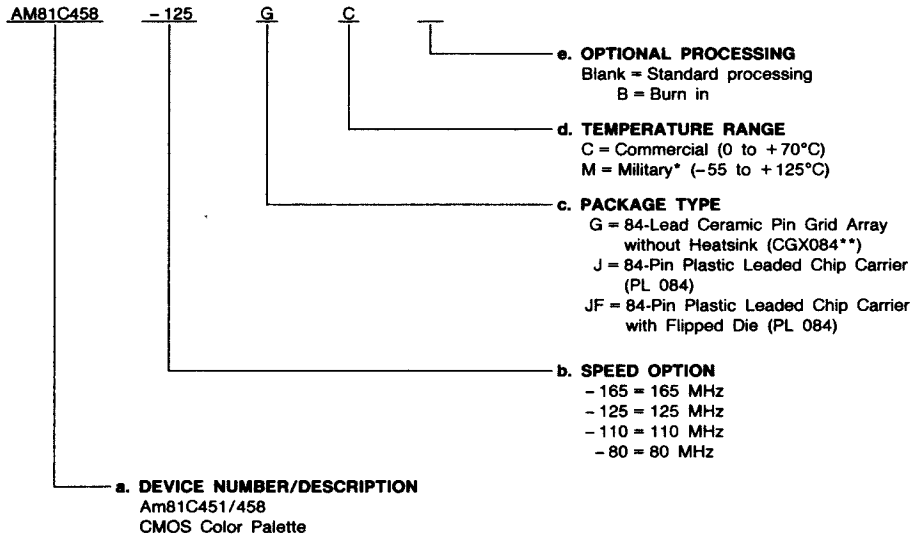
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM81C451-165	GC, JC, GM, GMB
AM81C451-125	
AM81C451-110	
AM81C451-80	
AM81C458-165	
AM81C458-125	
AM81C458-110	
AM81C458-80	

*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

**Preliminary; Package in development.

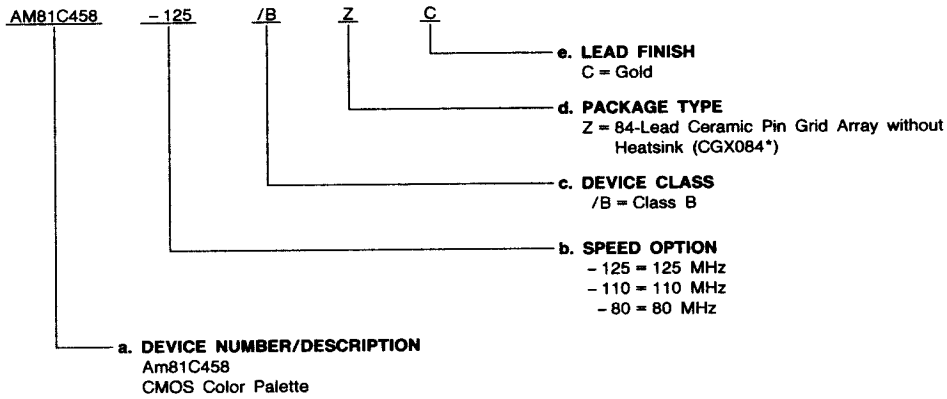
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defence applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM81C458-125	/BZC
AM81C458-110	
AM81C458-80	

*Preliminary; Package in development.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

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PIN DESCRIPTION

Timing Section

$\overline{BLANK}$ $\overline{Blank}$ (TTL-Compatible Input)
When active, the $\overline{BLANK}$ input overrides the color pixel and overlay data to force the Red, Green, and Blue video outputs to their blank levels. This blank level is required during the monitor's vertical and horizontal retrace times. It is latched on the rising edge of $\overline{LD}$.

CLK, $\overline{CLK}$ Clock Source Pins (Pseudo-ECL-Compatible Inputs)
These differential clock inputs operate at the pixel clock rate of the system. They are driven by ECL logic configured for single (+5 V) supply operation.

$\overline{LD}$ $\overline{Load\ Clock}$ (TTL-Compatible Input)
Data present on the $PIXA_{0-7}$ through $PIXE_{0-7}$ and $OVLA_{0,1}$ through $OVLE_{0,1}$, $\overline{SYNC}$, and $\overline{BLANK}$ inputs are clocked into the part on the rising edge of $\overline{LD}$. The input rate for this pin may be either one-fourth or one-fifth of the clock frequency, depending on how the part is programmed. See Display Memory Interface section under Functional Description.

$\overline{SYNC}$ $\overline{Sync}$ (TTL-Compatible Input)
When active, the $\overline{SYNC}$ input switches off a current source on the Green video output. It is latched on the rising edge of $\overline{LD}$. Because $\overline{SYNC}$ does not override any other inputs or control pins, it should be asserted only during blanking intervals.

Data Path Section

$OVLA_{0,1}$ through $OVLE_{0,1}$ Color Overlay Data Address (TTL-Compatible Inputs)
These ten inputs are organized as five 2-bit addresses. Each 2-bit address selects which of the four Overlay Registers is used to provide color information. These ten inputs are latched into the input buffer on the rising edge of $\overline{LD}$. Either four or all five ports may be used for selecting Overlay Registers. Unused inputs should be grounded. These inputs are used with bit CMD6 of the Command Register as follows (assuming no Read and no Blink Masking):

$OVLX_1$	$OVLX_0$	CMD6 = 1	CMD6 = 0
0	0	Color Palette RAM	Overlay Color 0
0	1	Overlay Color 1	Overlay Color 1
1	0	Overlay Color 2	Overlay Color 2
1	1	Overlay Color 3	Overlay Color 3

$PIXA_{0-7}$ through $PIXE_{0-7}$ Color Pixel Data Addresses (TTL-Compatible Inputs)
These 40 inputs are organized as five 8-bit addresses. Each 8-bit address selects which of the 256 entries in the Color Look-Up Table is to be used to provide pixel color information. These 40 inputs are latched into the input buffer on the rising edge of $\overline{LD}$. Either four or all five ports may be used for selecting color information. Unused inputs should be grounded.

Analog Section

COMP Compensation Capacitor Connection (Analog Input)
A 0.1-μF ceramic capacitor is connected between this pin and AV_{CC}.

FSADJ Full-Scale Adjust (Analog Input)
The magnitude of the full-scale video signal is controlled by a resistor connected between FSADJ and AGND. The typical value for this resistor for RS-343A into 37.5 ohms is 523 ohms.

R Red Video Output (Analog Output)
This is the analog output of the Red DAC. This output is capable of driving an RS-343A-compatible doubly terminated 75-ohm cable.

G Green Video Output (Analog Output)
This is the analog output of the Green DAC. This output is capable of driving an RS-343A-compatible doubly terminated 75-ohm cable. The SYNC current source is connected to this output.

B Blue Video Output (Analog Output)
This is the analog output of the Blue DAC. This output is capable of driving an RS-343A-compatible doubly terminated 75-ohm cable.

V_{REF} Voltage Reference (Analog Input)
An external voltage reference circuit must be used to supply this input with a 1.235-V (typical) reference.

MPU Interface

$AC_{0,1}$ Address Control (TTL-Compatible Inputs)
AC_0 and AC_1 allow the MPU to address any location in the Color Look-Up Table or any of the internal control registers. They are latched on the falling edge of $\overline{CE}$. See Table 1.

$\overline{CE}$ $\overline{Chip\ Select}$ (TTL-Compatible Input)
This signal enables the MPU interface. Data on D_{0-7} is internally latched on the rising edge of $\overline{CE}$ during Write operations.

D_{0-7} Data and Address Bus (TTL-Compatible Input/Output)
These eight pins are used to load and read back the internal control registers and the Color Look-Up Table. D_0 is the least-significant bit.

R/$\overline{W}$ Read/$\overline{Write}$ (TTL-Compatible Input)
R/$\overline{W}$ is latched on the falling edge of $\overline{CE}$. A "logical one" indicates a Look-Up Table or Register Read-Back operation. A "logical zero" indicates a Write operation.

Power Supply

AGND, DGND Analog, Digital Ground

AV_{CC}, DV_{CC} Analog, Digital +5-Volt Supply

FUNCTIONAL DESCRIPTION

The Am81C451/458 CMOS Color Palette integrates all the major functions required in the back-end of a video system, and supports pixel rates sufficient for most medium- to high-resolution monitors.

Four or five pixels are input in parallel from Display Memory and are serialized internally. A programmable Look-Up Table maps the serial pixel stream (address) into a physical color (data), and finally, three DACs convert the digital outputs of the look-up table into RS-343A-compatible RGB analog format.

Microprocessor Interface

A standard 8-bit MPU interface allows easy communication between the Am81C451/458 and most common MPUs. The $\overline{CE}$ and R/$\overline{W}$ inputs control MPU access timing, as shown in Figure 1. The AC_1 and AC_0 inputs select the access type as detailed in Table 1.

TABLE 1. AC_1, AC_0 DECODING

AC_1	AC_0	Access Type
0	0	Address Register
0	1	Look-Up Table
1	0	Control Registers
1	1	Overlay Registers

Fast access to the Look-Up Table and to the Overlay Registers is achieved by means of two internal counters: an 8-bit Address Register (AR0 – AR7), which generates addresses for the Color Memory locations and the Control Registers, and a Modulo 3 Counter (ARa,ARb) that controls which byte of the 24-bit Color Memory word is accessed. Tables 2 and 3 illustrate the operation of these two counters.

TABLE 2. ADDRESS REGISTER OPERATION

AR7-AR0	AC_1	AC_0	Location/Register Addressed by MPU
$00-$FF	0	1	Color Look-up Table Location #00-#FF
$00	1	1	Overlay Register 0
$01	1	1	Overlay Register 1
$02	1	1	Overlay Register 2
$03	1	1	Overlay Register 3
$04	1	0	Read Mask Register
$05	1	0	Blink Mask Register
$06	1	0	Command Register
$07	1	0	Test Register

TABLE 3. MODULO 3 COUNTER OPERATION

ARb	ARa	Color Byte Being Accessed
0	0	Red
0	1	Green
1	0	Blue

The Address Register, directly accessible by the MPU, auto-increments at the end of each third (Blue) access having $AC_0 = 1$. This feature avoids the rewriting of the Address Register with consecutive values, saving MPU time and Bus bandwidth for transfers to or from consecutive Color Memory locations.

The Modulo 3 Counter, not accessible by the MPU, increments at the end of each MPU access with $AC_0 = 1$ (color operations), and is reset to 0 at the end of each MPU access with $AC_0 = 0$ (Control Register operations).

Table 4 illustrates the Read/Write access to the Am81C451/458 palette.

TABLE 4. READ/WRITE ACCESS TO THE Am81C458

R/$\overline{W}$	AC_1	AC_0	ARb	ARa	Function
0	0	0	x	x	Write Address Register; AR7-AR0 ← D_{7-0}; ARb, ARa ← 0.
0	0	1	0	0	Write Red Color; RREG ← D_{7-0}; Incr. ARb, ARa.
0	0	1	0	1	Write Green Color; GREG ← D_{7-0}; Incr. ARb, ARa.
0	0	1	1	0	Write Blue Color; BREG ← D_{7-0}; ARb, ARa ← 0
					Write Color Look-Up Table; R7-R0 ← RREG; G7-G0 ← GREG; B7-B0 ← BREG; Incr. AR7-AR0.
0	1	0	x	x	Write Control Register; Reg (AR7-AR0) ← D_{7-0}; ARb, ARa ← 0.
0	1	1	0	0	Write Red Color; RREG ← D_{7-0}; Incr. ARb, ARa.
0	1	1	0	1	Write Green Color; GREG ← D_{7-0}; Incr. ARb, ARa.
0	1	1	1	0	Write Blue Color; BREG ← D_{7-0}; ARb, ARa ← 0;
					Write Overlay Register; R7-R0 ← RREG; G7-G0 ← GREG; B7-B0 ← BREG; Incr. AR7-AR0.
1	0	0	x	x	Read Address Register; D_{7-0} ← AR7-AR0; ARb, ARa ← 0.
1	0	1	0	0	Read Color LUT Red; D_{7-0} ← R7-R0; Incr. ARb, ARa.
1	0	1	0	1	Read Color LUT Green; D_{7-0} ← G7-G0; Incr. ARb, ARa.
1	0	1	1	0	Read Color LUT Blue; D_{7-0} ← B7-B0; ARb, ARa ← 0; Incr. AR7-AR0.
1	1	0	x	x	Read Control Register; D_{7-0} ← Reg (AR7-AR0); ARb, Ara ← 0.
1	1	1	0	0	Read Overlay Red; D_{7-0} ← R7-R0; Incr. ARb, ARa.
1	1	1	0	1	Read Overlay Green; D_{7-0} ← G7-G0; Incr. ARb, ARa.
1	1	1	1	0	Read Overlay Blue; D_{7-0} ← B7-B0; ARb, ARa ← 0; Incr. AR7-AR0.

Key:
← = "gets the value of"
D_{7-0} = MPU Data Bus
R7-R0 = Color Memory Red Byte
G7-G0 = Color Memory Green Byte
B7-B0 = Color Memory Blue Byte
RREG = Red Byte Register
GREG = Green Byte Register
BREG = Blue Byte Register
Reg (AR7-AR0) = Register pointed to by Address Register

Note that for the Am81C451 only the most significant data lines (D_7–D_4) are used while accessing the color lookup table or overlay registers. During a write cycle bits D_3–D_0 are ignored and during a read cycle bits D_3–D_0 are forced to logical zero.

If the pixel or overlay inputs address same entry in the color look-up table that is being written to by the MPU during blue write, the possibility exists that one or more pixels may be corrupted. Only one pixel may be corrupted if the MPU data is valid during the entire $\overline{CE}$ active time.

Display Memory Interface

The Am81C451/458 allows pixel data to be transferred from Display Memory at TTL-type data rates while presenting RGB information to the CRT at much higher rates through the use of internal latches and multiplexers.

Forty pixel data inputs ($PIXA_{0-7}$ through $PIXE_{0-7}$), ten overlay data inputs ($OVLA_{0,1}$ through $OVLE_{0,1}$), and two video inputs ($\overline{SYNC}$ and $\overline{BLANK}$), are loaded on the rising edge of $\overline{LD}$. An input MUX performs a 4:1 or a 5:1 serialization based on the FORMAT bit (CMD7) of the Command Register. During each clock cycle the Am81C451/458 outputs video information based first on the $PIXA_{0-7}$ inputs, then the $PIXB_{0-7}$ inputs, and so on until the $PIXD_{0-7}$ inputs (CMD7 = 0) or $PIXE_{0-7}$ inputs (CMD7 = 1), at which time the cycle repeats.

No phase relationship is imposed on the $\overline{LD}$ and CLK inputs; the only requirement is that the $\overline{LD}$ frequency be one-fourth or one-fifth of pixel clock (CLK, $\overline{CLK}$ depending on the CMD7 bit of the Command Register). This is obtained by virtue of an on-chip Locking Circuit that guarantees stable inputs to the Resync Register during positive transitions of the internal load signal (see Figure 1).

Note that the pixel data, overlay data, and $\overline{SYNC}$ and $\overline{BLANK}$ are loaded with the same $\overline{LD}$ clock to maintain synchronization with video data inside the Am81C451/458.

Color Selection

During each clock cycle, 10 bits of data are transferred from the input MUX and processed by the Read Mask, Blink Mask, and Command Register (see Figure 2). The processed data then selects an entry in the color palette RAM or an Overlay Register to provide color information.

The Read Mask is used to selectively enable or disable bit-planes from being presented to the color palette RAM; the Blink Mask is used to selectively enable or disable blinking on a bit-plane. CMD4 and CMD5 in the Command Register determine the blink-rate duty cycle. The counter that generates the internal blink clock is incremented during vertical retrace intervals. Such intervals are detected when the $\overline{BLANK}$ input is LOW for a period of at least 256 $\overline{LD}$ cycles.

Overlay Color Selection

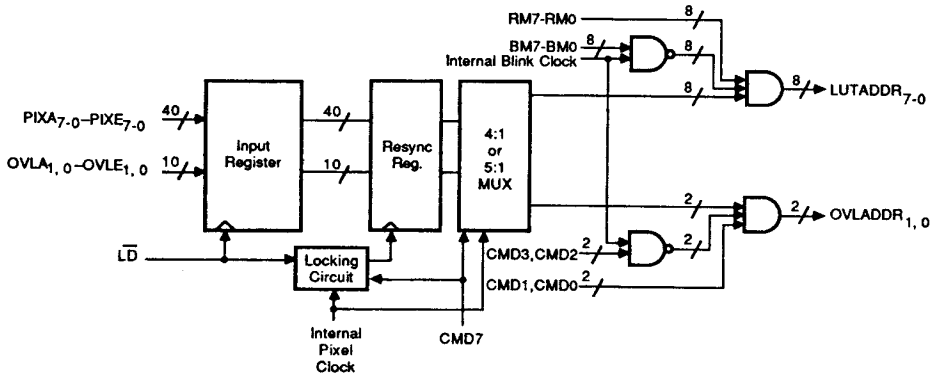
Four different overlay colors are available through four Overlay Registers. CMD1 and CMD0 in the Command Register act as Read Masks, and CMD2 and CMD3 in the Command Register act as Blink Masks on the overlay inputs (see Figure 1).

When $OVLADDR_1 = 0$ and $OVLADDR_0 = 0$ (see Figure 1), CMD6 of the Command Register selects between Overlay Register 0 and Look-Up Table output (determined by $LUTADDR_{7-0}$). See Table 5.

TABLE 5. OVERLAY COLOR SELECTION

$OVLADDR_1$	$OVLADDR_0$	CMD6 = 0	CMD6 = 1
0	0	Overlay Register 0	LUT
0	1	Overlay Register 1	Overlay Register 1
1	0	Overlay Register 2	Overlay Register 2
1	1	Overlay Register 3	Overlay Register 3

Key: LUT = Look-Up Table content addressed by $LUTADDR_{7-0}$
CMD6 = Bit 6 of Command Register (RAM Enable)



Note: CMDx bits are programmed in the Command Register
BMx bits are programmed in the Blink Mask Register
RMx bits are programmed in the Read Mask Register

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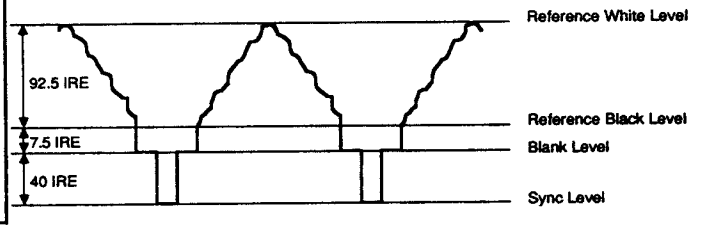
Figure 1. Input MUX and Masking Stage

Video Generation

During each clock cycle, 12(24) bits of information from either the Look-Up Table or an Overlay Register are presented to the three 4-bit (8-bit) DACs. These DACs convert the Color Memory digital output into RGB RS-343A analog format.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs are routed to the DACs after a delay equal to the pipeline delay incurred by the video stream to produce the relative Blank and Sync levels. $\overline{BLANK}$ is routed to all three DACs while $\overline{SYNC}$ is routed only to the Green DAC. See Figure 2 for DAC current and voltage levels.

RED	BLUE	GREEN	
mA	mV	mA	mV
19.04	714	26.67	1000
1.44	54	9.07	340
0.00	0	7.63	286
-	-	0.00	0



10451C-007A

DF006680

Note: 75-Ω doubly terminated load. Sync on Green DAC only. When Sync is used, the Green DAC current output is 7.63 mA higher than the corresponding Red or Blue current ouputs. When Sync is not used, Green, Red, and Blue outputs are identical.

Figure 2. DAC Current and Voltage Levels

3

User-Accessible Registers

In addition to the address register, there are four user-accessible registers: Command, Read Mask, Blink Mask, and Test. These registers should be initialized after power-up.

Command Register (CMD7 – CMD0)

This is an 8-bit register located at address #6, and is described below.

TABLE 6. COMMAND REGISTER DEFINITION

Position	Name	Description
CMD7	**FORMAT** 0 = 4:1 Multiplexing 1 = 5:1 Multiplexing	CMD7 specifies whether 4:1 or 5:1 multiplexing should take place on the pixel and overlay data. If CMD7 is set to logical '0' (4:1 multiplexing), $\overline{LD}$ should be one-fourth the frequency of CLK; the $PIXE_{0-7}$ and $OVLE_{0,\ 1}$ inputs are ignored and should be connected to GND. If CMD7 is set to logical '1' (5:1 multiplexing), $\overline{LD}$ should be one-fifth the frequency of CLK.
CMD6	**RAM Enable** 0 = Use Overlay Register 0 1 = Use LUT	When the processed overlay inputs $OVLADDR_1$ and $OVLADDR_0$ equal (0, 0) this bit selects between the Color Look-Up Table output and Overlay Register 0.
CMD5, CMD4	**Blink Rate Select** 00 = 25/75 (16/48) 01 = 50/50 (16/16) 10 = 50/50 (32/32) 11 = 50/50 (64/64)	These bits specify the blink rate and duty cycle of the internal blink clock. Numbers in parentheses specify the rate and duty cycle of the internal blink clock (logic I/logic 0) expressed in vertical retrace intervals. See Figure 1.
CMD3	**OVL_1 Blink Mask** 0 = Disable Blinking 1 = Enable Blinking	When this bit is set to a logical 1, the $OVLA_1$ Through $OVLE_1$ inputs are allowed to toggle at the selected blinking blink rate between the input value and logical 0 before being applied to the LUT/Overlay decode logic. When this bit is set to logical 0 it does not affect the $OVLA_1$ through $OVLE_1$ inputs.
CMD2	**OVL_0 Blink Mask** 0 = Disable Blinking 1 = Enable Blinking	When this bit is set to a logical 1, the $OVLA_0$ through $OVLE_0$ inputs are allowed to toggle at the selected blink rate between the input value and logical 0 before being applied to the LUT/Overlay decode logic. When this bit is set to logical 0 it does not affect the $OVLA_0$ through $OVLE_0$ inputs.
CMD1	**OVL_1 Read Mask** 0 = Disable Mask 1 = Enable Mask	When this bit is set to logical 0, the $OVLA_1$ through $OVLE_1$ inputs are forced to logical 0 before being applied to the LUT/Overlay decode logic. When this bit is set to logical 1 it does not affect the $OVLA_1$ through $OVLE_1$ inputs.
CMD0	**OVL_0 Read Mask** 0 = Disable Mask 1 = Enable Mask	When this bit is set to logical 0, the $OVLA_0$ through $OVLE_0$ inputs are forced to logical 0 before being applied to the LUT/Overlay decode logic. When this bit is set to logical 1 it does not affect the $OVLA_0$ through $OVLE_0$ inputs.

Read Mask Register (RM7 – RM0)

This is an 8-bit register located at address #4. It selectively enables (logical 1) or disables (logical 0) pixel bit-planes from addressing the Color Look-Up Table. Bit RM0 will mask inputs $PIXA_0$ through $PIXE_0$; bit RM1 will mask inputs $PIXA_1$ through $PIXE_1$; and so on.

Overlay plane masking is controlled by bits CMD1 and CMD0 of the Command Register. See Figure 1.

Blink Mask Register (BM7 – BM0)

This is an 8-bit register located at address #5. It selectively enables (logical 1) or disables (logical 0) pixel bit-planes from blinking. Bit BM0 will mask inputs $PIXA_0$ through $PIXE_0$; bit BM1 will mask inputs $PIXA_1$ through $PIXE_1$; and so on. When enabled, that particular bit-plane will toggle between its original value and logical 0 at the selected rate and duty cycle.

Overlay plane blinking is controlled by bits CMD3 and CMD2 of the Command Register. See Figure 1.

Test Register (T7 – T0)

This is an 8-bit register located at address #7. It is used to read back data presented to the DACs from the Color Memory (either pixel or overlay data). The four most-significant bits, T7 – T4, contain color information while the four least-significant bits, T3 – T0, contain control information, as shown in Table 7. T7 – T4 are defined only when exactly one of the T2 – T0 bits is a "logical one". Note that for the Am81C451, bit T3 is forced to logical zero.

When unused, this register should be initialized to Hex 00.

TABLE 7. TEST REGISTER DEFINITION

Test Register Bits	Function
T7-T4	Color Nibble
T3	1 = Select LOW Nibble 0 = Select HIGH Nibble
T2	1 = Enable Blue Data 0 = Disable Blue Data
T1	1 = Enable Green Data 0 = Disable Green Data
T0	1 = Enable Red Data 0 = Disable Red Data

As an example, in order to read the least-significant 4 bits of data presented to the Green DAC, the user must first write Hex 0A to the Test Register to enable the LOW nibble and green data. Subsequently, the user reads the Test Register, keeping the pixel inputs constant; bits D7 – D4 of the MPU interface Bus will contain the desired color data while bits D3 – D0 will contain Hex A.

When reading the Test Register, the data presented to the DAC inputs must be held stable during this period either by slowing the pixel clock or by holding the pixel and overlay inputs constant.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature
Under Bias ..... −55 to +125°C
Junction Temperature ..... +175°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs for
HIGH Output State ..... −0.5 V to V_{CC} Max.
DC Input Voltage GND ..... −0.3 to V_{CC} + 0.3 V
DC Input Current ..... −10 to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Military (M) Devices
Case Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A Subgroups 1, 2, 3, 7, & 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
DIGITAL CLOCK INPUTS (CLK, $\overline{CLK}$)							
V_{CKIH}	Input HIGH Voltage			V_{CC} − 1.0		V_{CC} + 0.5	V
V_{CKIL}	Input LOW Voltage			GND − 0.5		V_{CC} − 1.6	V
I_{CKIH}	Input HIGH Current					1	µA
I_{CKIL}	Input LOW Current					−1	µA
C_{CKIN}	Input Capacitance	f = 1 MHz, V_{IN} = 4.0 V				10	pF
DIGITAL INPUTS (Except CLK, $\overline{CLK}$)							
V_{IH}	Input HIGH Voltage			2.0		V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			GND − 0.5		0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V				1	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V				−1	µA
C_{IN}	Input Capacitance	f = 1 MHz, V_{IN} = 2.4 V				10	pF
DIGITAL OUTPUTS (D_{0-7})							
V_{OH}	Output HIGH Voltage	I_{OH} = 800 µA		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 6.4 mA				0.4	V
I_{OZ}	Three-State Current					10	µA
C_{OUT}	Output Capacitance				10		pF
ANALOG OUTPUTS (R_{FS} = 523 Ω, V_{REF} = 1.235 V)							
	Resolution (Each DAC)			4 (8)		4 (8)	Bits
LIN_i LIN_d	Accuracy (Each DAC): Integral Linearity Differential Linearity LSB Output Current		COM'L		69.1	±⅛ (±1) ±1/16 (±1)	LSB
			MIL			+⅛ (±2) +1/16 (±1)	
	LSB Output Current				1175 (69.1)		µA
	Gray Scale Error	% Gray Scale				±5	%
	Monotonicity					Guaranteed	
	Coding	Binary					
	Output Current: White Level Relative to Blank Level White Level Relative to Black Level Black Level Relative to Blank Level Blank Level on R, B Blank Level on G Sync Level on G	R_{FS} = 523 Ω, V_{REF} = 1.235 V		17.69 16.74 0.95 0 6.29 0	19.05 17.62 1.44 5 7.62 5	20.40 18.50 1.90 50 8.96 50	mA mA mA µA mA µA
	DAC-to-DAC Matching				2	5	%
V_{OC}	Output Compliance			−1.0		+1.2	V
R_{OUT}	Output Impedance				50		kΩ
C_{OUT}	Output Capacitance	f = 1 MHz, I_{OUT} = 0 mA			13	20	pF
I_{REF}	Volt Reference Input Current				10		µA
PSRR	Power Supply Rejection Ratio	C_{COMP} = 0.1 µF f = 1 KHz			0.5		%/%Δ V_{CC}

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 unless otherwise noted)

No.	Parameter Symbol	Parameter Description	165 MHz			125 MHz			110 MHz			80 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DIGITAL CPU INTERFACE TIMING															
1	t_S	R/$\overline{W}$, AC_0, AC_1 Setup Time	0			0			0			0			ns
2	t_H	R/$\overline{W}$, AC_0, AC_1 Hold Time	15			15			15			15			ns
3	t_{CYC}	CPU Cycle Time	100			100			110			125			ns
4	t_W	$\overline{CE}$ LOW Active Time	70			75			85			100			ns
5	t_W	$\overline{CE}$ HIGH Time	25			25			25			25			ns
6	t_{PD}	$\overline{CE}$ Edge to Data Bus Driven (C_L = 40 pF)	10			10			10			10			ns
7	t_{PD}	$\overline{CE}$ Edge to Data Valid (C_L = 40 pF)			70						85			100	ns
8	t_{PD}	$\overline{CE}$ Edge to Data Three-Stated (C_L = 40 pF)			15			15			15			15	ns
9	t_S	Write Data Setup Time	35						40			50			ns
10	t_H	Write Data Hold Time	0			0			0			0			ns
DIGITAL VIDEO PATH TIMING															
11	f_{CK}	Video Clock Frequency			165			125			110			80	MHz
12	f_{LD}	$\overline{LD}$ Rate			41.25			31.25			27.5			20	MHz
13	t_{CYC}	$\overline{LD}$ Cycle Time	24			32			36.36			50			ns
14	t_W	$\overline{LD}$ Pulse Width [illegible]	9			13			15			20			ns
15	t_W	$\overline{LD}$ Pulse Width [illegible]	9			13			15			20			ns
16	t_S	PIX_X, OVL_X, SYNC and $\overline{BLANK}$ Setup Time	2			3			3			4			ns
17	t_H	PIX_X, OVL_X, SYNC and $\overline{BLANK}$ Hold Time	2			2			2			2			ns
18	t_{CYC}	Clock Cycle Time	6			8			9.09			12.5			ns
19	t_W	Clock Pulse Width LOW	2.4			3.2			4.0			5.0			ns
20	t_W	Clock Pulse Width HIGH	2.4			3.2			4.0			5.0			ns
21	t_R, t_F	Clock Rise/Fall Time (20%-80%)			1.6			1.6			1.6			1.6	ns
22		Pipeline Delay	6		10	6		10	6		10	6		10	Clks

Notes: See notes following end of table continued on next page.

SWITCHING CHARACTERISTICS over operating ranges (Cont'd.)

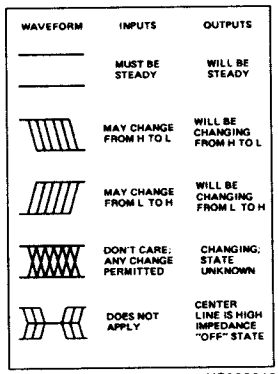
No.	Parameter Symbol	Parameter Description		165 MHz			125 MHz			110 MHz			80 MHz			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
ANALOG VIDEO DAC TIMING																
23		Analog Output Delay			20			20			20			20		ns
24	t_R, t_F	Analog Output Rise and Fall Time (Note 1)			2			2			2			2		ns
25	t_S	Analog Output Settling Time (Notes 1, 2)				6						8			12	ns
26		Analog Output Skew			0			0			0	2		0	2	ns
27		Glitch Impulse Energy (Note 2)			50			50			50			50		PV-sec
28		Clock and Data Feedthrough (Note 3)			TBD			TBD			TBD			TBD		dB
DYNAMIC POWER DISSIPATION																
		I_{CC} (Supply Current)	COM'L		270	370		250	340		240	330		230	295	mA
			MIL	–	–	–		250	425		240	410		230	370	

Notes: 1. Clock and data feedthrough is not included.
2. Includes clock and data feedthrough, –3–dB bandwidth = 2 x clock frequency.
3. Measurement performed on TTL digital inputs with 74HC logic level and with 1-kohm resistor to GND.

Test Conditions: TTL Input Level: 0 to 3 V with t_R, t_F(10-90%) ≤ 3 ns;
ECL Input Level: (V_{CC} - 0.8 V) to (V_{CC} - 1.8 V) with t_F, t_R (20-80%) ≤ 2 ns;
R_{SET} = 523 ohms, V_{REF} = 1.235 V;
Analog Output Load ≤ 10 pF; D_{0-7} Output Load ≤ 40 pF.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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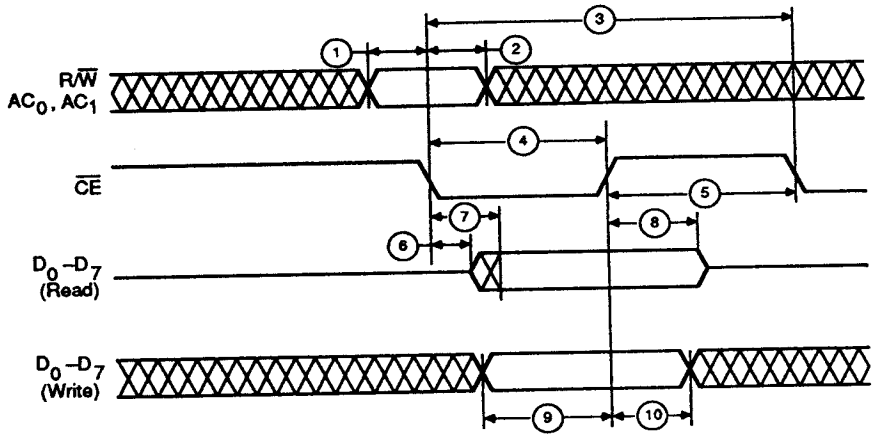
SWITCHING WAVEFORMS (Cont'd.)



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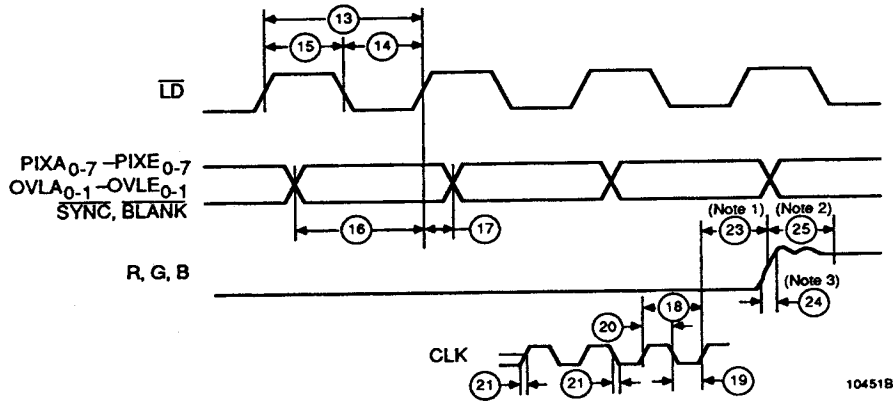
WF026630

CPU Read/Write Timing



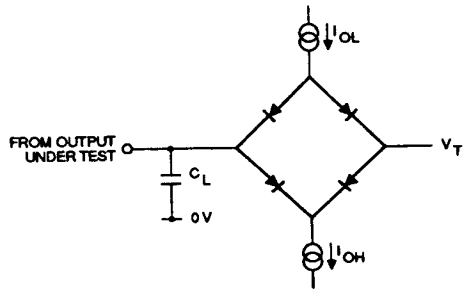
10451B-005A

WF026430

Notes: 1. Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale level.
2. Output settling time measured from 50% point of full-scale level to output settling within ±1 LSB.
3. Output rise/fall time measured between 10% and 90% points of full-scale level.

Video Input/Output Timing

SWITCHING TEST CIRCUIT



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Notes: 1. $C_L = 50$ pF (includes scope probe, wiring, and stray capacitance without device in test fixture).
2. $V_T = 1.5$ V.

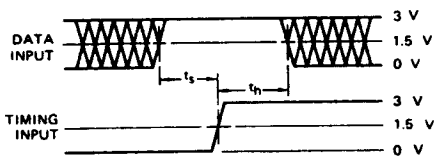
Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.

3

SWITCHING TEST WAVEFORM



WF021191

Notes: 1. Diagram show for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched are is don't care condition.

Setup and Hold Times

APPENDIX A — APPLICATION NOTE FOR THE Am81C458

The design of a system using the Am81C458 should be guided by considerations similar to those used for designing precision high-speed mixed analog and digital systems. The following rules and examples are given for orientation purposes. Users may choose to design circuits, differently from the examples given here.

Power pins should be decoupled from power lines of the rest of the system. The circuit board layout should have a dedicated analog power plane. The power plane should be connected to the main power plane by wires running through ferrite beads. The analog plane should be small enough so that no digital signal passes under it (see Figures A1 and A2).

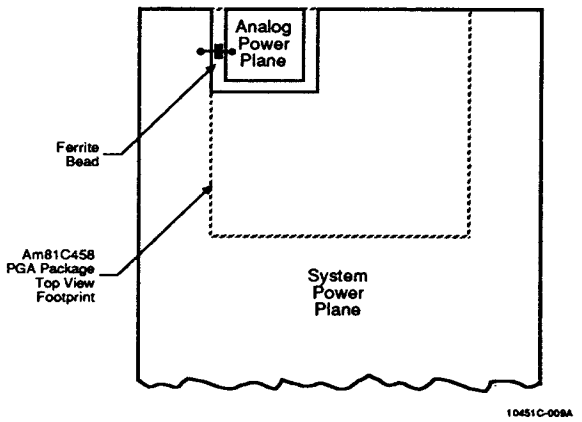


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Figure A1. Example of Power Planes Layout

There should be only one ground plane for all digital and analog ground pins, which is the same ground plane of the rest of the board. Tantalum capacitors, in parallel with a 0.1-μF ceramic capacitor, would be placed between each side of the ferrite beads and the ground plane. If too much ripple exists on the supply lines, the use of a dedicated linear regulator only for the Am81C451/458 is recommended.

The two groups of digital V_{CC} (DV_{CC}) pins should be decoupled from each other by connecting a 0.1-μF capacitor and a 0.01- μF capacitor in parallel between them and the closest group of digital ground pins (DGND).

A 0.1-μF ceramic capacitor, in parallel with a 0.001-μF chip capacitor, should be connected between each group of analog power pins (AV_{CC}) and the group of analog ground pins (AGND).

The COMP pin should also be decoupled from the power pins and the rest of the system. A 0.1-μF and a 0.01-μF chip capacitor should be connected, in parallel, between the COMP pin and the analog power plane.

Digital lines concerning the CPU interface should be kept far from pixel data lines. Pixel clock lines should be kept far from all other digital inputs. Analog outputs should be kept far from any other input. No digital line should run under the analog plane. The $\overline{CE}$ line should be as short as possible to minimize any noise picked up from other sources.

Connection with the monitor should be done through a doubly terminated 75-ohm coaxial cable. To minimize reflections, terminating resistors on the color palette side should be placed as close as possible to the R, G, B outputs.

The signals produced by the Am81C451/458, including Sync, are all positive (outgoing) currents, which when passing through the terminating resistors produce positive voltages. Since most monitors are AC-coupled, DC restoration with the proper DC levels is done inside the monitor. If a negative-going Sync (of −0.286 V) is required, DC-level shifting can be done outside the palette, prior to entering the transmission cable. Two possible circuits that produce the level shifting are shown here.

The first circuit (Figure A3) shows the 75-ohm terminating resistor relative to the green DAC, connected between the G output and a voltage source of −0.572 V. This resistor, in series with the other 75-ohm terminator inside the monitor, constitutes a voltage divider which forces the voltage on the line to be offset by half of 0.572 V (i.e., 0.286 V).

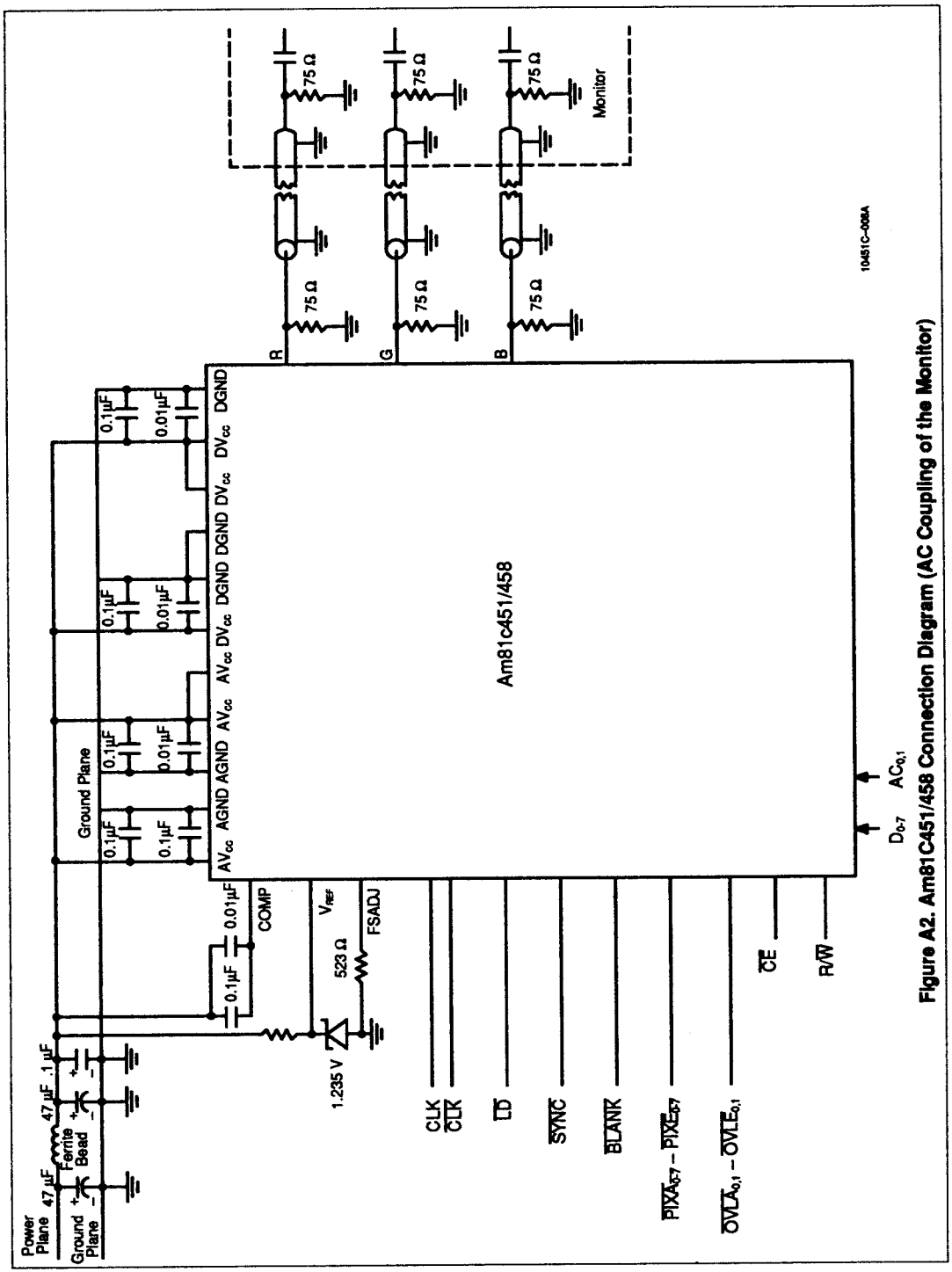

Figure A2. Am81C451/458 Connection Diagram (AC Coupling of the Monitor)

3

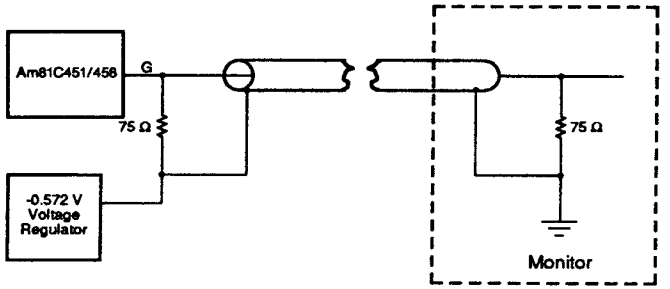

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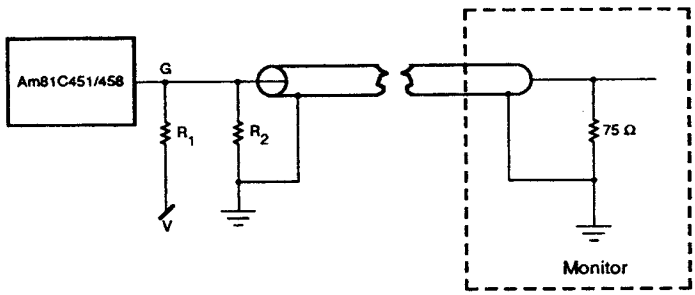
Figure A3. DC-Level Shifting Using a Voltage Regulator

The second circuit (Figure A4), useful if an exact 0.572-V voltage source is not available, shows two resistors (R_1 and R_2) instead of one, constituting the terminator at the transmitting side. R_1 is connected between the green DAC output and ground, while R_2 is connected between the green DAC output and a voltage source more negative than 0.572 V. R_1 and R_2 are such that in parallel they constitute 75 ohms, while their ratio is such that the voltage drop caused by the negative voltage source across R_1 is 0.572 V. This relationship is described by the following formulas:

$$R_2 = \frac{V \times 75}{-0.572}$$

$$R_1 = \frac{V \times 75}{V - 0.572} \quad \text{or} \quad R_1 = \frac{R_2 \times 75}{R_2 - 75}$$

The variable voltage drop across the parallel of R_1 and R_2 caused by the DAC currents adds to that caused by the external voltage source.



V	R_1	R_2
-5 V	655 Ω 1%	85 Ω 1%
-12 V	1573 Ω 1%	79 Ω 1%

BD003240

Figure A4. DC-Level Shifting Using Two Resistors in Parallel

TYPICAL APPLICATION

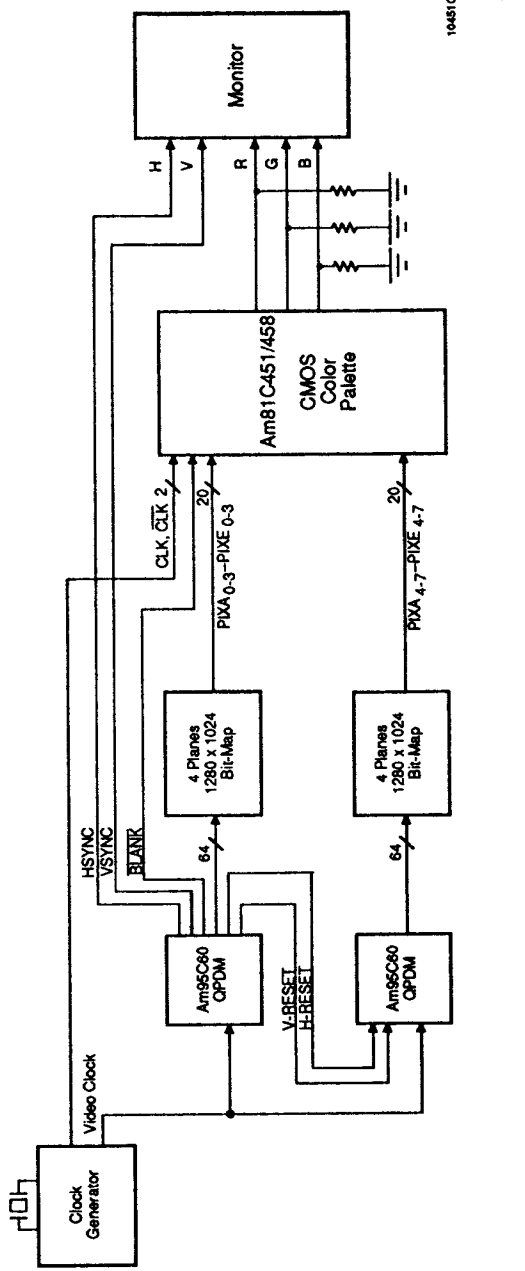


Figure A5. Application Example: Graphic System Using Two Am95C60 QPDMs and an Am81C451/458 Color Palette