

AmMCL00XA

2 or 4 Megabyte 3.0 Volt-only Flash Miniature Card

DISTINCTIVE CHARACTERISTICS

- **2 or 4 MBytes of addressable Flash memory**
- **2.7 V to 3.6 V, single power supply operation**
 - Write and read voltage: 3.0 V $-10/+20\%$
 - No additional supply current required for V_{PP}
- **Fast access time**
 - 150 ns maximum access time
- **CMOS low power consumption**
 - Typical active read current:
20 mA (word mode)
 - Typical active erase/write current:
40 mA (word mode)
 - Typical standby current:
25 μ A (4 MByte); 1 μ A (2 MByte)
- **High write endurance**
 - Guaranteed minimum 100,000 write/erase cycles per card
 - More than 1,000,000 cycles per card typical
- **Uniform sector architecture**
 - 64K byte individually useable sectors
 - Erase Suspend/Resume increases system level performance
 - $\overline{BUSY}$ (RY/ $\overline{BY}$, Ready/ $\overline{Busy}$) and $\overline{RESET}$ signals
- **Zero data retention power**
 - Batteries not required for data storage
- **Miniature Card standard form factor**
 - True interchangeability
 - 60-pad elastomeric connector
 - Supports multiple technologies
 - Sonic welded stainless steel case
 - PCMCIA Type II adapter available
 - Selectable byte- or word-wide configuration
- **60 connection bus**
 - 16-bit data bus
 - 25-bit address bus
 - Easy system integration
 - Low cost implementation
 - Low cost cards
- **Small Form Factor (38 mm x 33 mm x 3.5 mm)**
 - Minimized system area consumed by card
 - 16-bit non-multiplexed data bus addressing up to 4 MBytes
- **Consumer-friendly mechanicals**
 - User can easily insert and remove card, upgrade memory, and add applications
- **Voltage level keying**
 - Does not allow a 3 V card to plug into a 5 V system and vice versa
 - Single power supply design
 - System does not need a separate program voltage supply; only one is necessary to read and write

GENERAL DESCRIPTION

The Miniature Card is an expansion card that provides a low cost, low power, high-performance, small form factor solution for data and file storage to the portable, handheld market, which includes audio, digital film, wireless, and PDA (Portable Digital Assistant) applications.

Miniature cards can be easily “snapped” into the back of an electronic system and can be readily removed and replaced by end users. AMD’s 3 V Flash Miniature

Cards are manufactured using AMD’s industry leading 3.0 volt-only, single-power-supply Am29LV081 Flash Memory device, ensuring high reliability and excellent performance. The Miniature Card is less than 30% of the size of a PCMCIA memory card. Applications include digital voice recorders, pocket PCs and intelligent organizers, Smart cellular telephones, voice and data messaging pagers, digital still cameras and portable instrumentation.

The Miniature Card specification is defined by the Miniature Card Implementers Forum. The forum members

include major Flash memory vendors and leading consumer electronics OEMs. The goal of the forum is to promote an open, interoperable small form factor memory card standard. For more information on the Miniature Card specification, visit their web site at <http://www.mcif.org>.

AMD Flash Miniature Cards can be read in either a byte-wide or word-wide mode, which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification.

The Miniature Card is also designed with low-cost and rugged handling in mind. The card contains virtually no control logic, which keeps cost and power consumption to a minimum. The Miniature Card is packaged in a sonic welded, stainless steel case that guarantees durability, provides good ESD protection and ease of handling. The Miniature Card connects to the system via a state-of-the-art elastomeric connector. The elastomeric connector is based on a silicon rubber substrate with silver conductors, and offers a low-profile, low cost and reliable connection between the memory card and the system. Unlike alternative pin and socket solutions, the elastomer can be easily replaced if

damaged and requires minimal space on the system motherboard.

The Miniature Card has extensive third-party support, including socket and connector solution from Augat, software support from the major FTL software vendors, and PCMCIA adapter solutions and programmer support.

AMD's Miniature Flash cards can be used for both code and data storage. Since fast random access is possible, code can be directly executed from the card, reducing the amount of system RAM required. In addition, AMD's Flash technology offers unsurpassed endurance, data retention and reliability, eliminating the need for complex error correction and defect management hardware and software. Each Flash sector provides a minimum of 100,000 cycles, and a typical card life of one million or more cycles.

For more information, please contact your local AMD sales office or visit our Web site at <http://www.amd.com/html/products/nvd/nvd.html>.

DEFINITIONS

Table 1 lists the terms and definitions that may be used in conjunction with Miniature Card specifications.

Table 1. Miniature Card Definitions

Term	Meaning
AIS	Acronym for Attribute Information Structure. AIS is a Miniature Card specification for storing Miniature Card attribute information.
Elastomeric connector	A connector that is made of alternating layers of conductive and non-conductive silicone rubber.
ESD	Acronym for Electrostatic Discharge. ESD is part of the Miniature Card physical test suite.
FAT	Acronym for File Allocation Table. A FAT is a common method for managing files. FAT is used in DOS based system.
Flash	A type of non-volatile memory that is both readable and writeable, but requires the media to be erased before it is rewritten.
Host	Any system that incorporates a Miniature Card socket
Insertion, Cold	<i>User Perception:</i> Insertion of the Miniature Card when the host is off. <i>Host State:</i> The host would be either off or in sleep mode, no bus activity is occurring, the host is non-operational by the user. The user inserts the Miniature Card and then presses a button to turn the host on before the system is operational.
Insertion, Hot	<i>User Perception:</i> Insertion of a Miniature Card when the host is running. <i>Host State:</i> The host would be in running mode, bus activity is occurring, the host is operational by the user. The user inserts the card, the host recognizes it, and the host continues to be operational. Note: Hot insertion may require buffering on the host system for proper operation.
Insertion, Pseudo Hot	<i>User Perception:</i> Insertion of a Miniature Card when the host is running. <i>Host State:</i> The host would be in running mode, bus activity is occurring, the host is operational by the user. The user inserts the card, the host immediately powers off before the Miniature Card makes contact with the host's internal bus. The user would then need to press a button to turn the host on for it to become operational.
Interface Signals	Miniature Card signals that make connection through the elastomeric connector.

Table 1. Miniature Card Definitions (Continued)

Term	Meaning
JEDEC	Acronym for Joint Electronic Device Engineering Council
Miniature Card Backside	The side of the Miniature Card that contains the latching mechanism. The backside is opposite the frontside.
Miniature Card Bottomside	The side of the Miniature Card that contains the interface signals. The bottomside is opposite the topside.
Miniature Card Frontside	The side of the Miniature Card that contains power, insertion, ground, voltage keys, and alignment notch. The frontside is opposite the backside.
Miniature Card Topside	The side of the Miniature Card that contains the Miniature Card label. The topside is opposite the bottomside.
PC Card	A memory or I/O card compatible with the PC Card Standard
PC Card Adapter	The hardware that connects the Miniature Card 60 contact bus to the PC Card 68 pin bus. This hardware can be mechanically implemented by following the PC Card Type II specification.
Power/Insertion Signals	The three signals on the frontside of the Miniature Card that provide ground, power and early detection of insertion.
Pull-Ups	Resistors used to ensure that signals do not float when no device is driving them.
Removal, Cold	<i>User Perception:</i> Removal of a Miniature Card when the host is off. <i>Host State:</i> The host would either be off or in sleep mode, no bus activity is occurring, the host is non-operational by the user. User would turn off the host, then remove the Miniature Card and then press a button to turn the host on for it to become operational again.
Removal, Hot	<i>User Perception:</i> Removal of the Miniature Card when the host is running. <i>Host State:</i> The host would be in running mode, bus activity is occurring, the host is operational by the user. User removes the card, the host recognizes the event, and the host continues to be operational.
Removal, Pseudo Hot	<i>User Perception:</i> Removal of the Miniature Card when the host is running. <i>Host State:</i> The host would be in running mode, bus activity is occurring, the host is operational by the user. User removes the card, the host recognizes the event, the host immediately powers off before the Miniature Card removes contact with the host's internal bus. The user would then need to press a button to turn the host on for it to be operational again.
Sector	Usually 64 KBytes. In word mode, a sector is 64 KWords.
Tuple	An element of the PC Card Standard CIS which provide card attribute information, and a link to the next tuple in a string of tuples.
User Insertable	All Miniature Cards should be inserted into the host by the user without the need for any special tools.
User Removable	This type of Miniature Card can be removed by the user without the need for any special tools. It contains programs and data that users may want to switch often. The use of this type of card is similar to a floppy disk.
User Non-Removable	This type of Miniature Card must be removed by the user with a special tool. It contains memory upgrades or boot program that users switches only when they require an upgrade. The use of this type of card is similar to a SIMM memory expansion or boot hard disk.
XIP	Acronym for eXecute-In-Place, which refers to code that executes directly from a Miniature Card.

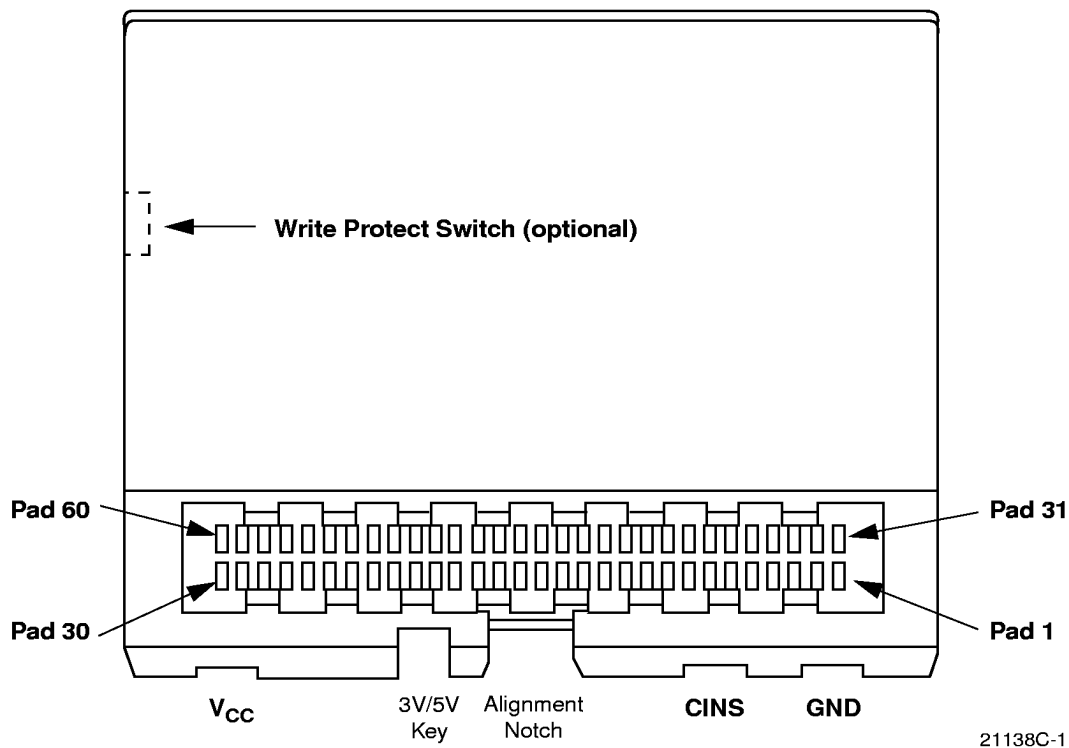


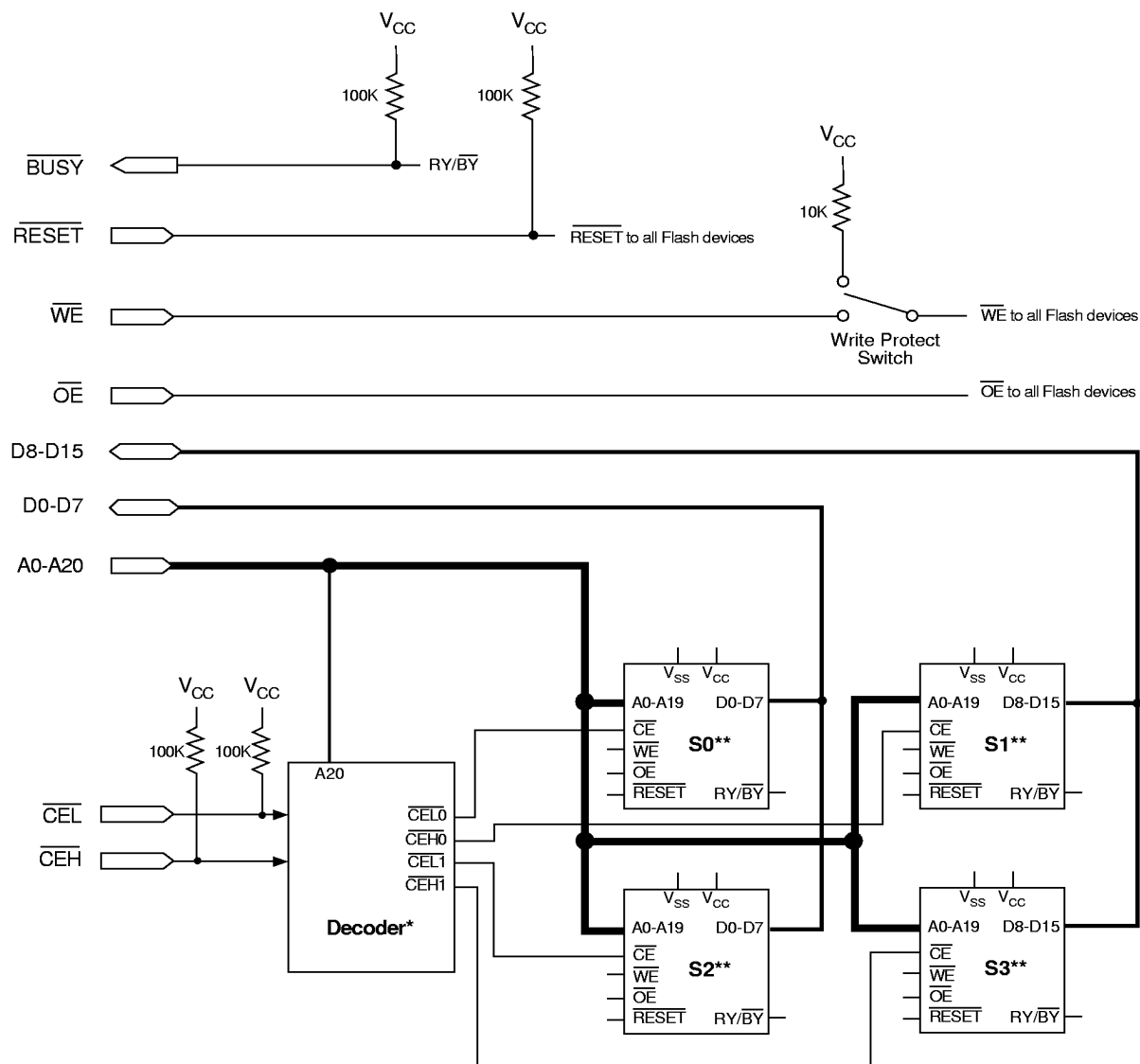
Figure 1. Miniature Card Connector (Card Bottom View)

Note: Refer to the Physical Dimensions section for more information. Also refer to the MCIF specification for detailed mechanical information, available on the Web at <http://www.mcif.org>.

Table 2. AMD Flash Miniature Cards and Flash Devices

Family Part Number	Density	No. of Flash Devices	AMD Flash Memory
AmMCL002A	2 MByte	2	Am29LV081
AmMCL004A	4 MByte	4	Am29LV081

BLOCK DIAGRAM



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* 4 MByte card only. Not used on 2 MByte card.

** 2 MByte card: Two Am29LV081 devices, S0 and S1
 4 MByte card: Four Am29LV081 devices, S0...S3

Note: On the 2 Mbyte card, A20–A24 are not connected. On the 4 MByte card, A21–A24 are not connected. Connections not shown in this diagram are **not connected** internally.

MINIATURE CARD PAD ASSIGNMENTS

A0–A24

Address A0 to A24 are the address bus lines that can address up to 32 Mwords (64 MBytes). The address lines are word addressed. The Miniature Card specification does not require the Miniature Card to decode the upper address lines. A 2 Mbyte Miniature Card that does not decode the upper address lines would repeat its address space every 2 MBytes. Address 0h would access the same physical location as 200000h, 400000h, 600000h, etc. On the 2 Mbyte cards, A20–A24 are not connected. On the 4 MByte cards, A21–A24 are not connected.

D0–D15

Data lines D0 through D15 constitute the data bus. The data bus is composed of two bytes; the low byte is D0–D7 and the high byte is D8–D15. These lines are tristated when $\overline{OE}$ is high.

$\overline{OE}$

$\overline{OE}$ indicates to the card that the current bus cycle is a read cycle. The output enable access time (t_{OE}) is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC} - t_{OE}$ time).

$\overline{WE}$

$\overline{WE}$ indicates to the card that the current bus cycle is a write cycle. The falling edge of $\overline{WE}$ (or $\overline{CE}$), whichever occurs later, latches address information and the rising edge of $\overline{WE}$ (or $\overline{CE}$), whichever occurs first latches data/command information.

$\overline{VS1}$

Voltage Sense 1 signal. This signal is grounded.

$\overline{VS2}$

Voltage Sense 2 signal. This signal is left open or not connected.

$\overline{CEL}$

$\overline{CEL}$ enables the low byte of the data bus (D0–D7) on the card.

$\overline{CEH}$

$\overline{CEH}$ enables the high byte of the data bus (D8–D15) on the card.

RESET

$\overline{RESET}$ controls card initialization. When $\overline{RESET}$ transitions from a low state to a high state, the Miniature Card resets to the Read state after a maximum delay of 20 μ s.

BUSY

$\overline{BUSY}$ is a signal generated by the card to indicate the status of operations within the Miniature Card. When $\overline{BUSY}$ is high, the Miniature Card is ready to accept the next command from the host. When $\overline{BUSY}$ is low, the Miniature Card is busy and unable to accept some data operations from the host. In Flash Miniature Cards the $\overline{BUSY}$ signal is tied to the components' $\overline{RY}/\overline{BY}$ signal.

$\overline{CD}$

$\overline{CD}$ is a grounded interface signal. After a Miniature Card has been inserted, $\overline{CD}$ will be forced low. The card detect signal is located in the center of the second row of interface signals, and should be one of the last interface signals to connect to the host. Do not confuse $\overline{CD}$ with $\overline{CINS}$. $\overline{CINS}$ is an early card detect that is one of the first signals to connect to the host.

$\overline{CINS}$

$\overline{CINS}$ is a grounded signal on the front of the Miniature Card that is used for early detection of a card insertion. $\overline{CINS}$ makes contact on the host when the front of the card is inserted into the socket, before the interface signals connect.

$\overline{BS8}$

The $\overline{BS8}$ (Bus size 8) signal indicates to the Miniature Card that the host has an 8-bit bus. AMD Flash Miniature Cards ignore this signal (no internal connection). An 8-bit host must connect its D0–D7 data lines to D8–D15 on the Miniature Card to retrieve the upper (odd) byte.

GND

Ground

V_{CC}

V_{CC} is used to supply power to the card.

NC

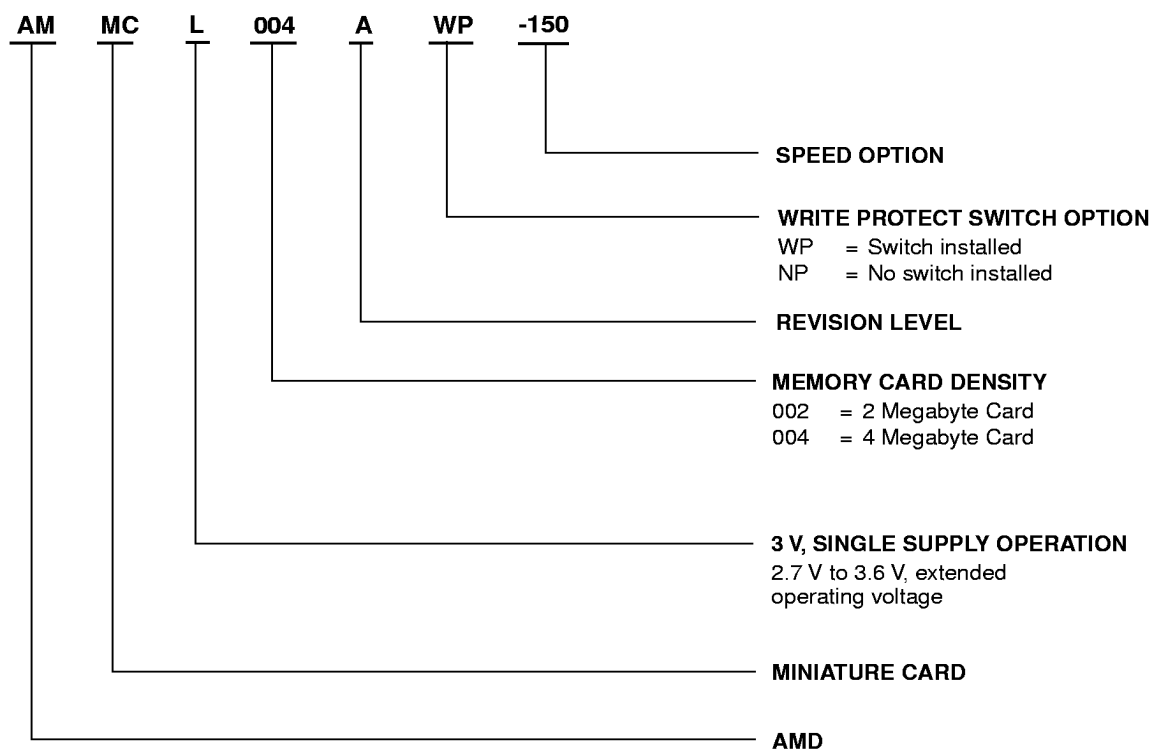
No connect

RFU

Reserved for future use

ORDERING INFORMATION**Standard Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



INTERFACE SIGNAL ASSIGNMENTS

Pad Number	Signal Name	Pad Number	Signal Name	Pad Number	Signal Name
1	A18	21	D12	41	A4
2	A16	22	D10	42	$\overline{\text{CE}}\overline{\text{L}}$
3	A14	23	D9	43	A1
4	NC	24	D0	44	NC
5	$\overline{\text{CE}}\overline{\text{H}}$	25	D2	45	NC
6	A11	26	D4	46	$\overline{\text{CD}}$
7	A9	27	RFU	47	A21
8	A8	28	D7	48	$\overline{\text{BUSY}}$
9	A6	29	NC	49	$\overline{\text{WE}}$
10	A5	30	NC	50	D14
11	A3	31	A19	51	RFU
12	A2	32	A17	52	D11
13	A0	33	A15	53	$\overline{\text{VS}}\overline{2}$
14	NC	34	A13	54	D8
15	A24	35	A12	55	D1
16	A23	36	$\overline{\text{RESET}}$	56	D3
17	A22	37	A10	57	D5
18	$\overline{\text{OE}}$	38	$\overline{\text{VST}}$	58	D6
19	D15	39	A7	59	RFU
20	D13	40	$\overline{\text{BS}}\overline{8}$	60	A20

Note: NC = No Connect; RFU = Reserved for Future Use.

FLASH MINIATURE CARD OPERATIONS

Voltage Sensing

AMD Miniature Cards provide two voltage sense signals for hosts that support multiple voltages. The multivoltage host can sense the voltage level of the Miniature Card and power up the card at that voltage. See Table 3 for a description of the voltage sense signals.

In addition to the voltage sense pins, there are also mechanical voltage keys on the Miniature Card that

ensure the card can only be inserted into host systems that can supply the proper voltage levels to the card. Refer to Section 4.1.2 in the Miniature Card specification for more information on mechanical keying.

Table 3. Voltage Sense Signals

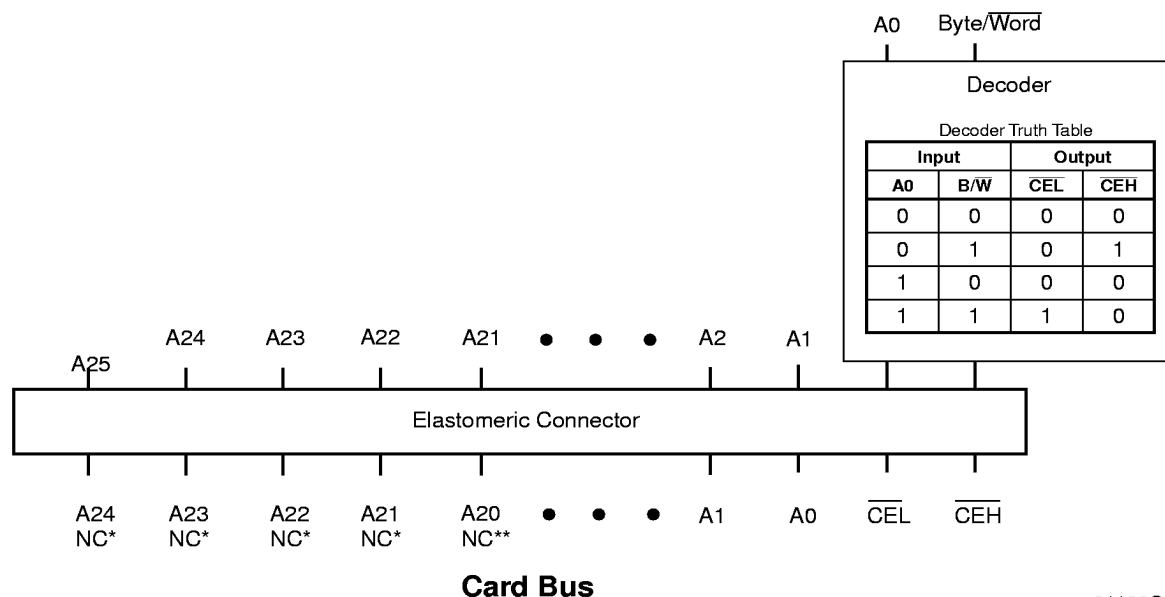
Miniature Card Power-Up Voltage	$\overline{\text{VS}}\overline{1}$	$\overline{\text{VS}}\overline{2}$
3 volt-only	Gnd	Open

Data Accesses

The Miniature Card has a 16-bit data bus that can accommodate word or byte accesses. By individually asserting $\overline{\text{CEL}}$ and $\overline{\text{CEH}}$, a host can access either byte. However, byte swapping (moving the high byte data to the low byte) is not supported.

Figure 2 shows the connections between the host and Miniature Card. The host system address lines range from A0–A25, whereas the Miniature Card address

lines range from A0–A24. On the host, A0 and the byte/word line are sent to a decoder and output to $\overline{\text{CEL}}$ and $\overline{\text{CEH}}$ on the Miniature Card. These two bits enable a single device for byte accesses and two devices for word accesses, as shown by the decoder truth table in Figure 2. Again, the Miniature Card address lines do not receive input from host address bit A0. In this document, all address references are **card addresses**, unless otherwise noted. Table 4 shows the read/write modes for Miniature Cards.



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* Not connected

** Not connected on 2 MByte card only

Figure 2. Host/Card Address Connections

Word-Wide Operations

The AMD Miniature Card provide the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations, the low bytes are controlled with $\overline{\text{CEL}}$. The high bytes are controlled with $\overline{\text{CEH}}$. Refer to the block diagram for more information.

Byte-Wide Operations

Byte-wide data is available for read and write operations ($\overline{\text{CEL}} = 0$, $\overline{\text{CEH}} = 1$). Even and odd bytes are stored in separate memory devices (for example, S0 and S1) and are accessed by controlling $\overline{\text{CEL}}$ and $\overline{\text{CEH}}$. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

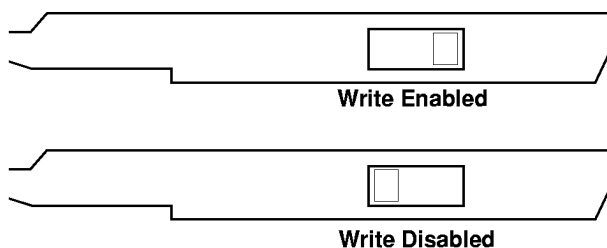
Each memory sector or device pair must be addressed separately for erase operations. Refer to the block diagram for more information.

Card Detection

Each $\overline{\text{CD}}$ (output) pin should be detected by the host system to determine if the memory card is adequately seated in the socket. $\overline{\text{CD}}$ and $\overline{\text{CINS}}$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Data Protection

An optional mechanical write protect switch provides user-initiated write protection. When this switch is activated, $\overline{\text{WE}}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands. This prevents the card from responding to any commands (for example, an Autoselect command). See Figure 3.



**Figure 3. Write Protect Switch
(Card Right Side View)**

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In addition to card-level data protection, AMD Flash Miniature Cards offer several device-level data protection features.

Device-Level Data Protection

AMD Flash memory devices offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up, each device automatically resets the internal state machine to the read mode. The control register architecture allows alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

AMD Flash memory devices also incorporates the following features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, the AMD memory devices in the Miniature Card lock out write cycles for $V_{CC} < V_{LKO}$ (see "DC Characteristics" on page 23 for voltages). When $V_{CC} < V_{LKO}$, the command register is disabled, all internal program/erase circuits are disabled, and the device resets to the read mode. The memory devices ignore all writes until $V_{CC} > V_{LKO}$. The user must

ensure that the control pins are in the correct logical state when $V_{CC} > V_{LKO}$ to prevent unintentional writes.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will neither initiate a write cycle nor change the command registers.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{CE} = \overline{WE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Read Mode

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins select and determine when to apply power to the high-byte and low-byte memory devices. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory device outputs. Refer to Table 4.

The Miniature Card automatically powers up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default state ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Table 4. Miniature Card Read/Write Modes

Function	$\overline{\text{CEH}}$	$\overline{\text{CEL}}$	WE	$\overline{\text{OE}}$	D8–D15	D0–D7
Read Mode						
Word Access	L	L	H	L	High Byte Data	Low Byte Data
Low Byte Access	H	L	H	L	High-Z	Low Byte Data
High Byte Access	L	H	H	L	High Byte Data	High-Z
Write Mode						
Word Access	L	L	L	H	High Byte Data	Low Byte Data
Low Byte Access	H	L	L	H	High-Z	Low Byte Data
High Byte Access	L	H	L	H	High Byte Data	High-Z
Standby Mode						
Standby	H	H	X	X	High-Z	High-Z

Notes:

1. Unlisted access combinations are invalid and may return unexpected results.
2. X indicates a don't care value.

Erase Operations

The AMD Flash Miniature Card is organized as an array of individual devices. Each Am29LV081 device contains sixteen 64 KByte sectors, for a total of 1 MByte of memory space per device.

Flash technology allows any logical “1” data bit to be programmed to a logical “0”. The only way to reset bits to a logical “1” is to erase that entire memory sector or memory device. Once a memory sector or memory device is erased, any address location may be programmed. Two or more devices may be erased concurrently when additional I_{CC} current is supplied to the card. However, erasing more than two devices concurrently is not typical in battery-powered applications, but may take place during procedures such as card testing.

Erase operations can be performed in several ways:

- Erase a single sector or multiple sectors in a device
- Erase a sector pair
- Erase multiple device pairs*
- Erase the entire card*

* This operation is only feasible in solutions capable of supplying more than the specified miniature card supply current requirement (150mA) per system. Each AMD Flash memory **device pair** can accept a maximum of 120mA supply current.

The common memory space data contents are altered in a similar manner to writing to individual Flash memory devices. An on-card address decoder activates the appropriate Flash device in the memory

array. Each device internally latches address and data during write cycles. Refer to Table 4.

Standby Mode

The AMD flash devices are designed to accommodate low standby power consumption. In order to achieve standby mode, the $\overline{\text{CE}}$ line must be deselected. In addition, while in the standby mode, data I/O pins remain in the high impedance state independent of the voltage level applied to the $\overline{\text{OE}}$ input. See the DC Characteristics section for more details on Standby Modes.

Deselecting $\overline{\text{CE}}$ ($\overline{\text{CE}}$ and $\overline{\text{RESET}} = V_{CC} \pm 0.3 \text{ V}$) puts the device into the I_{CC3} standby mode. If the device is deselected during an Embedded Algorithm operation, it continues to draw active power (I_{CC2}) prior to entering the standby mode, until the operation is complete. When the device is again selected ($\overline{\text{CE}} = V_{IL}$), active operations occur in accordance with the AC timing specifications.

Automatic Sleep Mode

Advanced power management features such as the automatic sleep mode minimize Flash device energy consumption. This is extremely important in battery-powered applications. The AMD memory devices automatically enable the low-power, automatic sleep mode when addresses remain stable for 300 ns. Automatic sleep mode is independent of the $\overline{\text{CE}}$, WE , and $\overline{\text{OE}}$ control signals. Typical sleep mode current draw from each device is $< 1 \mu\text{A}$. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

Command Definitions

Each memory device contains a command register, which is a latch that saves address, commands, and data information used by the state machine and memory array. The state machine is active when V_{CC} is greater than V_{LKO} (2.3 - 2.5 V). This is required for valid program and erase operations.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$ signals are at a logic-low level, and Output Enable ($\overline{OE}$) is at a logic-high, the command register is enabled for write operations. The falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs later, latches address information and the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first, latches data/command information.

Commands are accomplished by writing non-specific address and specific data sequences into the command register of accessed Flash memory devices.

Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode.

The byte-wide commands are defined in Tables 6 and 7; word-wide commands are defined in Table 5. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

Autoselect Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory device, as shown in Tables 5 through 7. When the autoselect command is issued to card address 00000H, the Miniature Card returns the manufacturer I.D. If the autoselect command is issued to card address 00001H, the Miniature Card provides the device I.D.

To terminate the autoselect operation, the Read/Reset command sequence must be written to the same device. The Autoselect command operates only if the card is not write protected.

Table 5. Word Command Definitions

Embedded Command Sequence (Note 1)	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Read/Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	1	XXXXH	F0F0H	RA	RW								
Autoselect Manufacturer ID	4	XXXXH	AAAAH	XXXXH	5555H	XXXXH	9090H	XX00H	0101H**				
Autoselect Device ID	4	XXXXH	AAAAH	XXXXH	5555H	XXXXH	9090H	XX01H	3838H**				
Word Write	4	XXXXH	AAAAH	XXXXH	5555H	XXXXH	A0A0H	PA	PW				
Device Erase	6	XXXXH	AAAAH	XXXXH	5555H	XXXXH	8080H	XXXXH	AAAAH	XXXXH	5555H	XXXXH	1010H
Sector Erase	6	XXXXH	AAAAH	XXXXH	5555H	XXXXH	8080H	XXXXH	AAAAH	XXXXH	5555H	SA	3030H
Sector Erase Suspend		XXXXH	B0B0H	Erase can be suspended during sector erase with Addr (don't care), Data (B0B0H)									
Sector Erase Resume		XXXXH	3030H	Erase can be resumed after suspend with Addr (don't care), Data (3030H)									

* During word addressing, $\overline{CE}L = 0$, $\overline{CE}H = 0$, and address is applied to Memory Device Pair 0 (S0 and S1). On 4 MByte cards, address for Memory Device Pair 1 = (Addr) + 200000H, and address is applied to Memory Device Pair 1 (S2 and S3). For host-to-card address bit connections, see Figure 2.

** This is not part of the command definition. This is data that will be read out.

Notes:

1. Write protect must not be enabled for proper operation of all commands except Reset/Read.
2. Address bits X = Don't Care for all commands except for Read Address (RA), Program Address (PA), and Sector Address (SA).
3. See Table 4 for read/write modes.
4. RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
SA = Address of the sector to be erased. Refer to Table 8 for sector addresses.
5. RW = Data read from location RA during read operation.
PW = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
6. Word = high byte + low byte.

Table 6. Even Byte Command Definitions

Embedded Command Sequence (Note 1)	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Read/Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	1	XXXXH	XXF0H	RA	RD								
Autoselect Manufacturer ID	4	XXXXH	XXAAH	XXXXH	XX55H	XXXXH	XX90H	XX00H	XX01H**				
Autoselect Device ID	4	XXXXH	XXAAH	XXXXH	XX55H	XXXXH	XX90H	XX01H	XX38H**				
Byte Write	4	XXXXH	XXAAH	XXXXH	XX55H	XXXXH	XXA0H	PA	PD				
Device Erase	6	XXXXH	XXAAH	XXXXH	XX55H	XXXXH	XX80H	XXXXH	XXAAH	XXXXH	XX55H	XXXXH	XX10H
Sector Erase	6	XXXXH	XXAAH	XXXXH	XX55H	XXXXH	XX80H	XXXXH	XXAAH	XXXXH	XX55H	SA	XX30H
Sector Erase Suspend		XXXXH	XXB0H	Erase can be suspended during sector erase with Addr (don't care), Data (XXB0H)									
Sector Erase Resume		XXXXH	XX30H	Erase can be resumed after suspend with Addr (don't care), Data (XX30H)									

* During even (low) byte accesses, $\overline{CE}L = 0$, $\overline{CE}H = 1$. Address is applied to Memory Device 0 (S0). On 4 MByte cards, address for Memory Device 2 (S2) = (Addr) + 200000H.

** This is not part of the command definition. This is data that will be read out.

Table 7. Odd Byte Command Definitions

Embedded Command Sequence (Note 1)	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Read/Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data	Addr*	Data
Reset/Read	1	XXXXH	F0XXH	RA	RD								
Autoselect Manufacturer ID	4	XXXXH	AAXXH	XXXXH	55XXH	XXXXH	90XXH	XX00H	01XXH**				
Autoselect Device ID	4	XXXXH	AAXXH	XXXXH	55XXH	XXXXH	90XXH	XX01H	38XXH**				
Byte Write	4	XXXXH	AAXXH	XXXXH	55XXH	XXXXH	A0XXH	PA	PDXXH				
Device Erase	6	XXXXH	AAXXH	XXXXH	55XXH	XXXXH	80XXH	XXXXH	AAXXH	XXXXH	55XXH	XXXXH	10XXH
Sector Erase	6	XXXXH	AAXXH	XXXXH	55XXH	XXXXH	80XXH	XXXXH	AAXXH	XXXXH	55XXH	SA	30XXH
Sector Erase Suspend		XXXXH	B0XXH	Erase can be suspended during sector erase with Addr (don't care), Data (B0XXH)									
Sector Erase Resume		XXXXH	30XXH	Erase can be resumed after suspend with Addr (don't care), Data (30XXH)									

* During odd (high) byte accesses, $\overline{CE}L = 1$, $\overline{CE}H = 0$, and address is applied to Memory Device 1 (S1). On 4 MByte cards, address for Memory Device 3 (S3) = (Addr) + 200000H + 100000H.

** This is not part of the command definition. This is data that will be read out.

Notes for Table 6 and Table 7:

- Write protect must not be enabled for proper operation of all commands except Reset/Read.
- For host-to-card address bit connections, see Figure 2.
- Address bit X= Don't Care for all address commands except for Program Address (PA), Read Address (RA) and Sector Address (SA).
- Bus operations are defined in Table 4.
- RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
SA = Address of the sector to be erased. Refer to Table 8 for sector addresses.
- RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$ pulse.

Table 8. Memory Sector Addresses

Sector	Card Address Bits				Device 0 and/or 1 (Note 1)	Device 2 and/or 3 (Note 1)
	A19	A18	A17	A16	Card Address Range	Card Address Range
0	0	0	0	0	00000h–0FFFFh	100000h–10FFFFh
1	0	0	0	1	10000h–1FFFFh	110000h–11FFFFh
2	0	0	1	0	20000h–2FFFFh	120000h–12FFFFh
3	0	0	1	1	30000h–3FFFFh	130000h–13FFFFh
4	0	1	0	0	40000h–4FFFFh	140000h–14FFFFh
5	0	1	0	1	50000h–5FFFFh	150000h–15FFFFh
6	0	1	1	0	60000h–6FFFFh	160000h–16FFFFh
7	0	1	1	1	70000h–7FFFFh	170000h–17FFFFh
8	1	0	0	0	80000h–8FFFFh	180000h–18FFFFh
9	1	0	0	1	90000h–9FFFFh	190000h–19FFFFh
10	1	0	1	0	A0000h–AFFFFh	1A0000h–1AFFFFh
11	1	0	1	1	B0000h–BFFFFh	1B0000h–1BFFFFh
12	1	1	0	0	C0000h–CFFFFh	1C0000h–1CFFFFh
13	1	1	0	1	D0000h–DFFFFh	1D0000h–1DFFFFh
14	1	1	1	0	E0000h–EFFFFh	1E0000h–1EFFFFh
15	1	1	1	1	F0000h–FFFFh	1F0000h–1FFFFh

Notes:

- For word addressing, devices 0 and 1 (S0 and S1) together form Memory Device Pair 0; devices 2 and 3 (S2 and S3) form Memory Device Pair 1. Refer to the block diagram for device connections.
- Card address bits range from A0 to A19. Host address bits range from A0 to A20. Host address bit A0 is used for controlling the $\overline{CE_L}$ and $\overline{CE_H}$ inputs to the card. Refer to Figure 2 for host-to-card address bit connections.

AMD FLASH MEMORY PROGRAM AND ERASE OPERATIONS

To simplify program and erase operations, AMD Flash Memory devices include Embedded Algorithms (Embedded Erase Algorithm and Embedded Program Algorithm) that allow the host to simply issue a command, after which it is free to perform other tasks. The host then only needs to monitor appropriate status bits to determine when the operation is complete.

Embedded Erase Algorithm

When erasing a sector or device, the Embedded Erase algorithm does not require the host to first entirely pre-program the device. Upon executing the Embedded Erase command sequence, the addressed memory sector or memory device automatically writes and verifies the entire memory device or memory sector for an all "0" data pattern. The system is not required to provide any controls or timing during these operations.

When the memory sector or memory device is automatically verified to contain an all "0" pattern, a self-timed chip erase-and-verify begins. The erase and verify operations are complete when the data on D7 (D15 on the odd byte) of the memory sector or memory device is "1" (see Write Operation Status section), at which time the device returns to the read mode. The system is not required to provide any control or timing during these operations. If a Reset command is issued while the erase operation is in progress, the erase operation will stop, and the data in that device will be undefined. In that case, restart the erase on that sector and allow it to complete.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required).

The Embedded Erase command sequence is a command only operation that stages the memory sector or memory device for automatic electrical erasure of all bytes in the array. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on D7 (D15 on the odd byte) of the memory sector or memory device is "1" (see Write Operation Status section) at which time the device returns to the Read mode. Please note that for the memory device or memory sector erase operation, $\overline{Data}$ Polling may be performed at any address in that device or sector.

Figure 4 and Table 9 illustrate the Embedded Erase Algorithm, a typical command string and bus operations.

As described earlier, once the memory sector in a device or memory device completes the Embedded Erase operation, it returns to the Read mode and addresses are no longer latched. Therefore, the device requires that a valid address input to the device is

supplied by the system at this particular instant of time. Otherwise, the system will never read a "1" on D7 (D15 on the odd byte). A system designer has the following choices to implement the Embedded Erase algorithm:

1. The host may keep the sector address (within any of the sectors being erased) valid during the entire Embedded Erase operation.
2. Once the system executes the Embedded Erase command sequence, the host may remove the address from the device and perform other tasks. The host is required to keep track of the valid sector address by loading it into a temporary register. When the host comes back to $\overline{Data}$ Poll the device, it must reassert the same address.
3. The host may monitor $\overline{BUSY}$ (RY/ $\overline{BY}$) to determine the status of the Embedded Algorithm in progress. A "0" indicates that the device is busy; a "1" indicates that the algorithm is complete.

Since the Embedded Erase operation takes a significant amount of time (typical 1 s), option 2 makes more sense. However, the choice of these three options has been left to the system designer.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$), whichever occurs later, while the data is latched on the rising edge of $\overline{WE}$ (or $\overline{CE}$) pulse, whichever occurs first. A time-out of 80 μ s from the rising edge of the last sector erase command will initiate the sector erase command.

Multiple sectors can be specified for erase by writing the six bus cycle operation as described above and then following it by additional writes of the Sector Erase command to addresses of other sectors to be erased. The time between Sector Erase command writes must be less than 80 μ s, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 μ s from the rising edge of the last $\overline{WE}$ (or $\overline{CE}$) will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ (or $\overline{CE}$) occurs within the 80 μ s time-out window, the timer is reset. During the 80 μ s window, any command other than Sector Erase or Erase Suspend written to the device will reset the device back to Read mode. Once the 80 μ s window has timed out, only the Erase suspend command is recognized. Note that although the Reset command is not recognized in the Erase Suspend mode, the device is available for read or program operations in sectors that

are not erase suspended. The Erase Suspended and Erase Resume commands may be written as often as required during a sector erase operation. Hence, once erase has begun, it must ultimately complete unless Hardware Reset is initiated. Loading the sector erase registers may be done in any sequence and with any number of sectors (0 to 15).

A Reset command issued after the device has begun execution stops the erase operation, but the data in the sector will be undefined. In that case, restart the erase on that sector and allow it to complete.

The automatic sector erase begins after the 80 μ s time out from the rising edge of the $\overline{WE}$ (or $\overline{CE}$) pulse for the last sector erase command pulse and terminates when the data on D7 is "1" (see Write Operation Status section) at which time the device returns to read mode. $\overline{Data}$ Polling must be performed at an address within any of the sectors being erased.

If $\overline{Data}$ Polling or the Toggle Bit indicates the device has been written with a valid Sector Erase command, D3 may be used to determine if the sector erase timer

window is still open. If D3 is high ('1'), the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by the $\overline{Data}$ Polling or Toggle Bit. If D3 is low ('0'), the device will accept additional sector erase commands. To be certain the command has been accepted, the software should check the status of D3 following each Sector Erase command. If D3 was high on the second status check, the command may not have been accepted.

It is recommended that the user guarantee the time between sector erase command writes be less than 80 μ s by disabling the processor interrupts just for the duration of the Sector Erase (30H) commands. This approach will ensure that sequential sector erase command writes will be written to the device while the sector erase timer window is still open.

Figure 4 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Table 9. Embedded Erase Algorithm

Bus Operation	Command	Comments
Standby		Wait for V_{CC} ramp
Write	Embedded Erase command sequence	6 bus cycle operation
Read		$\overline{Data}$ Poll or check $\overline{BUSY}$ (RY/BY) to verify erasure

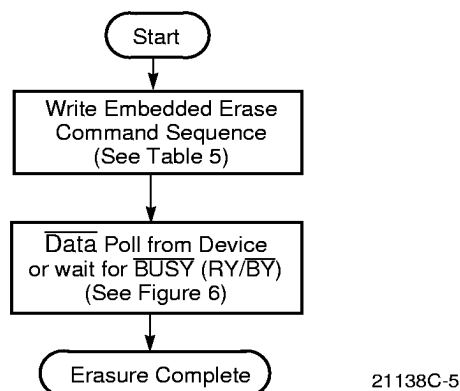


Figure 4. Embedded Erase Algorithm

Note: The latest release of the software drivers for AMD Miniature Cards and devices may be downloaded from the AMD web site at <http://www.amd.com>.

Embedded Program Algorithm

The Embedded Program setup is a four bus cycle operation that stages the addressed memory location or memory device for automatic programming.

Once the Embedded Program setup operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ (or $\overline{CE}$) pulse.

Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further control or timing. The device will automatically provide an adequate internally generated write pulse and verify margin. The automatic programming operation is completed when the data on D7 of the addressed memory sector or memory device is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the Read mode (no write verify command is required).

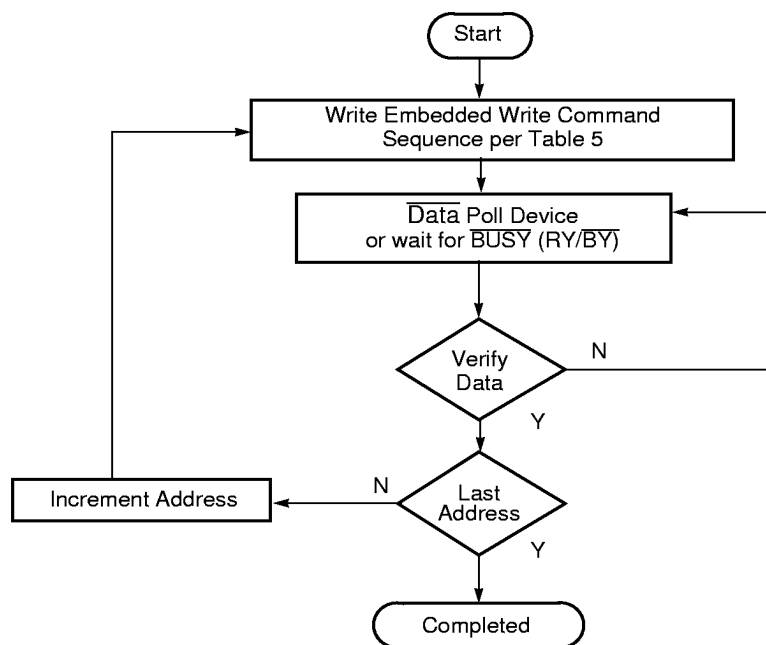
Addresses are latched on the falling edge of $\overline{WE}$ (or $\overline{OE}$) during the Embedded Program command execution and hence the system is not required to keep the addresses stable during the entire Programming operation. However, once the device completes the Embedded Program operation, it returns to the Read mode and addresses are no longer latched. Since a verify valid data must occur on D7, at this particular instant, the system is required to supply a valid address input to the device. A system designer has three choices to implement the Embedded Programming algorithm:

1. The system (CPU) keeps the address valid during the entire Embedded Programming operation, or
2. Once the system executes the Embedded Programming command sequence, the CPU takes away the address from the device and becomes free to do other tasks. In this case, the CPU is required to keep track of the valid address by loading it into a temporary register. When the CPU comes back for performing Data Polling, it should reassert the same address.
3. The host may monitor $\overline{BUSY}$ (RY/ $\overline{BY}$) to determine the status of the Embedded Algorithm in progress. A "0" indicates that the device is busy; a "1" indicates that the algorithm is complete.

However, since the Embedded Programming operation takes only 9 μ s typically, it may be easier for the CPU to keep the address stable during the entire Embedded Programming operation instead of reasserting the valid address during Data Polling. Any commands written to the device during this period will be ignored. Figure 5 and Table 10 illustrate the Embedded Program Algorithm, a typical command string, and bus operation.

Table 10. Embedded Program Algorithm

Bus Operation	Command	Comments
Standby		Wait for V_{CC} ramp
Write	Embedded Program command sequence	3 bus cycle operation
Write	Program Address/Data	1 bus cycle operation
Read		Data Poll or check $\overline{BUSY}$ (RY/ $\overline{BY}$) to verify program



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Figure 5. Embedded Program Algorithm

Reset Command

The device will automatically power up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Characteristics section for the specific timing parameters.

The reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

Sector Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data read or programs in a sector not being erased. This command is applicable **only** during the Sector Erase operation, which includes the time-out period for Sector Erase. The Erase Suspend command will be ignored if written during the execution of the Chip Erase operation or Embedded Program Algorithm (but will reset the chip if written improperly during the command sequences.) Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation. Once in Erase Suspend, the device is available for read (note that in the Erase Suspend mode, the

Reset/Read command is not required for read operations and is ignored) or program operations in sectors not being erased. Any other command written during the Erase Suspend mode will be ignored, except for the Erase Resume command. Writing the Erase Resume command resumes the sector erase operation. The addresses are “don’t cares” when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 μ s and 20 μ s to actually suspend the operation and go into erase suspended read mode (pseudo-read mode), at which time the user can read or program from a sector that is **not** erase suspended. Reading data in this mode is the same as reading from the standard read mode, except that the data must be read from sectors that have not been erase suspended.

Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause D2 to toggle. Polling D2 on successive reads from a given sector provides the system the ability to determine if a sector is in Erase Suspend.

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase suspend-program mode. Again, programming in this mode is the same as programming in the regular Byte Program mode, except that the data

must be programmed to sectors that are not erase suspended. Successively reading from the erase suspended sector while the device is in the erase suspend-program mode will cause D2 to toggle. Completion of the erase suspend operation can be determined two ways:

- Checking the status of the toggle bit D2
- Checking the status of the RY/ $\overline{\text{BY}}$ pin

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. However, another Erase Suspend command can be written after the device has resumed sector erase operations.

Write Operation Status

Table 11 shows the status bit states for device program and erase operations.

Data Polling—D7 (D15 on Odd Byte)

The Miniature card features $\overline{\text{DATA}}$ Polling as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During the Embedded Program Algorithm, an attempt to read the device will produce the compliment of the data last written to D7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to D7. Note that just at the instant when D7 switches to true data, the other bits, D6–D0, may not yet be true data. However, they will all be true data on the next read from the device. **Please note that Data Polling (D7) may give an inaccurate result when an attempt is made to write to a protected sector.** During an Embedded Erase Algorithm, an attempt to read the device will produce a '0' at the D7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce a '1' at D7.

Table 11. Hardware Sequence Flags

Status			D7	D6	D5	D3	D2
In Progress	Byte Program in Embedded Program Algorithm		$\overline{\text{D7}}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle (Note 1)
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{\text{D7}}$	Toggle (Note 2)	0	1	1 (Note 3)
Exceeded Time Limits	Byte Program in Embedded Program Algorithm		$\overline{\text{D7}}$	Toggle	1	0	1
	Program/Erase in Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{\text{D7}}$	Toggle	1	1	N/A

Notes:

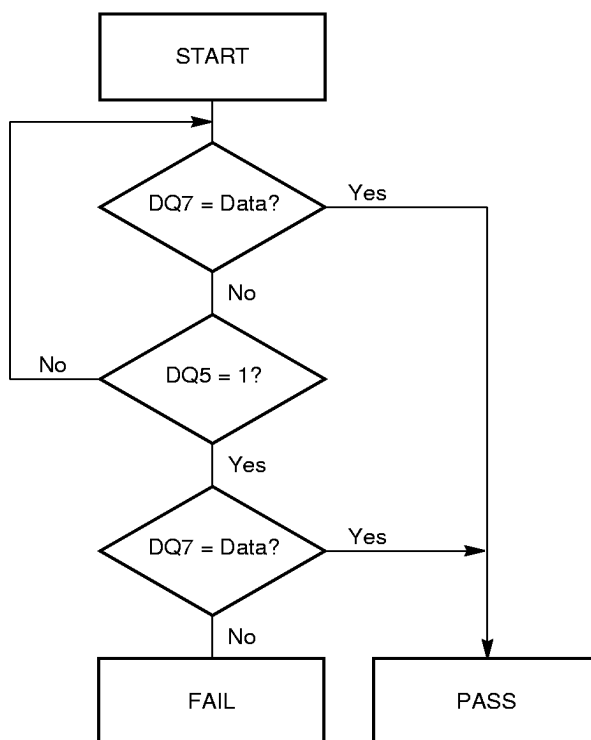
1. Performing successive read operations from the erase-suspended sector will cause D2 to toggle.
2. Performing successive read operations from any address will cause D6 to toggle.
3. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the D2 bit. However, successive reads from the erase-suspended sector will cause D2 to toggle.

BUSY (RY/ $\overline{\text{BY}}$ —Ready/Busy)

The $\overline{\text{BUSY}}$ signal indicates to the host the status of operations within the Miniature Card. The $\overline{\text{BUSY}}$ signal is tied to the components' RY/ $\overline{\text{BY}}$ pins.

The RY/ $\overline{\text{BY}}$ signal from AMD Flash devices in the Miniature Card indicate that the Embedded Algorithms are either in progress or have been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the

device is ready to accept any read/write or erase operation. When the RY/ $\overline{\text{BY}}$ pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If a Flash device is placed in an Erase Suspend mode, the RY/ $\overline{\text{BY}}$ output will be high. Refer to the section "Sector Erase Suspend" for more information.



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Note: D7 is rechecked even if D5 = 1 because D7 may change simultaneously with D5.

Figure 6. Data Polling Algorithm

WORD-WIDE PROGRAMMING

The Word-Wide Programming sequence will be as usual per Table 5. The Program word command is A0A0H. Each byte is independently programmed. For example, if the high byte of the word indicates the successful completion of programming via one of its write status bits such as D15, software polling should continue to monitor the low byte for write completion and data verification, or vice versa. During the Embedded Programming operations the device executes programming pulses in 9 μ s increments.

WORD-WIDE SECTOR ERASING

The Word-Wide Sector Erasing of a memory device pair is similar to word-wide programming. The erase word command is a six-bus-cycle command sequence (see Table 5). Each sector is independently erased and verified. Word-wide erasure reduces total erase time when compared to byte erasure. Each Flash memory device in the card may erase at different rates. Therefore, each device (byte) must be verified separately.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -30°C to $+70^{\circ}\text{C}$
Ambient Temperature
with Power Applied. -10°C to $+70^{\circ}\text{C}$
Voltage at All Pins (Note 1) -0.5 V to $V_{\text{CC}}+0.5\text{ V}$
 V_{CC} (Note 1) -0.5 V to 3.6 V
Output Short Circuit Current (Note 2) 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V . During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20 ns . Maximum DC voltage on output and I/O pins is $V_{\text{CC}} + 0.5\text{ V}$. During voltage transitions, outputs may overshoot to $V_{\text{CC}} + 2.0\text{ V}$ for periods up to 20 ns .
2. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal $V_{\text{OUT}} = 0.5\text{ V}$ or 3.6 V , $V_{\text{CC}} = V_{\text{CCmax}}$. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.
3. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Case Temperature (T_{C}) 0°C to $+70^{\circ}\text{C}$
 V_{CC} Supply Voltages. $+2.7\text{ V}$ to $+3.6\text{ V}$

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC\ max}$		± 5	μA
I_{LO}	Output Leakage Current	$V_{IN} = V_{SS}$ to V_{CC} , $V_{CC} = V_{CC\ max}$		± 5	μA
I_{CCS}	V_{CC} Standby Current	$\overline{CE_L}$, $\overline{CE_H}$, $\overline{RESET} = V_{IH}$ $V_{CC} = 3.6V$; $V_{IN} = V_{SS}$ or V_{CC}	2 Mbyte	100	μA
			4 Mbyte	220	μA
I_{CC}	V_{CC} Supply Current, word mode (Note 2)	$\overline{RESET} = V_{IH}$; $\overline{CE_L}$ and $\overline{CE_H} = V_{IL}$	Read	32	mA
			Write	60	mA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		$0.7 V_{CC}$	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OUT} = 5.8\ mA$		0.45	V
V_{OH}	Output High Voltage	$I_{OUT} = -2.0\ mA$	$0.85 V_{CC}$		V
V_{LKO}	Low V_{CC} Lock-Out Voltage		2.3	2.5	V

Notes:

- $V_{CC} = 2.7\ V$ to $3.6\ V$.
- Supply current is a max RMS value. Read frequency = 5 MHz.

CONNECTOR DC SPECIFICATIONS

Parameter	Min	Max	Units
Interface Signal Resistance (Note 2)		2.0	Ω
Interface Signal Current (Notes 1, 2)	125		mA
Power/Insertion Signal Resistance		0.060	Ω
Power/Insertion Signal Current (Note 1)	500		mA

Notes:

- This current is a minimum that the connector should withstand, and a maximum that the host should provide.
- On the host, these specifications must be met for one conducting channel on elastomeric connectors.

CARD AND PAD CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Max	Unit
C_{CARD}	Card Input Capacitance		40	pF
C_{HOST}	System Load Capacitance		120	pF
$C_{I/O}$	I/O Capacitance D0-D15		40	pF

Notes:

- Sampled, not 100% tested.
- Test conditions $T_A = 25^\circ C$, $f = 1.0\ MHz$.

AC CHARACTERISTICS

Read-only Operations

			Card Speed		
Parameter Symbol		Parameter Description	150 ns		Unit
JEDEC	Standard		Min	Max	
t _{AVAV}	t _{RC}	Read Cycle Time	150		ns
t _{ELQV}	t _{CE}	Chip Enable Access Time		150	ns
t _{AVQV}	t _{ACC}	Address Access Time		150	ns
t _{GLQV}	t _{OE}	Output Enable Access Time		50	ns
t _{ELQX}	t _{LZ}	Chip Enable to Output in Low-Z	5		ns
t _{EHQZ}	t _{DF}	Chip Disable to Output in High-Z		30	ns
t _{GLQX}	t _{OLZ}	Output Enable to Output in Low-Z	5		ns
t _{GHQZ}	t _{DF}	Output Disable to Output in High-Z		30	ns
t _{AXQX}	t _{OH}	Output Hold from First of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
	t _{Ready}	RESET Pin Low to Read Mode		20	μs

AC CHARACTERISTICS

Write Operations (Erase/Program)

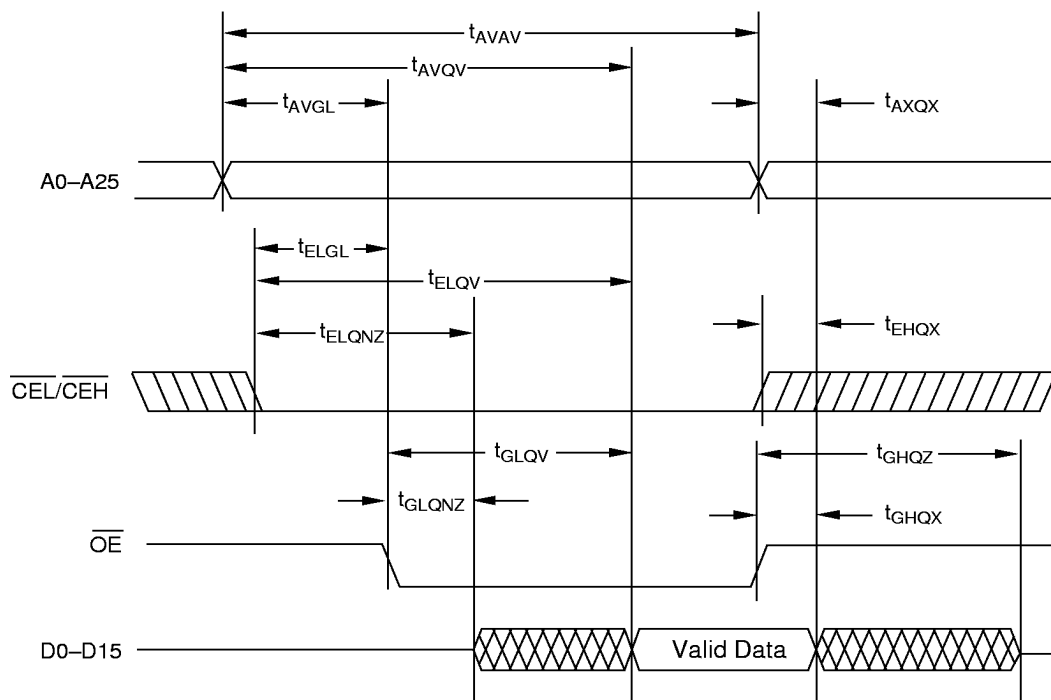
			Card Speed			
Parameter Symbols		Parameter Description	150 ns			Unit
JEDEC	Standard		Min	Typ	Max	
t _{AVAV}	t _{RC}	Read Cycle Time	150			ns
t _{ELQV}	t _{CE}	Chip Enable Access Time			150	ns
t _{AVQV}	t _{ACC}	Address Access Time			150	ns
t _{GLQV}	t _{OE}	Output Enable Access Time			50	ns
t _{ELQX}	t _{LZ}	Chip Enable to Output in Low-Z	5			ns
t _{EHQZ}	t _{DF}	Chip Disable to Output in High-Z			30	ns
t _{GLQX}	t _{OLZ}	Output Enable to Output in Low-Z	5			ns
t _{GHQZ}	t _{DF}	Output Disable to Output in High-Z			30	ns
t _{AXQX}	t _{OH}	Output Hold From First of Address, $\overline{CE}$, or $\overline{OE}$ Change	0			ns
t _{WHGL}		Write Recovery Time Before Read	0			μs
t _{GLQNZ}		Data Output enable time from $\overline{OE}$ active	0			ns
t _{ELQNZ}		Data Output enable time from $\overline{CE}$ active	0			ns
t _{WLWH}		$\overline{WE}$ pulse width	50			ns
t _{ELGL} t _{ELWL}		$\overline{CE}$ setup time to $\overline{WE}$ or $\overline{OE}$ active	0			ns
t _{AVGL} t _{AVWL}		Address setup time to $\overline{WE}$ or $\overline{OE}$ active	0			ns
t _{DVWH}		Data setup time to $\overline{WE}$ inactive	50			ns
t _{WHDX}		Data hold time from $\overline{WE}$ inactive	0			ns
t _{WHAX}		Address hold time from $\overline{WE}$ inactive	0			ns
t _{WHEH}		$\overline{CE}$ hold time from $\overline{WE}$ inactive	0			ns
	t _{RP}	$\overline{RESET}$ Pulse Width	500			ns
	t _{BUSY}	Program/Erase Valid to RY/ $\overline{BY}$ Delay	90			ns
t _{WHWH1}		Programming Operation		9	300	μs
t _{WHWH2}		Sector Erase Operation		1.5	15	s

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



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Figure 7. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

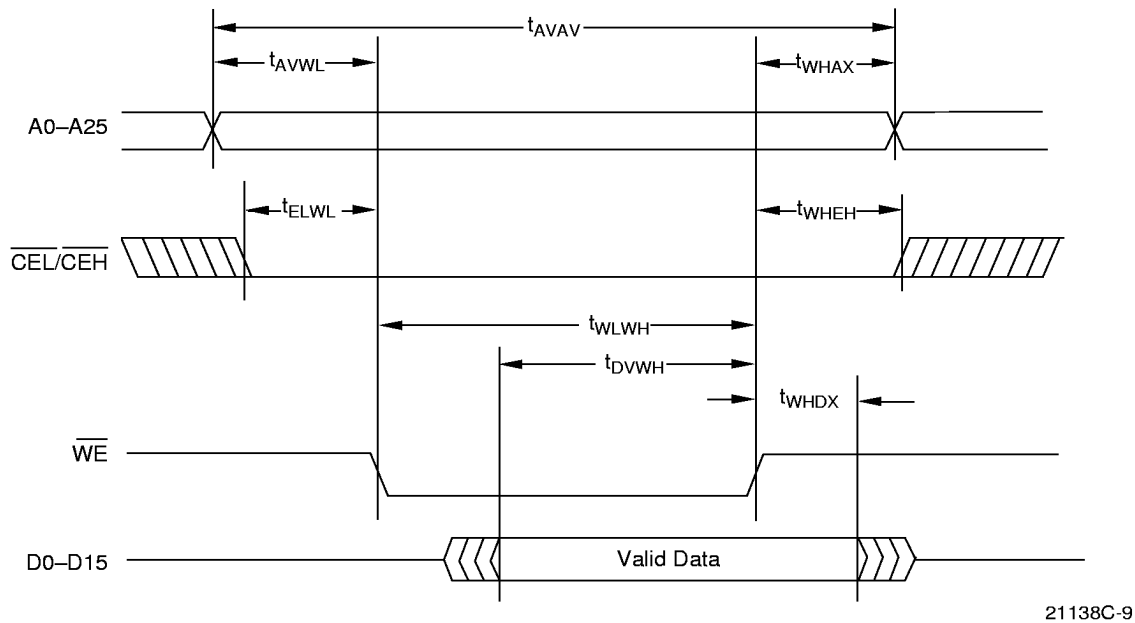
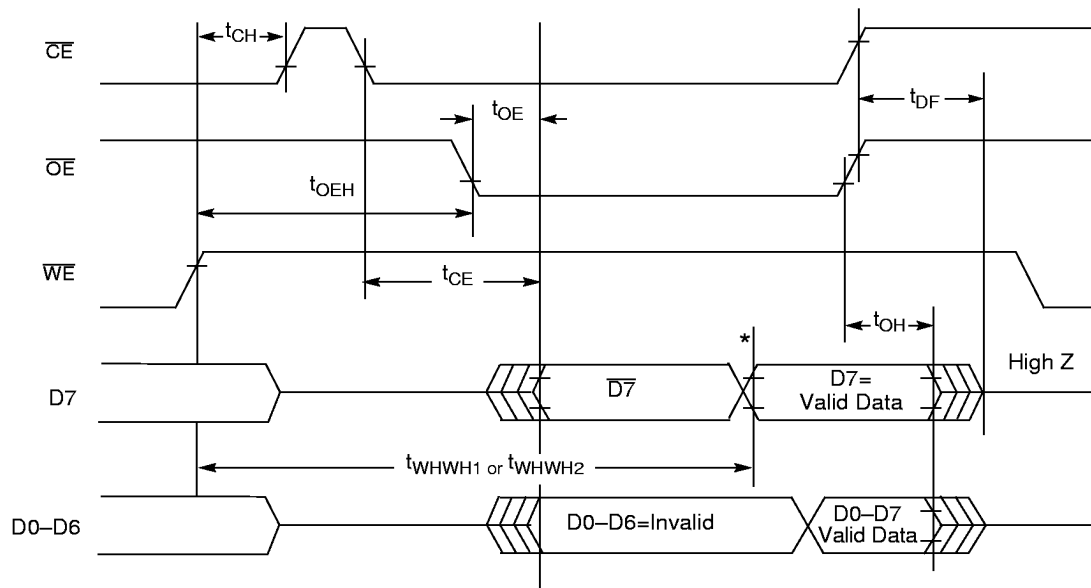


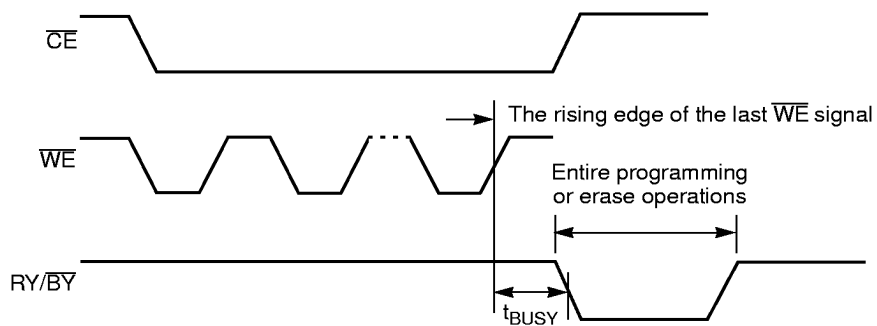
Figure 8. AC Waveforms for Write Operations



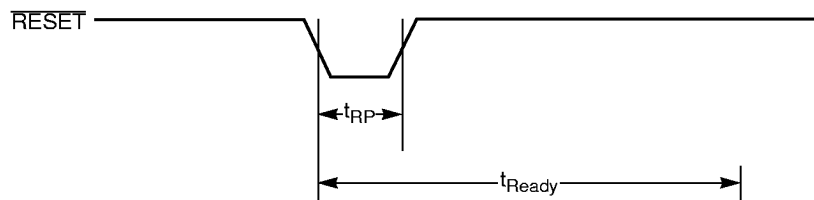
*D7=Valid Data (The device has completed the Embedded operation).

Figure 9. AC Waveforms for Data Polling During Embedded Algorithm Operations

SWITCHING WAVEFORMS



21138C-11

Figure 10. $RY/\overline{BY}$ Timing Diagram During Program/Erase Operations

21138C-12

Figure 11. $\overline{RESET}$ Timing Diagram

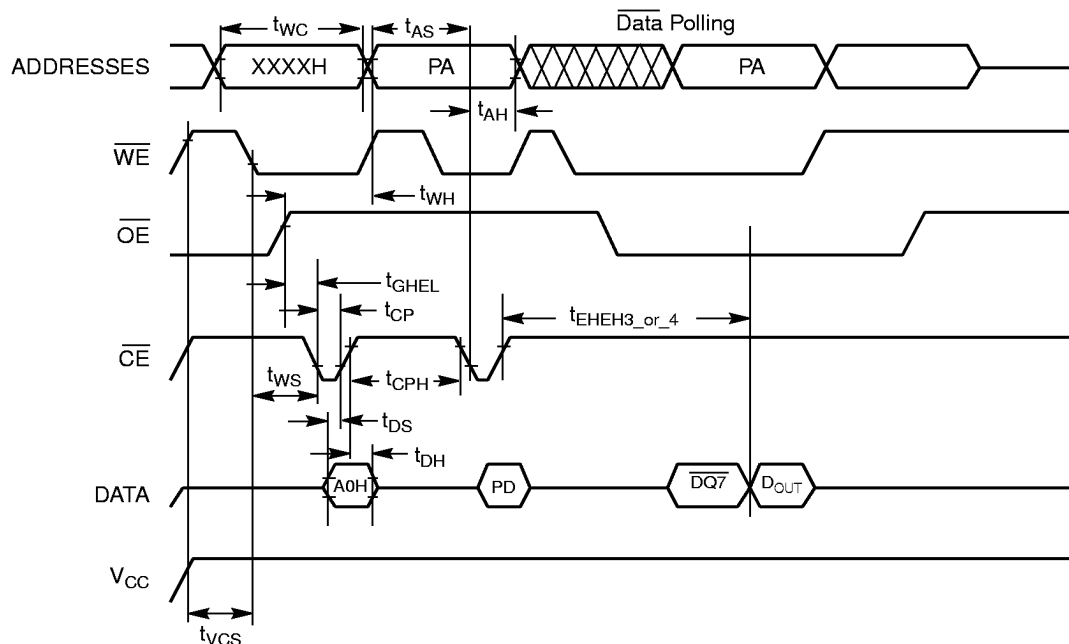
AC CHARACTERISTICS-ALTERNATE $\overline{CE}$ CONTROLLED WRITES

Write/Erase/Program Operations

			Card Speed			
Parameter Symbols		Parameter Description	150 ns			Unit
JEDEC	Standard		Min	Typical	Max	
tAVAV	tWC	Write Cycle Time	150			ns
tAVEL	tAS	Address Setup Time	10			ns
tELAX	tAH	Address Hold Time	50			ns
tDVEH	tDS	Data Setup Time	50			ns
tEHDX	tDH	Data Hold Time	0			ns
tGLDV	tOEHL	Output Enable Hold Time for Embedded Algorithm	10			ns
tGHEL		Read Recovery Time before Write	0			μs
tWLEL	tWS	WE Setup Time before CE	0			ns
tEHWL	tWH	WE Hold Time	0			ns
tELEH	tCP	CE Pulse Width	50			ns
tEHEL	tCPH	CE Pulse Width HIGH (Note 3)	20			ns
tEHEH3		Embedded Programming Operation (Notes 3,4)		9	300	μs
tEHEH4		Embedded Erase Operation for each 64K byte Memory Sector (Notes 1, 2)		1.5	15	s
tVCS		VCC Setup Time to Write Enable LOW	50			μs

Notes:

1. Rise/fall time ≤ 10 ns.
2. Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exceed the device specification.
3. Card Enable Controlled Programming:
Flash Programming is controlled by the valid combination of the Card Enable ($\overline{CE1}$, $\overline{CE2}$) and Write Enable ($\overline{WE}$) signals. For systems that use the Card Enable signal(s) to define the write pulse width, all setup, hold, and inactive write enable timing should be measured relative to the Card Enable signal(s).
4. Under worst case condition of 90°C, $V_{CC} = 2.7$ V, 100,000 cycles. Excludes system level overhead, the time required to execute the four bus cycle command necessary to program each byte.

**Notes:**

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. These waveforms are for the x16 mode.

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Figure 12. Alternate $\overline{CE}$ Controlled Write Operation Timings

AIS MEMORY MAP

The AIS (Attribute Information Structure) is an area of memory used for storing information about the configuration of the Miniature Card. The AIS is recommended to be stored in the first sector of the first device of the Flash array. As this area is not explicitly protected, the AIS information must be reloaded onto the card in the event that the information is erased.

The AIS has five unique information areas:

1. Identification Data: This data includes Manufacturer information (Manufacturer and card name).
2. Compatibility Data: This data specifies basic information about the card (memory size, access time, memory type, power, etc.)
3. Burst Data (not applicable)
4. DRAM Data (not applicable)
5. Reserved Data: This data area is reserved for future use.

The AIS supports up to four different memory technologies on a card. Some of the information areas are repeated in the memory map in order to specify different technologies (see Table 12). The Technology Count field in the Identification Data section defines the number of different technologies on a card. The first memory technology is defined in the AIS memory map from address 40H through 7FH. The second memory technology is defined from 80H through BFH. The third memory technology is defined from C0H to DFH. The fourth memory technology is defined from E0H to FFH.

The AIS is stored as bytes within the 16-bit Miniature Card data word. The even byte D0–D7 stores the AIS data, and the odd byte D8–D15 is reserved by the card manufacturer for manufacturing information.

Table 12. Miniature Card AIS Memory Assignments

Card Address	Section	Description
00H–0FH	PC Card Compatibility Area*	Reserved for PC Card Tuples
10H–1FH	Identification Data Identifies Card Type	
20H–2FH	Identification Data Identifies Card Type	
30H–3FH	Identification Data Identifies Card Type	
40H–4FH	Compatibility Data (Area 1)	Memory Technology #1
50H–5FH	Burst Data (not applicable)	
60H–6FH	DRAM Data (not applicable)	
70H–7FH	Reserved for future use	
80H–8FH	Compatibility Data (not applicable)	(Memory Technology #2)
90H–9FH	Burst Data (not applicable)	
A0H–AFH	DRAM Data (not applicable)	
B0H–BFH	Reserved for future use	
C0H–CFH	Compatibility Data (not applicable)	(Memory Technology #3)
D0H–DFH	Reserved for future use	
E0H–EFH	Compatibility Data (not applicable)	(Memory Technology #4)
F0H–FFH	Reserved for future use	

* For more information on PC Card Compatibility refer to table 13 or the Miniature Card PC Compatibility Guide.

Note: "Not applicable" indicates the address space does not apply to AMD Flash Miniature Cards, but is defined by MCIF.

Table 13. PC Card Compatibility Memory Assignments

Address	Values	Description
00h	01h	TPL_CODE CISTPL_DEVICE
01h	03h	TPL_LINK
02h	53	Device ID
03h	2MB (5V)=7C, 4MB=FC (5V); 8MB (5V) = 1E	Device Size
04h	FF	End of CISTPL_DEVICE
05h	1Ch	TPL_CODE CISTPL_DEVICE_OC
06h	03h	TPL_LINK
07h	53h	Device ID
08h	2MB (3V) = 7C; 4MB (3V) = FC	Device Size
09h	FFh	End of CISTPL_DEVICE_OC
0Ah	00h	CISTPL_NULL
0Bh	00h	CISTPL_NULL
0Ch	00h	CISTPL_NULL
0Dh	00h	CISTPL_NULL
0Eh	80h	TPL_CODE CISTPL_MINI
0Fh	F0h	TPL_LINK

Identification Data

The identification data provides basic identification information about the card. This data section is required on all cards. Table 14 shows the Identification Data for AMD's 3 volt-only Miniature cards.

Compatibility Data

The compatibility data provides basic compatibility across all cards. This data section is required on all cards. The addresses in parentheses are specified for cards with more than one memory technology on the card. Table 15 shows the compatibility data for AMD 3-volt only Miniature Cards

Table 14. AMD Identification Data

Card Address	Value	Description
10H	99H	Miniature Card Identifier: Fixed value for a host to identify an inserted Miniature Card
11H	11H	Level of Compliance: Defines the level of AIS supported. The Miniature Cards described in this document are rev 1.1 compliant.
12H	78H or 76H	AIS Checksum: The modulo-256 sum of all even bytes from 10H–FFH. A valid checksum sums to 00H (2's complement). 2 MByte card: 88H + 78H = 00H 4 MByte card: 8AH + 76H = 00H
13H	41H	Manufacturer Name: 13H–26H. String of ASCII characters at addresses 13H to 26H to identify the manufacturer of the Miniature Card. ASCII character "A"
14H	4DH	ASCII character "M"
15H	44H	ASCII character "D"
16H	20H	ASCII character - SPACE
17H	49H	ASCII character - "I"
18H	4EH	ASCII character - "N"
19H	43H	ASCII character - "C"
1AH	00H	ASCII character - NULL
1BH	00H	ASCII character - NULL
1CH–26H	00H	Unused space in manufacturer name field
27H	33H	Card Name: (addresses 27H–3AH). String of ASCII characters to identify the card name. ASCII character "3"
28H	56H	ASCII character "V"
29H	4DH	ASCII character "M"
2AH	43H	ASCII character "C"
2BH	20H	ASCII character - SPACE
2CH	53H	ASCII character "S"
2DH	65H	ASCII character "e"
2EH	72H	ASCII character "r"
2FH	69H	ASCII character "i"
30H	65H	ASCII character "e"
31H	73H	ASCII character "s"

Table 14. AMD Identification Data (Continued)

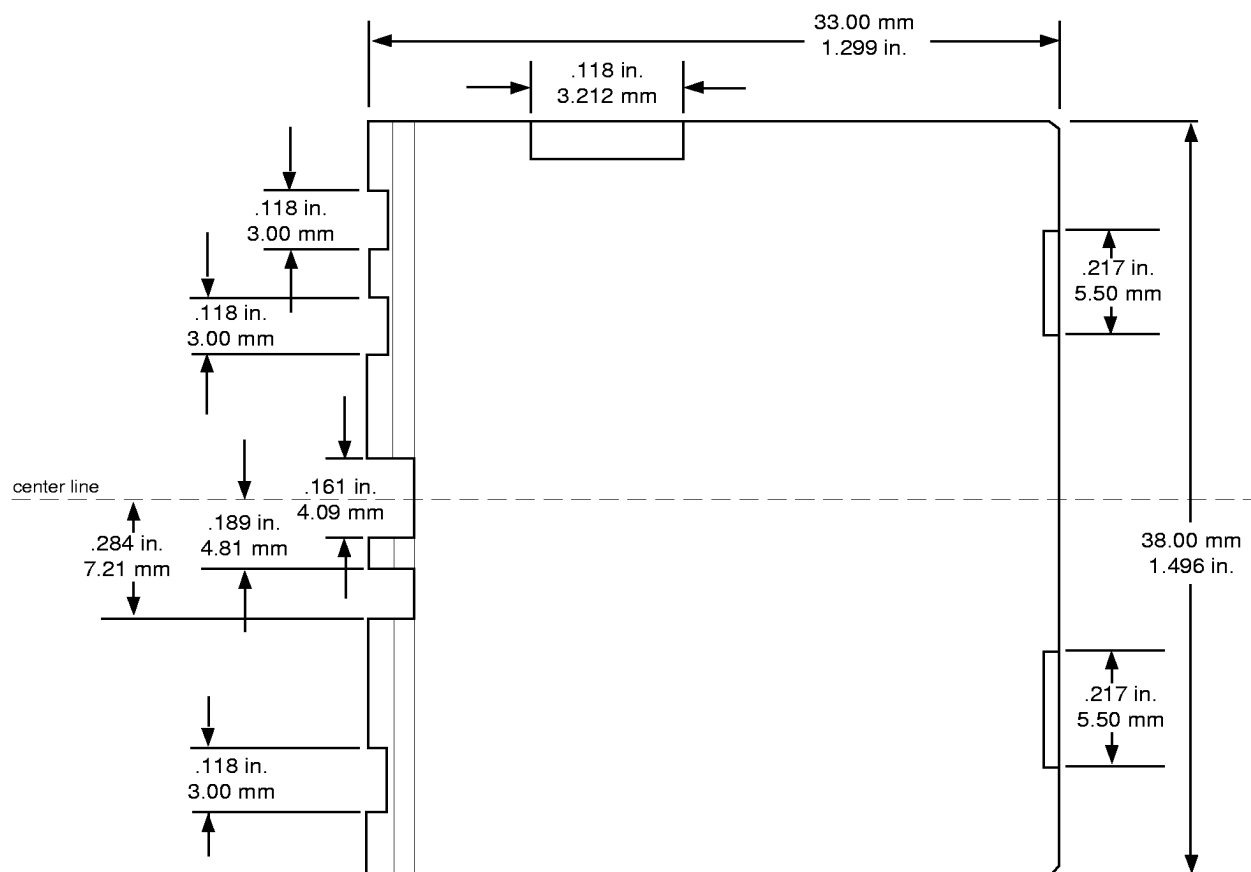
Card Address	Value	Description
32H	00H	ASCII character - NULL
33H–3AH	00H	Unused space in card name field
3BH	01H	Technology Count: Defines the number of different memory technologies on the Miniature Card. Technology count set to 1
3CH–3FH	00H	Reserved space set to 00H; for future use

Table 15. AMD Compatibility Data

Card Address	Value	Description
40H	00H	Defines the type of memory technology; Flash = 000 Binary
41H	01H	Device JEDEC Manufacturer ID
42H	38H	Device JEDEC Component ID: Am29LV081 = 38H
43H	01H or 03H	Memory array size: 02 = 2 MByte, 04 = 4 MByte
44H	00H	N/A
45H	0FH	3.3V access time: 150 ns
46H	00H	N/A
47H	00H	N/A
48H	24H	Typical read/write current at 3.3V: 20 mA read, 40 mA write (word mode)
49H	00H	N/A
4AH	00H	Typical card standby current: 10 μ A for 2 MByte, 40 μ A for 4 MByte
4BH–4FH, 8CH–8FH, CCH–CFH, ECH–EFH	00H	Reserved for future use
80H–8BH, C0–CBH, E0H–EBH	00H	These addresses are designated for other memory technologies, which are not used in AMD Flash Miniature Cards.

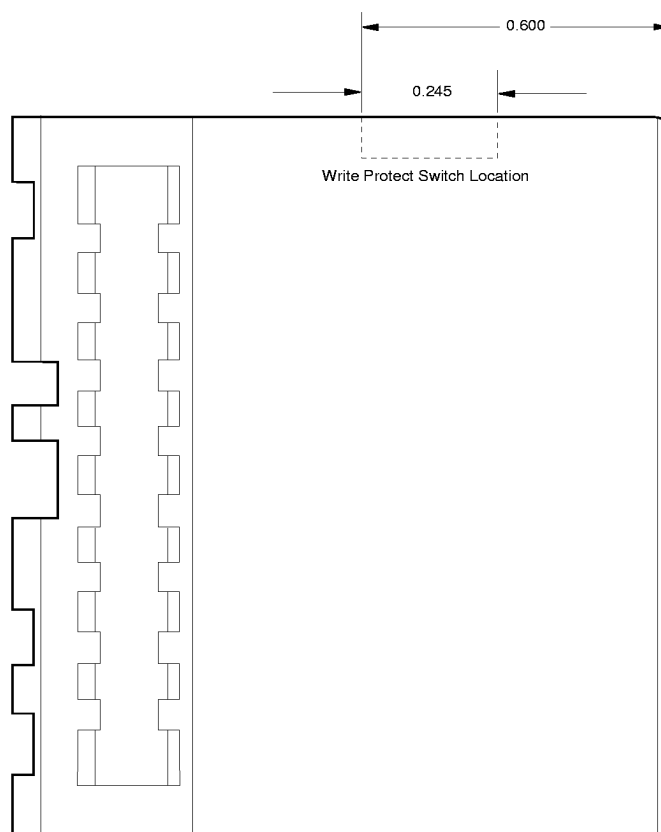
Note:

All reserved bytes must be set to 00H. All reserved fields (bits) within bytes must be set to 0BH. All unused fields must be set to 00H.

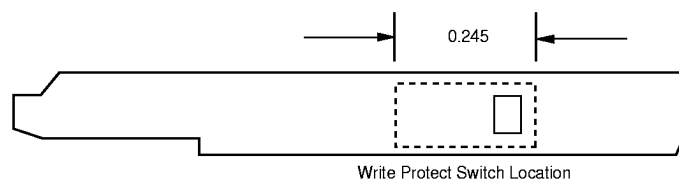


PHYSICAL DIMENSIONS

Bottom View



Right Side View



REVISION HISTORY

General Description

Reworded first paragraph.

Block Diagram

Updated.

Pad Assignments

VS1: this signal is grounded.

Reset: Added text regarding 20 μ s delay.

WE: Inserted reference to $\overline{CE}$.

Erase Operations

Removed third paragraph.

Table 5, Word Command Definitions

Added note on Autoselect, fifth cycle.

Tables 6 and 7, Byte Command Definitions

Added note on Autoselect, fifth cycle.

Embedded Erase Algorithm

Paragraph 4: Removed last sentence

Added D15 references with D7 references.

Sector Erase

Added in D3 paragraphs.

Word-Wide Programming

Clarified section.

Absolute Maximum Ratings

Changed 5.0 V to 3.6 V in Note 2

DC Characteristics

Revised table.

Added read frequency in Note 2 of DC Characteristics table.

AC Characteristics

Removed table containing t_{RCB} and t_{FCB}

Revised Read-only Operations Table.

Removed asterisk note on t_{READY}

Switching Waveforms

Changed t_{BUSY} time from 50ns to 90ns

AC Characteristics—Alternate $\overline{CE}$ Controlled Writes

Added typical specifications.

Revised parameters in table.

Table 13, PC Card Compatibility Memory Assignments

Added table.

Table 14, AMD Identification Data and Table 15, AMD Compatibility Data

Corrected parameters in AIS

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