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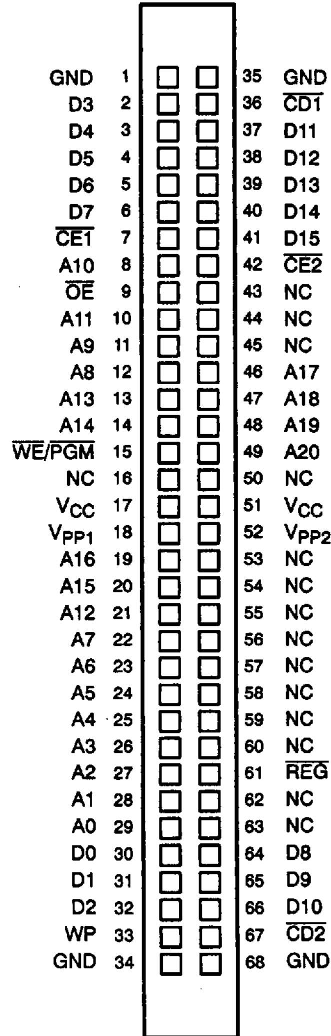
TEXAS INSTR (ASIC/MEMORY)

CMS68F256, CMS68F512, CMS68F1MB, CMS68F2MB FLASH MEMORY CARDS

T-81-27-90

- **Industry Standard PCMCIA Cards**
- **Standard Card Size (85,6 mm × 54,0 mm × 3,3 mm)**
- **Single 5-V Power Supply (± 5% Tolerance)**
- **Utilize TSOP-I (Thin Small Outline Package-Type I) Flash Memory Devices**
- **68-Pin PCMCIA (Rev. 2.0) / JEIDA (Rev. 4.0) Compatible**
- **8-Bit or 16-Bit User Configurable Organization**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 55°C**
- **Standard 68-Pin Two-Piece Connector**
- **All Input/Output Signals Fully TTL Compatible**
- **3-State Output**

68-PIN MEMORY CARD† (CONNECTOR VIEW)



† Pinout shown is for maximum density card. See pin assignment table for specifics.

NC – No internal connection

description

The CMS68Fxxx series are TI standard memory cards designed to be used either as an internal memory system or as external add-on memory according to PCMCIA/JEIDA industry standard card specifications. These cards are offered with a memory size from 256K bytes to 2048K bytes of Flash memory devices and the card organization (× 8 or × 16) is directly user configurable.

The cards are comprised of 2, 4, or 8 1M-byte or 2M-byte Flash memory devices in 32-lead plastic Thin Small Outline Packages (TSOP-I).

available organizations

PART NUMBER	ORGANIZATION	ACCESS TIME	TOTAL DENSITY	CONNECTOR
CMS68F256-250	256K × 8 / 128K × 16	250 ns	256K-Bytes	Two-piece, 68 pin
CMS68F512-250	512K × 8 / 256K × 16	250 ns	512K-Bytes	Two-piece, 68 pin
CMS68F1MB-250	1M × 8 / 512K × 16	250 ns	1M-Bytes	Two-piece, 68 pin
CMS68F2MB-250	2M × 8 / 1M-Byte × 16	250 ns	2M-Bytes	Two-piece, 68 pin

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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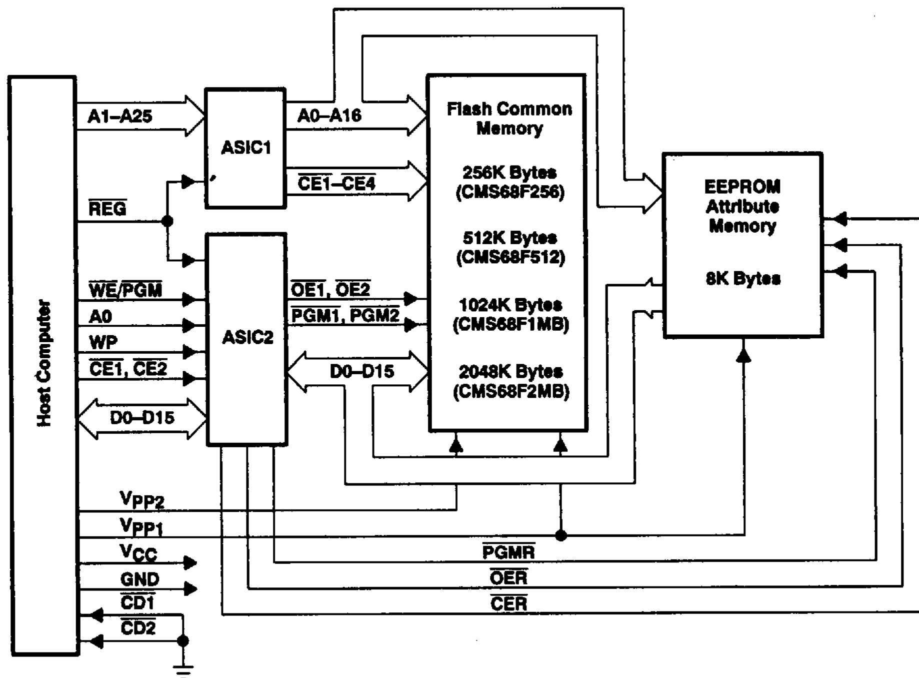
pin assignments

CMS68F256
CMS68F512
CMS68F1MB
CMS68F2MB

'68F256	'68F512	'68F1MB	'68F2MB	PIN #	PIN #	'68F2MB	'68F1MB	'68F512	'68F256
GND	GND	GND	GND	1	35	GND	GND	GND	GND
D3	D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	D4	3	37	D11	D11	D11	D11
D5	D5	D5	D5	4	38	D12	D12	D12	D12
D6	D6	D6	D6	5	39	D13	D13	D13	D13
D7	D7	D7	D7	6	40	D14	D14	D14	D14
$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	7	41	D15	D15	D15	D15
A10	A10	A10	A10	8	42	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC	NC
A11	A11	A11	A11	10	44	NC	NC	NC	NC
A9	A9	A9	A9	11	45	NC	NC	NC	NC
A8	A8	A8	A8	12	46	A17	A17	A17	A17
A13	A13	A13	A13	13	47	A18	A18	A18	NC
A14	A14	A14	A14	14	48	A19	A19	NC	NC
$\overline{WE}$/PGM	$\overline{WE}$/PGM	$\overline{WE}$/PGM	$\overline{WE}$/PGM	15	49	A20	NC	NC	NC
NC	NC	NC	NC	16	50	NC	NC	NC	NC
V_{CC}	V_{CC}	V_{CC}	V_{CC}	17	51	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{PP1}	V_{PP1}	V_{PP1}	V_{PP1}	18	52	V_{PP2}	V_{PP2}	V_{PP2}	V_{PP2}
A16	A16	A16	A16	19	53	NC	NC	NC	NC
A15	A15	A15	A15	20	54	NC	NC	NC	NC
A12	A12	A12	A12	21	55	NC	NC	NC	NC
A7	A7	A7	A7	22	56	NC	NC	NC	NC
A6	A6	A6	A6	23	57	NC	NC	NC	NC
A5	A5	A5	A5	24	58	NC	NC	NC	NC
A4	A4	A4	A4	25	59	NC	NC	NC	NC
A3	A3	A3	A3	26	60	NC	NC	NC	NC
A2	A2	A2	A2	27	61	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$
A1	A1	A1	A1	28	62	NC	NC	NC	NC
A0	A0	A0	A0	29	63	NC	NC	NC	NC
D0	D0	D0	D0	30	64	D8	D8	D8	D8
D1	D1	D1	D1	31	65	D9	D9	D9	D9
D2	D2	D2	D2	32	66	D10	D10	D10	D10
WP	WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	GND	34	68	GND	GND	GND	GND

functional block diagram



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operation

There are seven modes of operation for the CMS68Fxxx described in the table below. The read mode requires a single 5-V supply.

operation table

FUNCTIONAL MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$ / PGM	V_{PP2}	V_{PP1}	D15–D8	D7–D0
Standby	X	H	H	X	X	X	V_{CC}	V_{CC}	HI-Z	HI-Z
Read (x8)	H H	H H	L L	L H	L L	H H	V_{CC} V_{CC}	V_{CC} V_{CC}	HI-Z HI-Z	EV-BY OD-BY
Read (x16)	H	L	L	X	L	H	V_{CC}	V_{CC}	OD-BY	EV-BY
OD-BY Read	H	L	H	X	L	H	V_{CC}	V_{CC}	OD-BY	HI-Z
Write (x8)	H H	H H	L L	L H	H H	L L	V_{CC} V_{PP}	V_{PP} V_{CC}	XXX XXX	EV-BY OD-BY
Write (x16)	H	L	L	X	H	L	V_{PP}	V_{PP}	OD-BY	EV-BY
OD-BY Write	H	L	H	X	H	L	V_{PP}	V_{CC}	OD-BY	XXX

attribute memory read function

FUNCTIONAL MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$ / PGM	V_{PP2}	V_{PP1}	D15–D8	D7–D0
Standby Mode	X	H	H	X	X	X	V_{CC}	V_{CC}	HI-Z	HI-Z
Byte access (8 bits)	L L	H H	L L	L H	L L	H H	V_{CC} V_{CC}	V_{CC} V_{CC}	HI-Z HI-Z	EV-BY Not Valid
Byte access (16 bits)	L	L	L	X	L	H	V_{CC}	V_{CC}	Not Valid	EV-BY
Odd-byte-only access	L	L	H	X	L	H	V_{CC}	V_{CC}	Not Valid	HI-Z

EV-BY = Even Byte
OD-BY = Odd Byte
HI-Z = High Impedance
X = V_{IL} or V_{IH}
H = High
L = Low

pin description

SYMBOL	FUNCTION
A0–A20	Address input lines, driven by the host, which enable direct addressing of up to 2 megabytes of memory. Signal A0 is not used in word access mode. Signal A20 is the most significant bit.
D0–D15	Bidirectional data bus The most significant bit is D15. Bit number and significance decrease downward to D0.
$\overline{CE1}$, $\overline{CE2}$	Active-low card enable signals driven by the host; $\overline{CE1}$ is used to enable even bytes, $\overline{CE2}$ for odd bytes. A multiplexing scheme based on A0, $\overline{CE1}$, $\overline{CE2}$ allows 8-bit hosts to access all data on D0–D7 if desired.
$\overline{OE}$	Active-low signal, driven by the host, which is used to gate memory read data from the memory card.
$\overline{WE/PGM}$	Programming enable signal
V_{PP1}	Programming voltage 1
V_{PP2}	Programming voltage 2
$\overline{CD1}$, $\overline{CD2}$	Card detect signals for proper memory card insertion detection. The signals are connected to ground internally on the memory card.
WP	Status signal of Write Protect switch on the memory card.
$\overline{REG}$	When active, access to the memory card is limited to Attribute Memory used to record capacity and other configuration and attribute information.
V_{CC}	Power supply
GND	Ground
NC	No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	– 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	– 0.5 to 14 V
Input voltage range, (see Note 1)	– 0.5 to 6.5 V
Output voltage range, (see Note 1)	– 0.5 to V_{CC}
Operating free-air temperature range	– 0°C to 55°C
Storage temperature range	– 20°C to 65°C
Connector insertion cycles	10 000

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{PPH}	Supply voltage		11.4		12.6	V
V_{PPL}	Supply voltage	Read Mode	0		6.5	V
V_{IH}	High-level input voltage	TTL	2.4		V_{CC} + 0.3	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.5	
V_{IL}	Low-level input voltage	TTL	– 0.5		0.8	V
		CMOS	– 0.5		GND + 0.2	
T_A	Operating free-air temperature		0		55	°C

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage (except WP)		I_{OH} = 12 mA, V_I = 0.9 V_{CC}	3.7		V
			I_{OH} = 1.2 mA, V_I = 0.9 V_{CC}	4.4		
V_{OL}	Low-level output voltage (except CD1, CD2)		I_{OL} = 12 mA, V_I = 0.1 V_{CC}		0.5	V
			I_{OL} = 1.2 mA, V_I = 0.1 V_{CC}		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.25 V		±10	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±10	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.25 V		80	mA
I_{PP2}	V_{PP} write current		V_{PP} = V_{PPH}, Write in progress		60	mA
I_{PP3}	V_{PP} write verify current		V_{PP} = V_{PPH}, Erasure in progress		12	µA
I_{PP4}	V_{PP} erase verify current		V_{PP} = V_{PPH}, Erasure verify in progress		12	mA
I_{PP5}	V_{PP} leakage current		V_{PP} ≤ V_{CC}		±80	µA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{CEx}$ = V_{IH}, V_{CC} = 5.25 V		25	mA
		CMOS-input level	$\overline{CEx}$ = V_{CC} ± 0.2 V, V_{CC} = 5.25 V		20	
I_{CC2}	V_{CC} supply current (active, output open)		$\overline{CEx}$ = V_{IL}; V_{CC} = 5.25 V, I_{OUT} = 0 mA, f = 6 MHz		80	mA

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capacitance over recommended ranges of supply voltage and free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz			8	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz			16	pF

† Capacitance measurements are made on sample basis only.
‡ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics for read-only operations for attribute memory over recommended ranges of supply voltage and operating free-air temperature (see Notes 2 and 3)

PARAMETER		TEST CONDITIONS (SEE NOTES 2 & 3)	MIN	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		200	ns
$t_{a(E)}$	Access time ROM chip enable			200	ns
$t_{en(G)}$	Output enable time from $\overline{OE}$			100	ns
t_{dis}	Output disable time from $\overline{OE}$ or $\overline{CEx}$, whichever occurs first¶		0	60	ns
$t_{v(A)}$	Output data valid time after change of address $\overline{CEx}$ or $\overline{OE}$ whichever occurs first		0		ns

¶ Value calculated from 0.5-V delta to measured output level.

NOTES: 2. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference input/output wave forms for timing parameters).
3. Common test conditions apply for t_{dis} except during programming.

timing requirements for read-only operations over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER	CHARACTERISTICS	MIN	MAX	UNIT
t_{avav} / t_{rc}	Read cycle time	250		ns
t_{elqv} / t_{ce}	Chip enable access time		250	ns
t_{avqv} / t_{acc}	Address access time		250	ns
t_{glqv} / t_{oe}	Output enable access time		120	ns
t_{elox} / t_{lz}	Chip enable to output in low-Z	5		ns
t_{ehqz}	Chip disable to output in high-Z		60	ns
t_{glqx} / t_{olz}	Output enable to output in low-Z	5		ns
t_{ghqz} / t_{df}	Output disable to output in high-Z		60	ns
t_{oh}	Output hold from address $\overline{CE}$ or $\overline{OE}$ change (see Note 5)	5		ns
t_{whgl}	Write recovery time before read	6		µs

NOTES: 4. Rise/fall time ≤ 10 ns.
5. Read timing parameters during read/write operations are the same as during read-only operations.

timing requirements for write/erase operations over recommended ranges of supply voltage and operating free-air temperature (see Notes 4 and 5)

PARAMETER	CHARACTERISTICS	MIN	MAX	UNIT
t_{avav} / t_{wc}	Write cycle time	250		ns
t_{avwl} / t_{as}	Address setup time	0		ns
t_{wlax} / t_{ah}	Address hold time	100		ns
t_{dvwh} / t_{ds}	Data setup time	80		ns
t_{whdx} / t_{dh}	Data hold time	30		ns
t_{whgl}	Write recovery time before read	6		µs
t_{ghwl}	Read recovery time before read	0		µs
t_{wloz}	Output high-Z from write enable	5		ns
t_{whox}	Output low-Z from write enable		60	ns
t_{elwl} / t_{cs}	Chip enable setup time before write	40		ns
t_{wheh} / t_{ch}	Chip enable hold time	0		ns
t_{wlwh} / t_{wp}	Write pulse duration	100		ns
t_{whwl} / t_{wph}	Write pulse duration high	20		ns
t_{whwh1}	Duration of write operation (see Note 6)	10		µs
t_{whwh2}	Duration of erase operation (see Note 6)	9.5		ms
t_{vpel}	Vpp setup time to chip enable low	100		ns

NOTES: 4. Rise/fall time ≤ 10 ns.
5. Read timing parameters during read/write operations are the same as during read-only operations. Refer to timing requirements for Read Operations.
6. The integrated stop timer terminates the write/erase operations, thereby eliminating the need for a maximum specification.

alternative $\overline{CE}$-controlled writes over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	CHARACTERISTICS	MIN	MAX	UNIT
t_{avav}	Write cycle time	250		ns
t_{avel}	Address setup time	0		ns
t_{elax}	Address hold time	100		ns
t_{dveh}	Data setup time	80		ns
t_{ehdx}	Data hold time	30		ns
t_{ehgl}	Write recovery time before read	6		µs
t_{ghel}	Read recovery time before read	0		µs
t_{wlel}	Write enable setup time before chip-enable	0		ns
t_{ehwh}	Write enable hold time	0		ns
t_{eleh}	Write pulse duration (see Note 7)	100		ns
t_{ehel}	Write pulse duration high	20		ns
t_{pel}	Vpp setup time to chip enable low	100		ns

NOTE 7: Chip Enable Controlled Writes: Write operations are driven by the valid condition of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse duration (with a longer Write Enable timing waveform) all set-up, hold, and inactive Write Enable times should be measured relative to the Chip Enable waveform.

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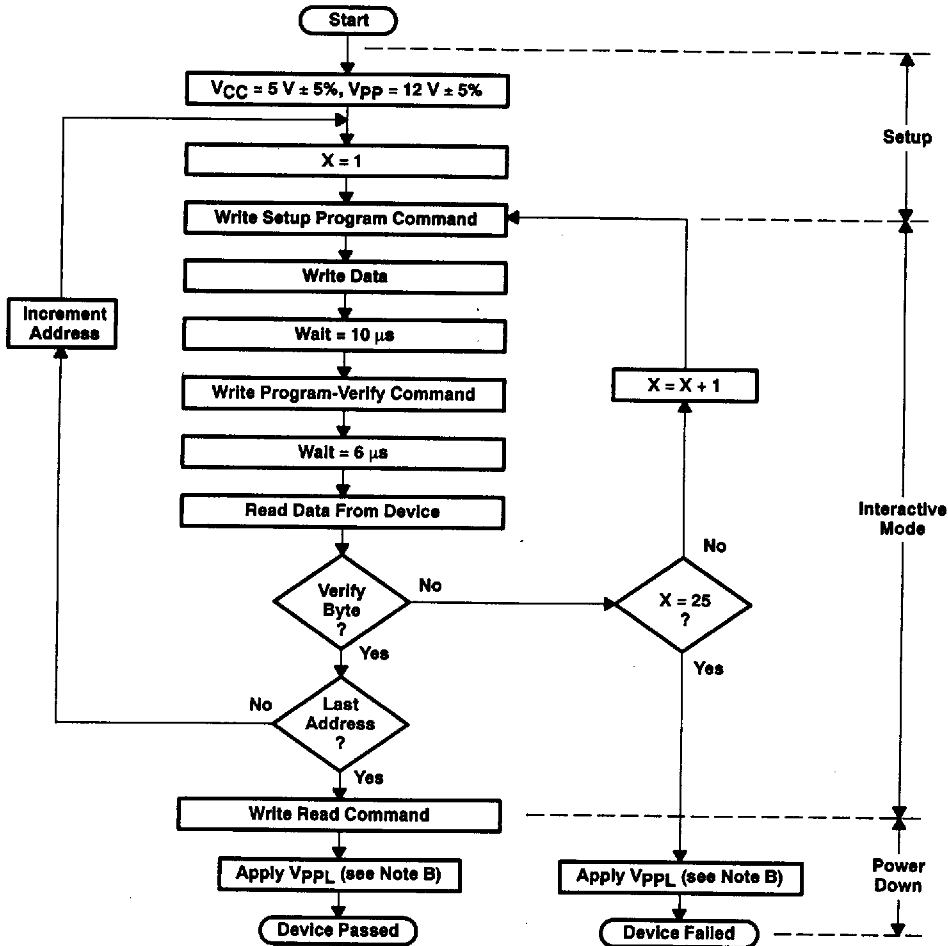
programming flowchart: write algorithm for byte-wide mode



BUS OPERATION	COMMAND	COMMENTS
Initialize Address Standby		Wait for V_{PP} ramp to V_{PPH} (see Note A) Initialize Pulse Count
Write	Setup Program	Data = 40h
Write	Write-Data	Valid Address Data
Standby		Wait = 10 µs
Write	Program Verify	Data = C0h; Ends Program Operation
Standby		Wait = 5 µs
Read		Read Byte to Verify Programming; Compare Output to Expected Output
Write	Read	Data = 00h; Register Reset for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

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flash-erase flowchart: erase algorithm for byte-wide mode

Start
All Bytes = 00h ?
No → Program All Bytes to 00h
Yes
Address = 00000h Odd = 0
V_{CC} = 5 V ± 5%, V_{PP} = 12 V ± 5%
X = 1
Write Setup Erase Program
Write Write-Erase Command
Wait = 10 ms
Write Erase-Verify Command
Wait = 6 µs
Read Data From Device
Verify Byte = FFh ?
No → X = 3000 ?
X = 3000 ? No → X = X + 1 → Write Setup Erase Program
X = 3000 ? Yes → Apply V_{PPL} (see Note B) → Device Failed
Verify Byte = FFh ? Yes → Last Address ?
Last Address ? No → Increment Address + 2 → Write Erase-Verify Command
Last Address ? Yes → Odd = 1 ?
Odd = 1 ? No → Odd = 1 Address = 00001h → X = 1
Odd = 1 ? Yes → Write Read Command
Apply V_{PPL} (see Note B)
Device Erased

Pre-Program
Setup
Interactive Mode
Power Down

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

flash-erase flowchart: erase algorithm for byte-wide mode (continued)

BUS OPERATION	COMMAND	COMMENTS
		Entire Memory Must = 00h Before Erasure Use Fastwrite Programming Algorithm
		Initialize Addresses
Standby		Wait = V_{PP} Ramp to V_{PPH} (see Note A)
		Initialize Pulse Count
Write	Setup Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 9.5 ms
Write	Erase Verify	Address = Byte to Verify; Data = A0h; Ends the Erase Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Erasure; Compare Output to FFh
Write	Read	Data = 00h; Register Reset for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

programming flowchart: write algorithm for word-wide mode

Start

V_{CC} = 5 V ± 5%, V_{PP} = 12 V ± 5%

Get Address, Get Write-Data

Val-Data = Write-Data
Counter-L = 0
Counter-H = 0
Flag = 0
W-Com = 4040h
C-Com = C0C0h

Write Setup
Program Command

Write Data

Time Out = 10 μs

Write Program-Verify Command

Time Out = 6 μs

Read Address/Flash-Data

Flash-Data = Val-Data ? (No → Flag = 0 ?; Yes → More Data ?)

Flag = 0 ? (Yes → Write Verify and Mask Subroutine → Write Setup Program Command; No → Write Read Command)

Write Verify
and
Mask Subroutine

More Data ? (Yes → Get Address, Get Write-Data; No → Write Read Command)

Write Read Command

Apply V_{PPL}

Device Passed

Write Read Command

Apply V_{PPL}

Device Failed

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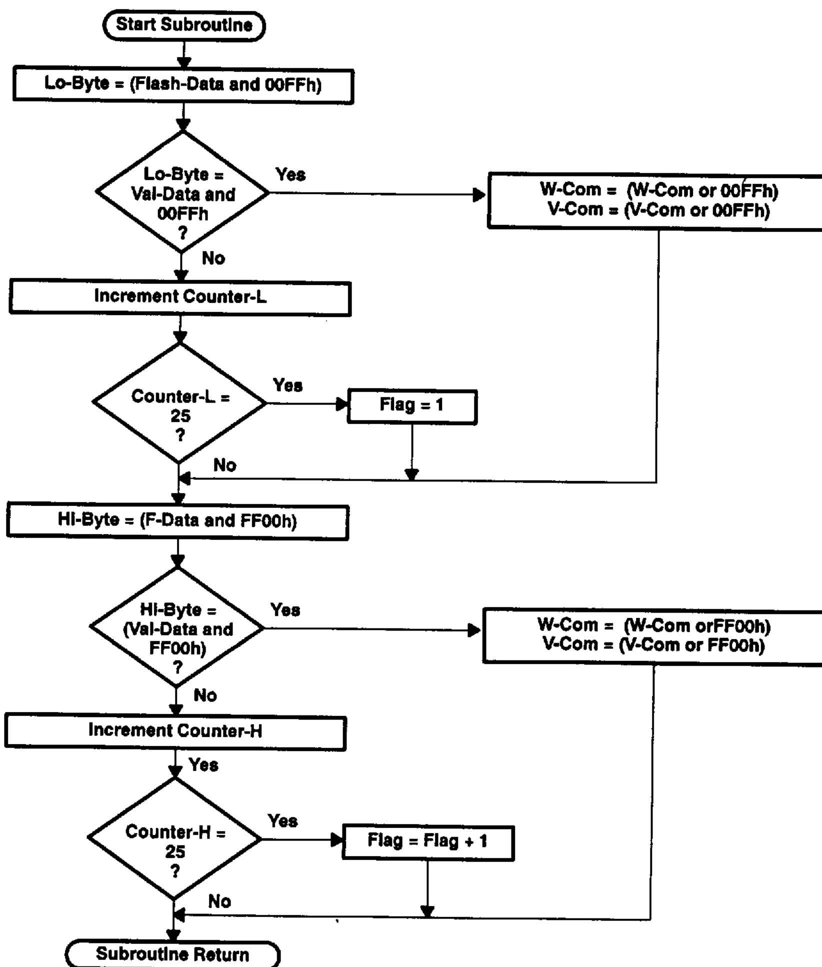
write verify and mask subroutine for read-write mode



BUS OPERATION	COMMAND	COMMENTS
Write	Setup Program	Data = W-Com
Write	Write-Data	Valid Address Data (Write-Data)
Write	Program-Verify	Data = C-Com; Ends Programs Operations

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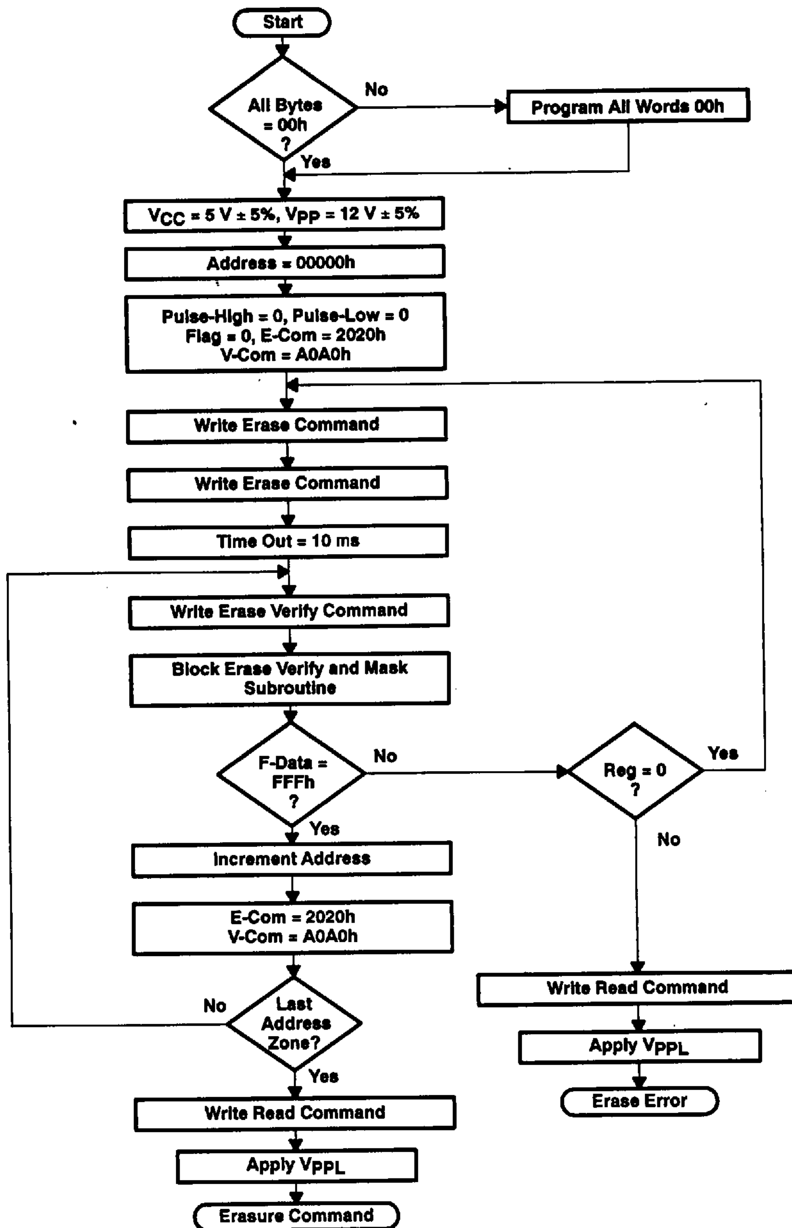
erase algorithm for word-wide mode



BUS OPERATION	COMMAND	COMMENTS
Write	Erase	Data = 2020h
Write	Erase-Verify	Data = A0A0h

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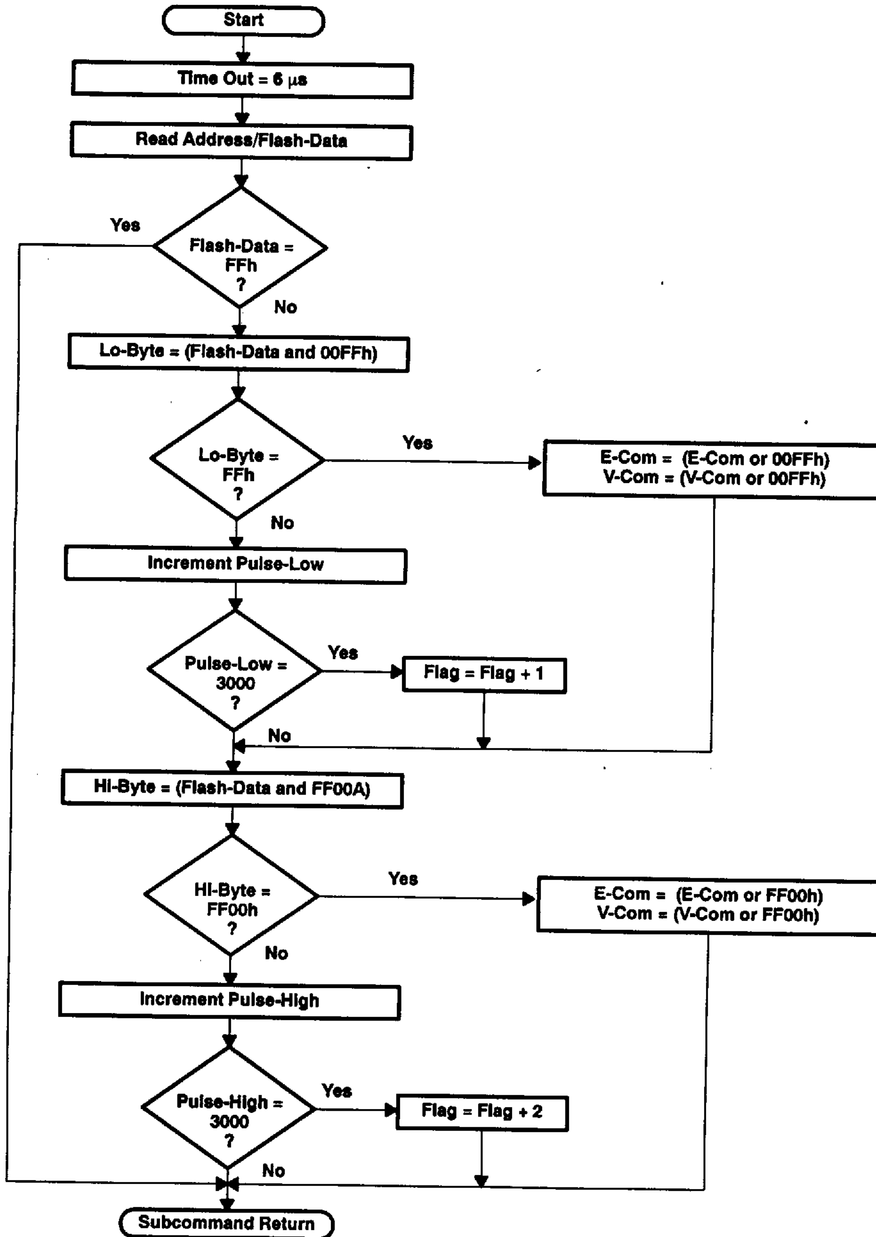
block erase verify and mask subroutine



PARAMETER MEASUREMENT INFORMATION

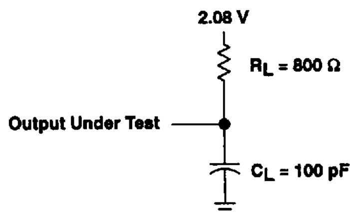
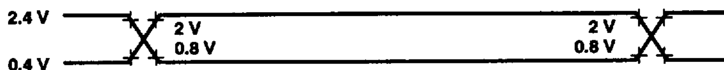


Figure 1. Load Circuit for Timing Parameters

Input/output wave forms for timing parameters



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

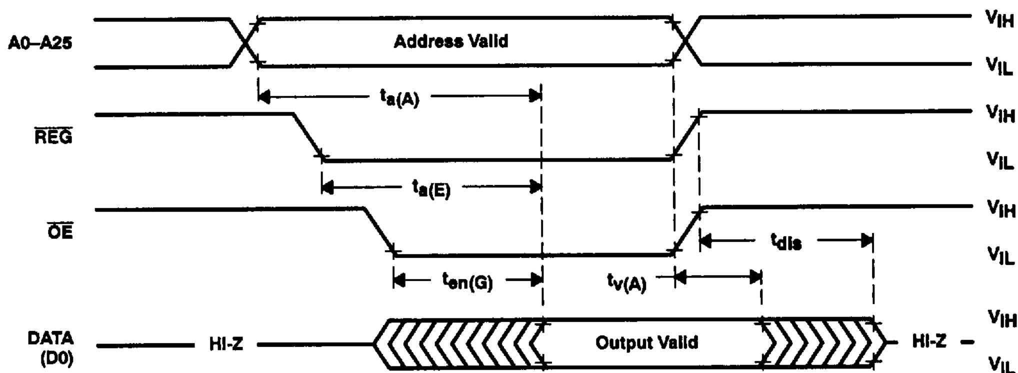
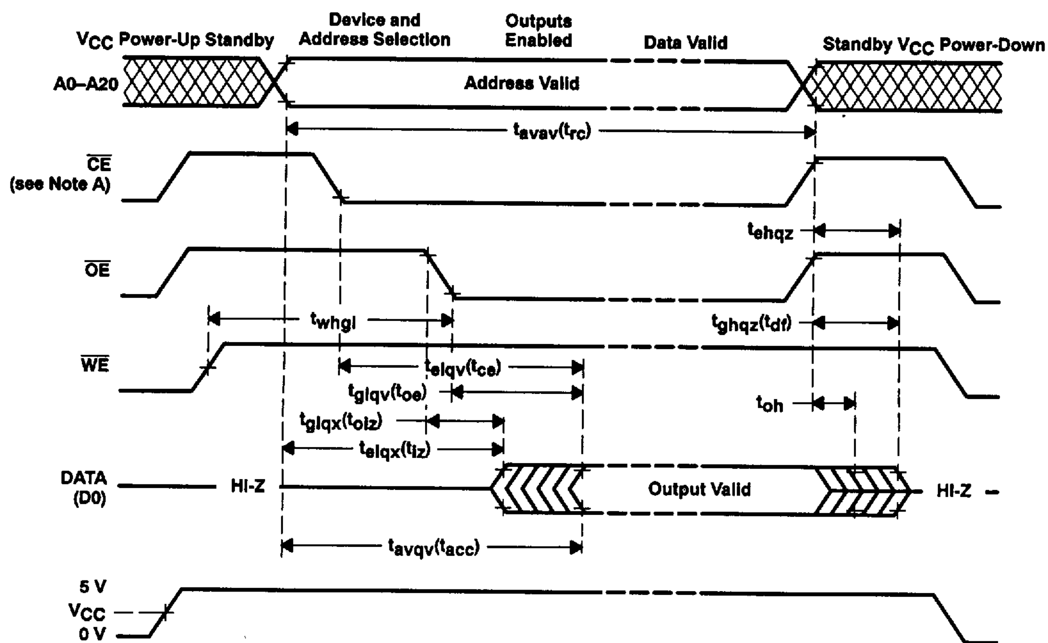


Figure 2. Attribute Memory Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.

Figure 3. Read Operations Timing

PARAMETER MEASUREMENT INFORMATION

NOTE A: $\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.

Figure 4. Write Operations Timing

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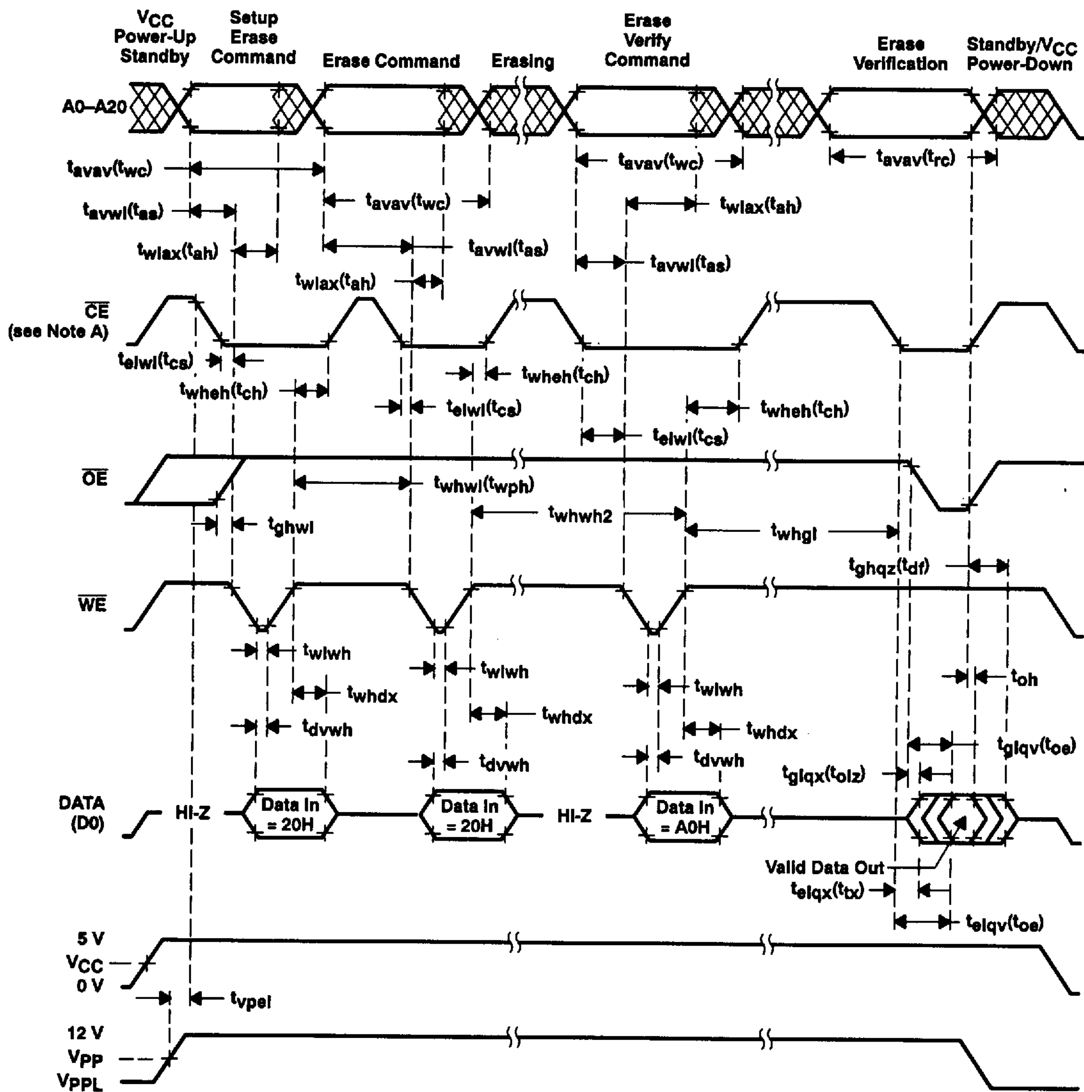
TEXAS INSTR (ASIC/MEMORY)

PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.

Figure 5. Erase Operations Timing

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

Vcc Power-Up Standby
Setup Program Command
Program Command Latch Address and Data
Programming
Program Verify Command
Program Verification
Standby/Vcc Power-Down

A0–A20

$\overline{CE}$ (see Note A)

$\overline{OE}$

$\overline{WE}$

DATA (D0)
Hi-Z
Data In = 40H
Data In
Data In = C0H
Valid Data Out

5 V
V_{CC}
0 V

12 V
V_{PP}
V_{PPL}

NOTE A: $\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.

Figure 6. Write Operations Timing