CS-117/117R

2, 4 or 6-Channel Winchester Read/Write Circuit with Control and Data Protect Functions

Description

The CS-117 is a monolithic Read/Write IC designed for use in Winchester disk drive magnetic memory systems. The circuit interfaces with up to six heads to provide the necessary R/W functions, as well as control and data protect functions. LSTTL interfaces are used for the Write Data, Head Select, R/$\overline{W}$ Select, Write Unsafe, and Chip Select circuits. Write current is generated internally as a function of an external resistor.

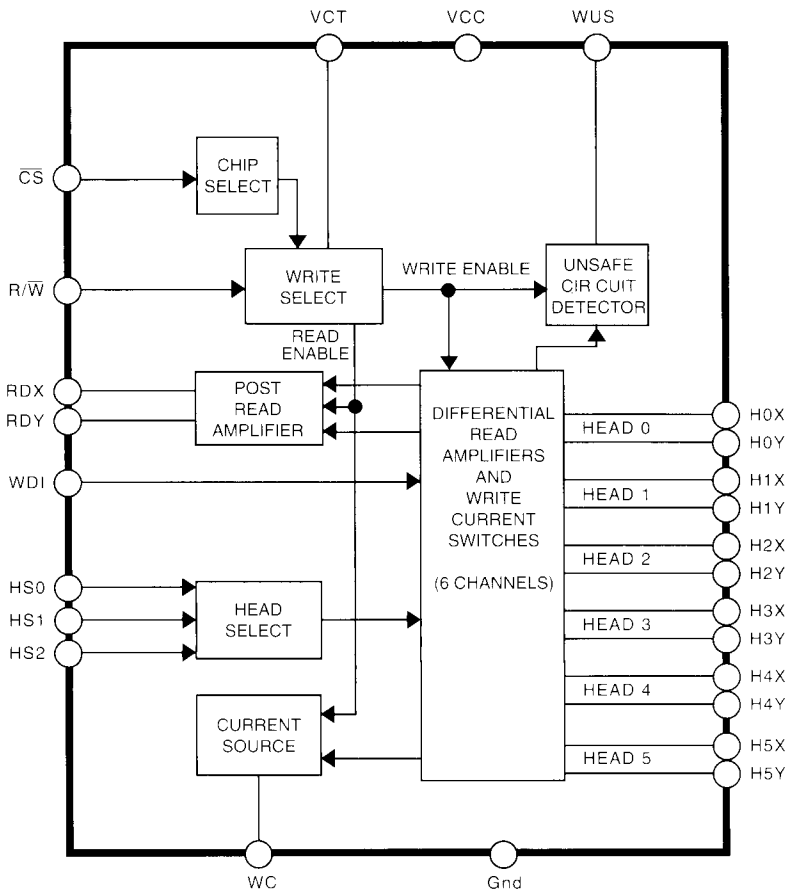
Write current transitions occur at each negative transition of the write data input. The low noise read amplifier has a typical voltage gain of 100. Balanced emitter follower outputs are used in the read amplifier. The CS-117 operates on +5V and +12V supplies.

The CS-117R performs the same function as the CS-117 with the addition of internal damping resistors.

Features

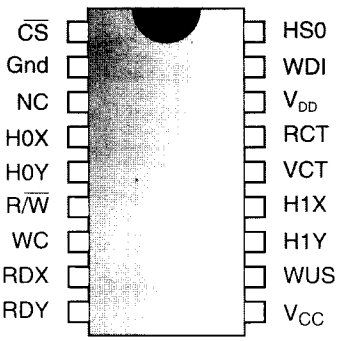
- **Controls up to 6 R/W Channels**
- **On-Chip Write Current Source Externally Set**
- **Drives Center-Tapped Ferrite Heads**
- **Independent Read and Write Busses**
- **TTL Write Data Input**
- **LSTTL Control Interface**
- **Emitter Follower Read Amplifier Outputs**
- **5V & 12V Power Supplies**

Block Diagram

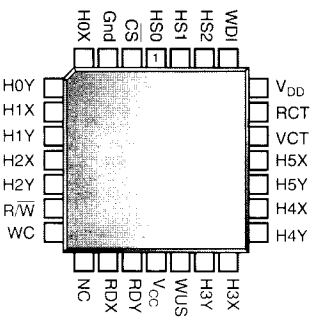


Package Options

18, 22, 28L PDIP & 18L SO Wide



28L PLCC



CSC™ CHERRY SEMICONDUCTOR

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Electrical Characteristics: V5 = 4.5 TO 5.5V, V12 = 10.8 TO 13.2V, 25°C ≤ T_J ≤ 125°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
■ Power Supply				
+5V Supply Current	Read/Idle Modes		25	mA
+5V Supply Current	Write Mode		30	mA
+12V Supply Current	Read Mode		50	mA
+12V Supply Current	Write Mode		30 + IW	mA
+12V Supply Current	Idle Mode		25	mA
Power Dissipation	Read Mode, T_J = 125°C		600	mW
Power Dissipation	Write Mode, T_J = 125°C IW = 35mA, RCT = 130		700	mW
Power Dissipation	Write Mode, T_J = 125°C IW = 35mA, RCT = 0		1050	mW
Power Dissipation	Idle Mode, T_J = 125°C		400	mW
■ Logic Signals				
Input Low Voltage (VIL)		-0.3	0.8	V
Input Low Current	VIL = 0.8V	-0.4		mA
Input High Voltage (VIH)		2.0	V_5 + 0.3	V
Input High Current	VIH = 2.0V		100	µA
US Low Level Voltage (VLUS)	ILUS = 8mA (Denotes safe condition)		0.5	V
US High Level Current (IHUS)	VHUS = 5.0V (Denotes unsafe condition)		100	µA
■ Write Mode Iw = 25mA, Lh = 10uH, Rd = 750Ω, f(Data) = 5MHz, CL (RDX, RDY) ≤ 20pF				
Write Current Range		10	35	mA
Write Current Constant "K"		133	147	V
Differential Head Voltage Swing		5.7		VpK
Unselected Diff. Head Current			2	mApK
Differential Output Capacitance			15	pF
Differential Output Resistance		10		kΩ
WDI Transition Frequency	WUS = Low	125		kHz
■ Read Mode (V_{IN} is referenced by V_{CT})				
Differential Voltage Gain	V_{IN} = 1mVpp @ 300kHz Z_L = 1kΩ per side	80	120	V/V
Bandwidth (-3dB)	Z_S < 5Ω, V_{IN} = 1mVpp	30		MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0		2.1	nV/√Hz
Differential Input Capacitance	f = 5MHz		23	pF
Differential Input Resistance	f = 5MHz	2		kΩ
Input Bias Current (per side)			45	µA
Dynamic Range	DC input voltage where gain falls by 10% (tested with 0.5mVpp input @ 300kHz)	-2.0	2.0	mV
Common Mode Rejection Ratio	V_{CM} = V_{CT} + 100mV	50		dB
Power Supply Rejection Ratio	100mVpp on V5 or V12, f = MHz	45		dB
Channel Separation	Unselected channels driven with V_{IN} = 100mVpp, f = 5MHz	45		dB
Output Offset Voltage		-480	+480	mV
Common Mode Output Voltage		5.0	7.0	V
Single Ended Output Resistance	f = 5MHz		30	Ω

Electrical Characteristics: (continued)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
■ Switching Characteristics T_J = 25°C, I_W = 35mA, Lh = 10µH, Rd = 75Ω, f(Data) = 5MHz				
Read to Write Transition Time	Delay to 90% of Write Current		1.0	µs
Write to Read Transition Time	Delay to 90% of 100mV 10MHz Read Signal Envelop Write Current Delay to 10%		1.0	µs
Head Select Switching Delay	Delay to 90% of 100mV 10MHz Read Signal Envelop		1.0	µs
Chip Disable Transition				
Read/Write to Idle	Delay to 90% Decay of Write Current		1.0	µs
Idle to Read/Write	Delay to 90% of Write Current or to 90% of 100mV 10MHz read signal envelop			
Head Current Transition Time	IW = 35mA, Lh = 0, Rh = 0 10% to 90% points		20	ns
Unsafe to Safe Delay After Write Data Begins	IW = 20mA, Lh = 10µH		1.0	µs
Safe to Unsafe Delay	IW = 35mA, Lh = 10µH	1.6	8.0	µs
Head Current Switching Delay	35mA, Lh = 0µH, Rh = 0			
a) Time	50% VIL input to 50% output		25	ns
b) Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall time		2	ns

Package Pin Description

PACKAGE PIN #			PIN SYMBOL	FUNCTION
18L PDIP/SO	22L PDIP	28L PDIP/PLCC		
1	1	2	$\overline{CS}$	Chip select; low enables device
2	2	3	Gnd	Ground connection
3		12	NC	No connection
4	3	4	HOX	X, Y Head connections
5	4	5	HOY	X, Y Head connections
6	9	10	R/$\overline{W}$	Read/Write control; high selects read mode
7	10	11	WC	Write Current; used to set the magnitude of the write current
8	11	13	RDX	X, Y, Read data; differential read signal output
9	12	14	RDY	X, Y Read Data; differential read signal output
10	13	15	V_{CC}	5V supply line
11	14	16	WUS	Write unsafe; high indicates unsafe writing condition
12	6	7	H1Y	X, Y Head connections
	8	9	H2Y	X, Y Head connections
	15	17	H3Y	X, Y Head connections
		19	H4Y	X, Y Head connections
		21	H5Y	X, Y Head connections
13	5	6	H1X	X, Y Head connections
	7	8	H2X	X, Y Head connections

Package Pin Description (continued)

PACKAGE PIN #			PIN SYMBOL	FUNCTION
18L PDIP/SO	22L PDIP	28L PDIP/PLCC		
	16	18	H3X	X, Y Head connections
		20	H4X	X, Y Head connections
		22	H5X	X, Y Head connections
14	17	23	VCT	Voltage Center Tap; voltage source for head center tap
15	18	24	RCT	External Resistor connected to V_{DD}
16	19	25	V_{DD}	12V supply line
17	20	26	WDI	Write Data In; negative transition toggles head current direction
18		1	HS0	Head select
	21	28	HS1	Head select
	22	27	HS2	Head select

Package Specification

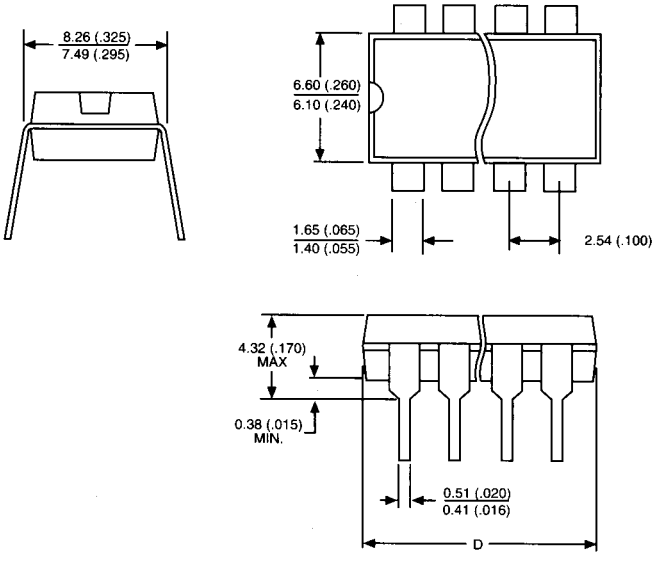
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D Metric		D English	
	Max	Min	Max	Min
18L PDIP	22.99	22.73	.905	.895
22L PDIP	27.94	27.69	1.100	1.090
28L PDIP	36.96	36.70	1.455	1.445
18 SO Wide	11.71	11.46	.461	.451
28L PLCC A	12.57	12.32	.495	.485
28L PLCC B	11.53	11.43	.454	.450

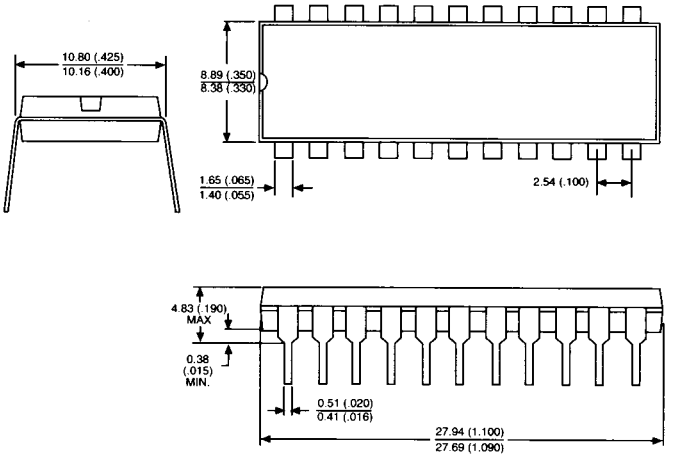
PACKAGE THERMAL DATA

Thermal Data	$R\Theta_{JA}$	$R\Theta_{JC}$	
18L PDIP	29	65	°C/W
22L PDIP	24	60	°C/W
28L PDIP	23	55	°C/W
18L SO Wide	21	100	°C/W
28L PLCC	18	70	°C/W

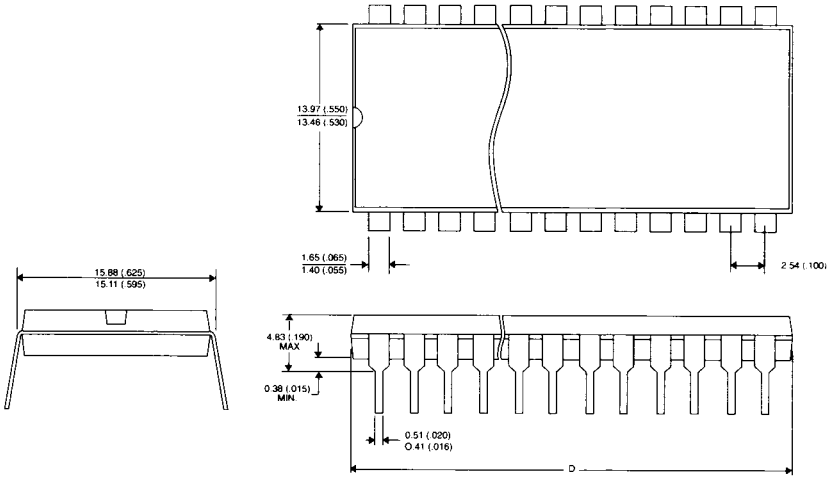
18L PDIP



22L PDIP

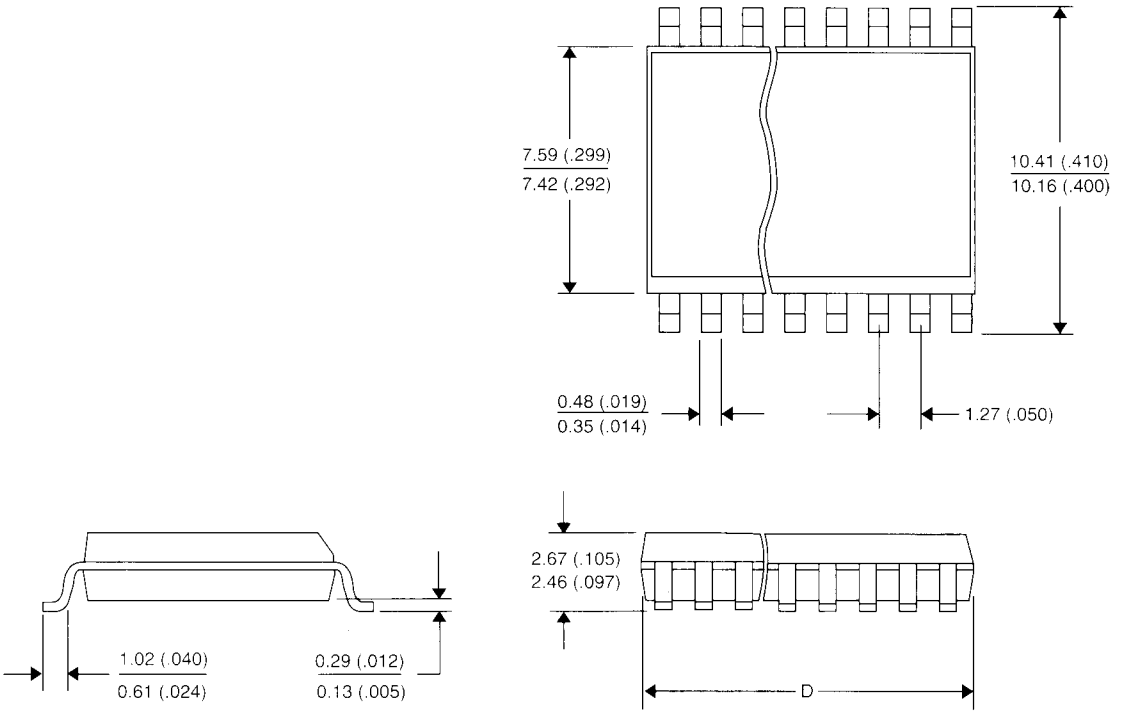


28L PDIP

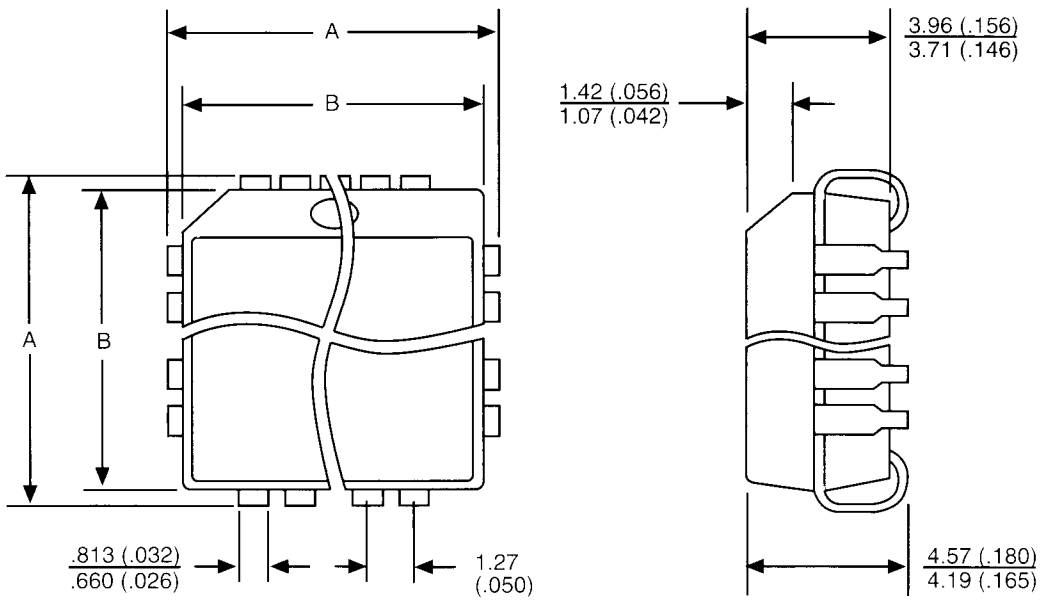


Package Specification (continued)

SO Wide



PLCC



Ordering Information

Part Number	Description
CS-117-2DW18	18 Lead SO Wide
CS-117-2N18	18 Lead PDIP
CS-117-4N22	22 Lead PDIP

With Internal Damping Resistors

Part Number	Description
CS-117-2RDW18	18 Lead SO Wide
CS-117-6RFN28	28 Lead PLCC
CS-117-6RN28	28 Lead PDIP

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