# CY62137FV30 MoBL®

## 2-Mbit (128K x 16) Static RAM

## Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40°C to +85°C
  - Automotive-A: –40°C to +85°C
  - Automotive-E: –40°C to +125°C
- Wide voltage range: 2.20V–3.60V
- Pin compatible with CY62137CV/CV25/CV30/CV33, CY62137V, and CY62137EV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 5 µA (Industrial)
- Ultra low active power
  - Typical active current: 1.6 mA at f = 1 MHz (45 ns speed)
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Byte power down feature
- Available in Pb-free 48-Ball VFBGA and 44-pin TSOP II package

## Functional Description

The CY62137FV30 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 90% when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins ($IO_0$ through $IO_{15}$) are placed in a high impedance state in the following conditions:

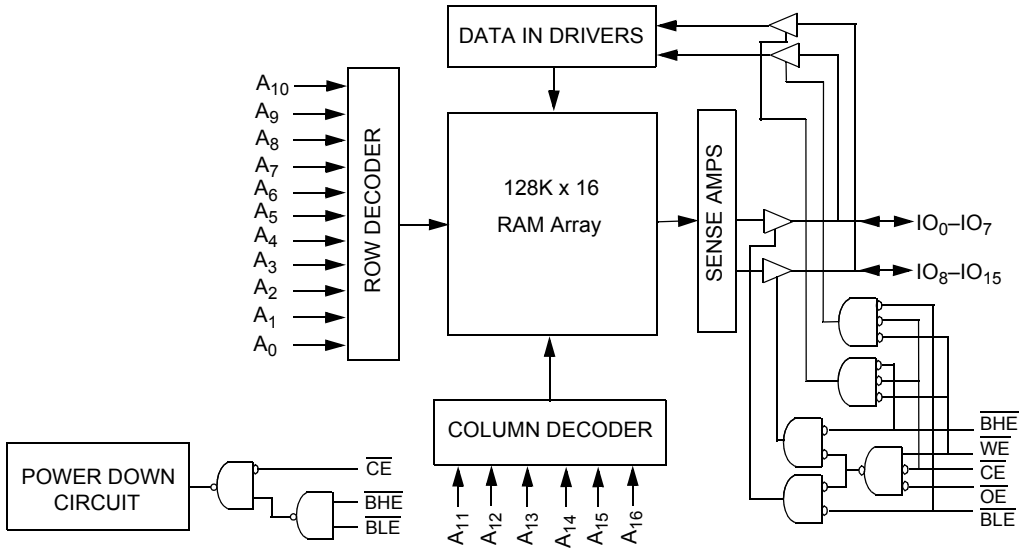
- Deselected ($\overline{CE}$ HIGH)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- Write operation is active ($\overline{CE}$ LOW and $\overline{WE}$ LOW)

Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins ($IO_0$ through $IO_7$) is written into the location specified on the address pins ($A_0$ through $A_{16}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from IO pins ($IO_8$ through $IO_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{16}$).

Read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW, while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on $IO_0$ to $IO_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on $IO_8$ to $IO_{15}$. See the "Truth Table" on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

## Logic Block Diagram



## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating $I_{CC}$ (mA) | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | | f = 1MHz | | f = $f_{max}$ | | | |
| | | Min | Typ [1] | Max | | Typ [1] | Max | Typ [1] | Max | Typ [1] | Max |
| CY62137FV30LL | Ind'l/Auto-A | 2.2V | 3.0V | 3.6V | 45 | 1.6 | 2.5 | 13 | 18 | 1 | 5 |
| | Auto-E | 2.2V | 3.0V | 3.6V | 55 | 2 | 3 | 15 | 25 | 1 | 20 |

## Pin Configuration

**Figure 1. 48-Ball VFBGA Pinout** [2, 3]

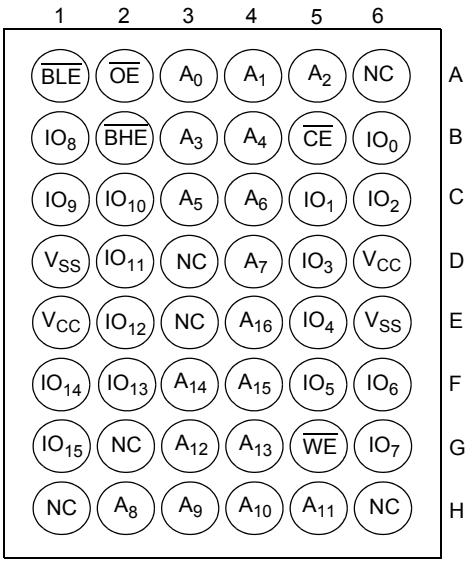
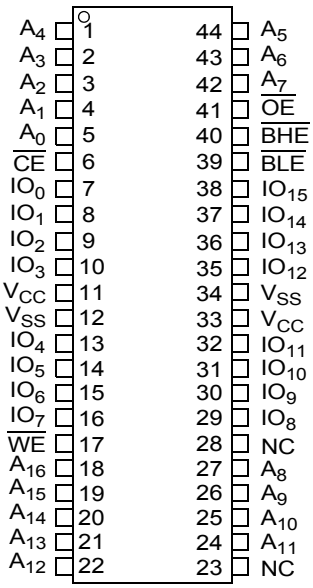



**Figure 2. 44-Pin TSOP II** [2]




**Notes**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, and H6 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb, respectively.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential .....-0.3V to 3.9V

DC Voltage Applied to Outputs in High Z state [4, 5].....-0.3V to 3.9V

DC Input Voltage [4, 5].....–0.3V to 3.9V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (MIL–STD–883, Method 3015)

Latch up Current ..... > 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ [6] |
|---|---|---|---|
| CY62137FV30LL | Ind'l/Auto-A | –40°C to +85°C | 2.2V to 3.6V |
| | Auto-E | –40°C to +125°C | |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 45 ns (Ind'l/Auto-A) | | | 55 ns (Auto-E) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Typ[1] | Max | |
| $V_{OH}$ | Output HIGH Voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OH}$ = –0.1 mA | 2.0 | | | 2.0 | | | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OH}$ = –1.0 mA | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $2.2 \le V_{CC} \le 2.7$ | $I_{OL}$ = 0.1 mA | | | 0.4 | | | 0.4 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | $I_{OL}$ = 2.1mA | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | $2.2 \le V_{CC} \le 2.7$ | | 1.8 | | $V_{CC}$ + 0.3 | 1.8 | | $V_{CC}$ + 0.3 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | 2.2 | | $V_{CC}$ + 0.3 | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | $2.2 \le V_{CC} \le 2.7$ | | –0.3 | | 0.6 | –0.3 | | 0.6 | V |
| | | $2.7 \le V_{CC} \le 3.6$ | | –0.3 | | 0.8 | –0.3 | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $GND \le V_I \le V_{CC}$ | | –1 | | +1 | –4 | | +4 | µA |
| $I_{OZ}$ | Output Leakage Current | $GND \le V_O \le V_{CC}$, Output disabled | | –1 | | +1 | –4 | | +4 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $f = f_{max} = 1/t_{RC}$ | $V_{CC} = V_{CC(max)}$, $I_{OUT}$ = 0 mA, CMOS levels | | 13 | 18 | | 15 | 25 | mA |
| | | f = 1 MHz | | | 1.6 | 2.5 | | 2 | 3 | |
| $I_{SB1}$ | Automatic CE Power Down Current – CMOS Inputs | $\overline{CE} \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V, $V_{IN} \le$ 0.2V, f = $f_{max}$ (address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, and $\overline{BLE}$), $V_{CC}$ = 3.60V | | | 1 | 5 | | 1 | 20 | µA |
| $I_{SB2}$ [7] | Automatic CE Power Down Current – CMOS Inputs | $\overline{CE} \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0, $V_{CC}$ = 3.60V | | | 1 | 5 | | 1 | 20 | µA |

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

**Notes**

4. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
5. $V_{IH(max)}=V_{CC}$+0.75V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC}$(min) and 200 µs wait time after $V_{CC}$ stabilization.
7. Only chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) are tied to CMOS levels to meet the $I_{SB2}$ / $I_{CCDR}$ specification. Other inputs can be left floating.

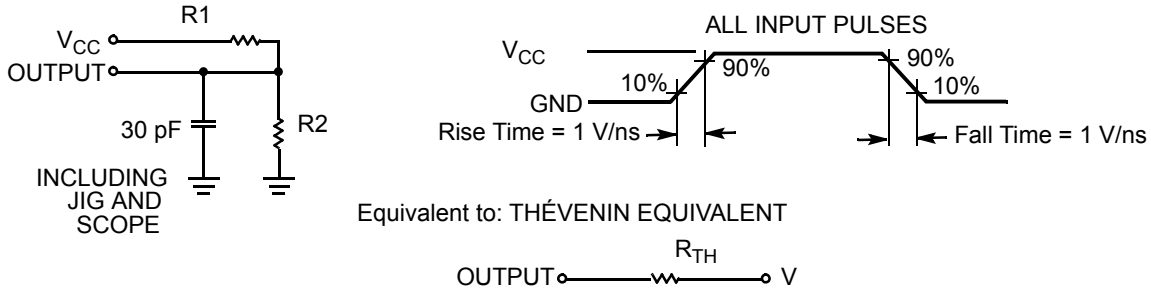
## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | VFBGA | TSOP II | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board | 75 | 77 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 10 | 13 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveform**




| Parameters | 2.5V (2.2V to 2.7V) | 3.0V (2.7V to 3.6V) | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

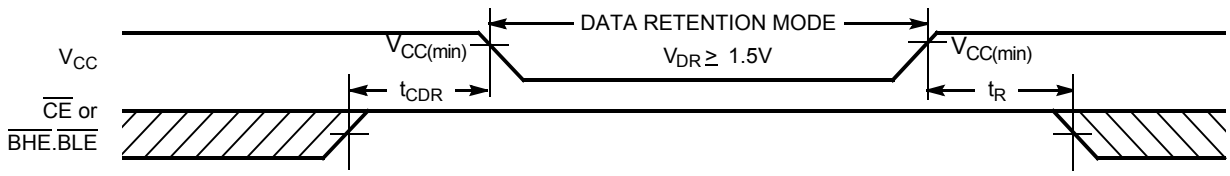
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | | Min | Typ [1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | | 1.5 | | | V |
| $I_{CCDR}$ [7] | Data Retention Current | $V_{CC}$ = 1.5V, $\overline{CE} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$ | Ind'l/Auto-A | | | 4 | µA |
| | | | Auto-E | | | 12 | |
| $t_{CDR}$ [8] | Chip Deselect to Data Retention Time | | | 0 | | | ns |
| $t_R$ [9] | Operation Recovery Time | | | $t_{RC}$ | | | ns |

## Data Retention Waveform

**Figure 4. Data Retention Waveform** [10]




**Notes**

8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
10. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

Over the Operating Range [11, 12]

| Parameter | Description | 45 ns (Ind'l/Auto-A) | | 55 ns (Auto-E) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 45 | | 55 | | ns |
| $t_{AA}$ | Address to Data Valid | | 45 | | 55 | ns |
| $t_{OHA}$ | Data Hold From Address Change | 10 | | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 45 | | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 22 | | 25 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [13] | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [13, 14] | | 18 | | 20 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z [13] | 10 | | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z [13, 14] | | 18 | | 20 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power Up | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power Down | | 45 | | 55 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Data Valid | | 45 | | 55 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Low Z [13, 15] | 5 | | 10 | | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to High Z [13, 14] | | 18 | | 20 | ns |
| **Write Cycle** [16] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 45 | | 55 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 35 | | 40 | | ns |
| $t_{AW}$ | Address Setup to Write End | 35 | | 40 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Setup to Write Start | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 35 | | 40 | | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Write End | 35 | | 40 | | ns |
| $t_{SD}$ | Data Setup to Write End | 25 | | 25 | | ns |
| $t_{HD}$ | Data Hold From Write End | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [13, 14] | | 18 | | 20 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [13] | 10 | | 10 | | ns |

**Notes**

11. Test conditions for all parameters, other than tri-state parameters, assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in "AC Test Loads and Waveforms" on page 4.
12. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. Please see application note AN13842 for further clarification.
13. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
14. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
15. If both byte enables are toggled together, this value is 10 ns.
16. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

## Switching Waveforms

**Figure 5. Read Cycle 1: Address Transition Controlled** [17, 18]

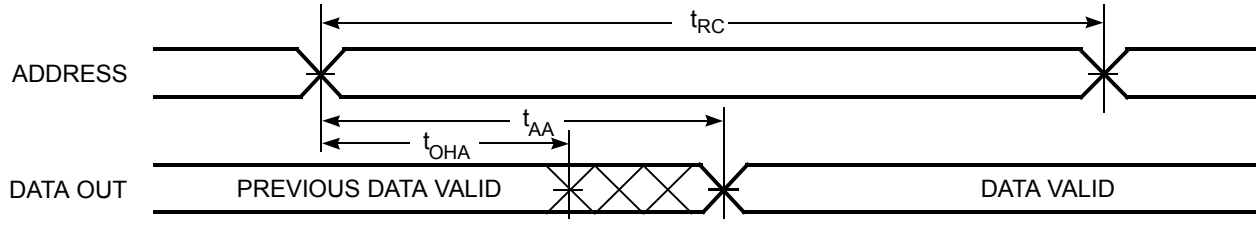
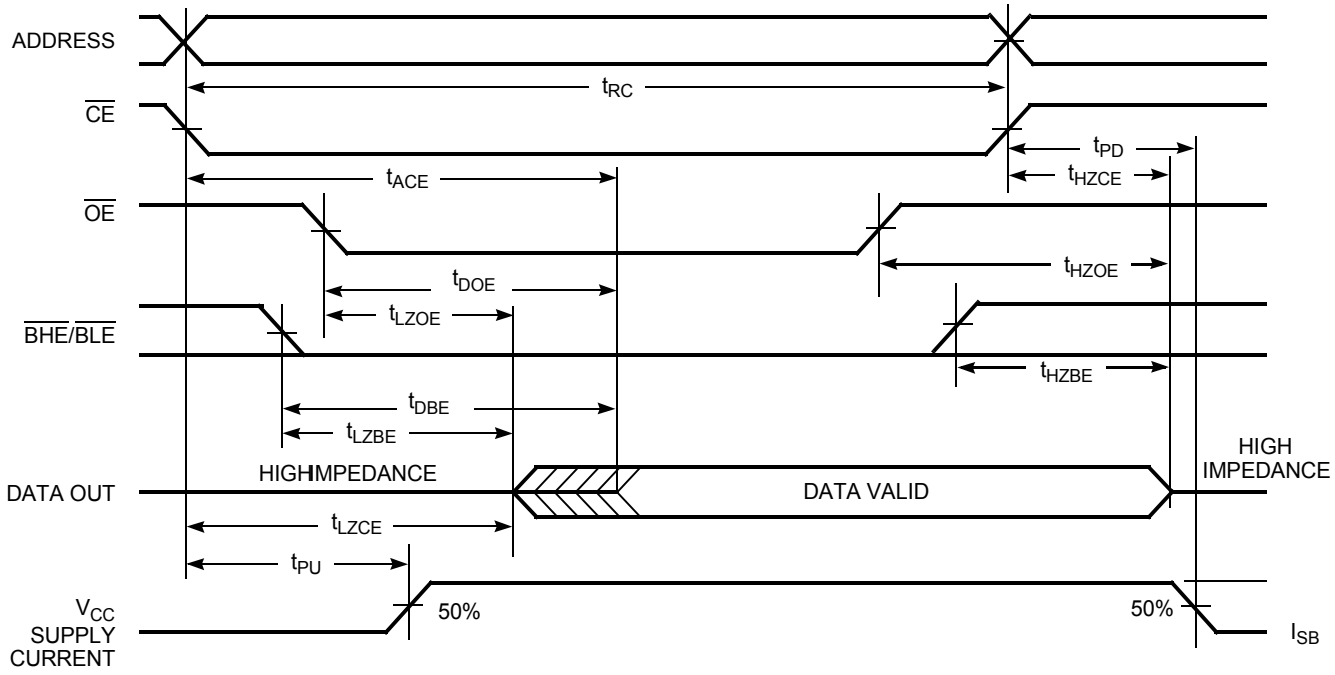



**Figure 6. Read Cycle 2: $\overline{OE}$ Controlled** [18, 19]




**Notes**
17. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$.
18. $\overline{WE}$ is HIGH for read cycle.
19. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 7. Write Cycle 1: $\overline{WE}$ Controlled** [16, 20, 21]

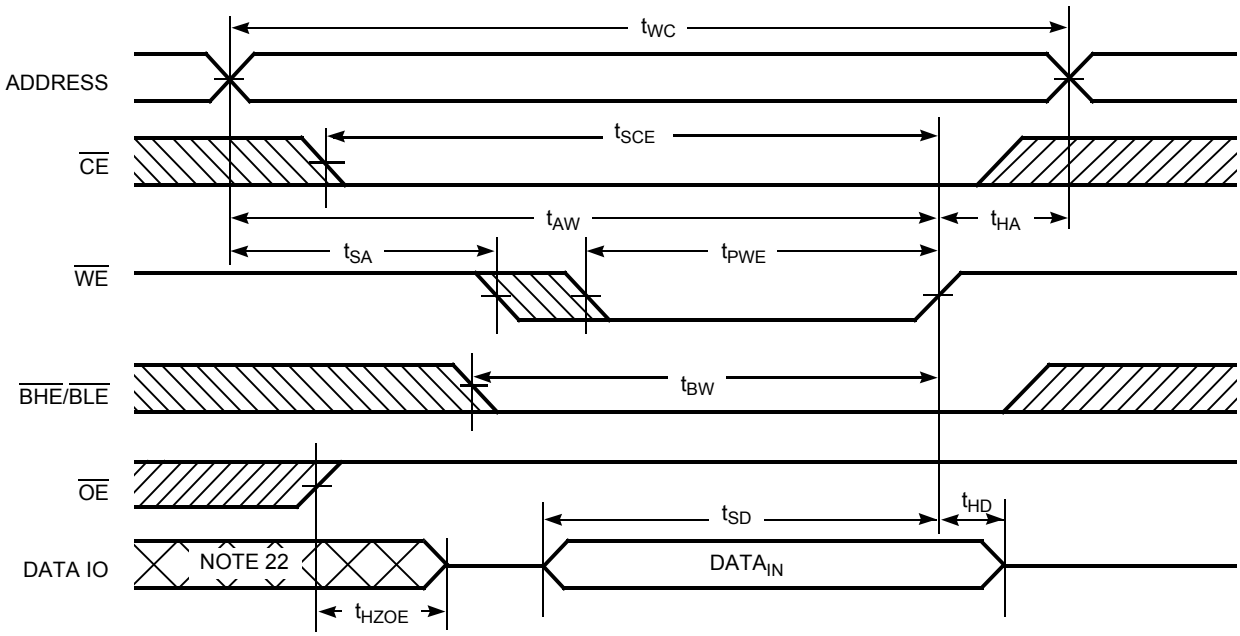
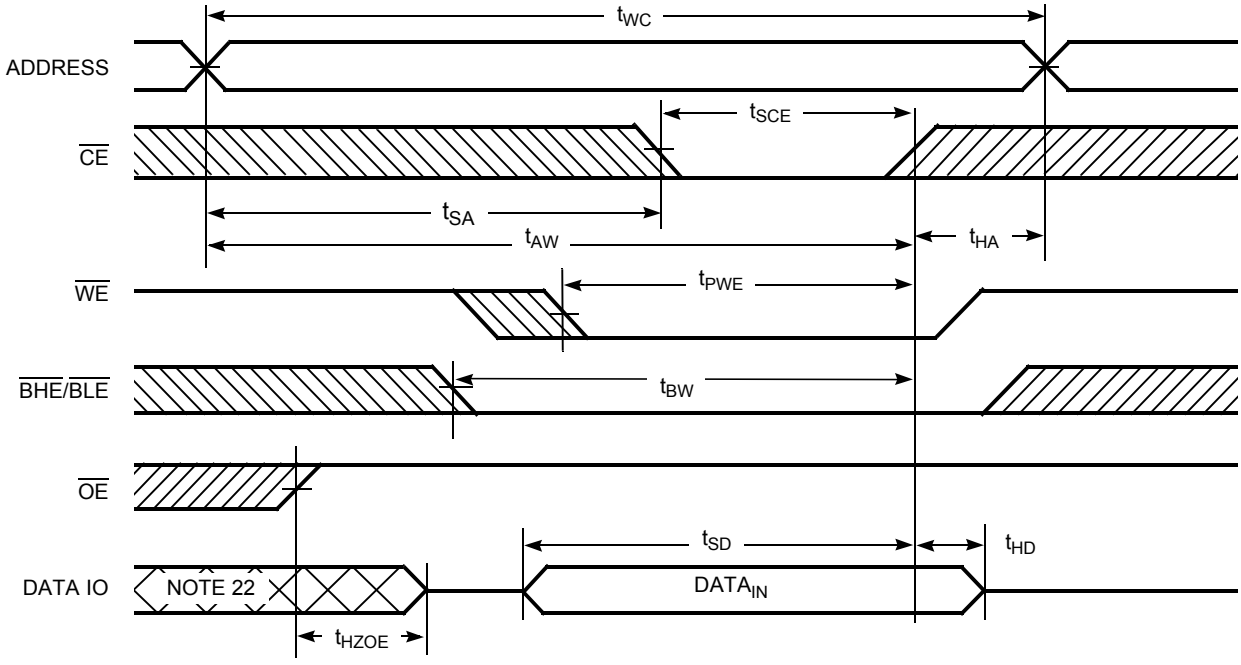



**Figure 8. Write Cycle 2: $\overline{CE}$ Controlled** [16, 20, 21]




**Notes**
20. Data IO is high impedance if $\overline{OE}$ = $V_{IH}$.
21. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
22. During this period, the IOs are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 9. Write Cycle 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [21]**

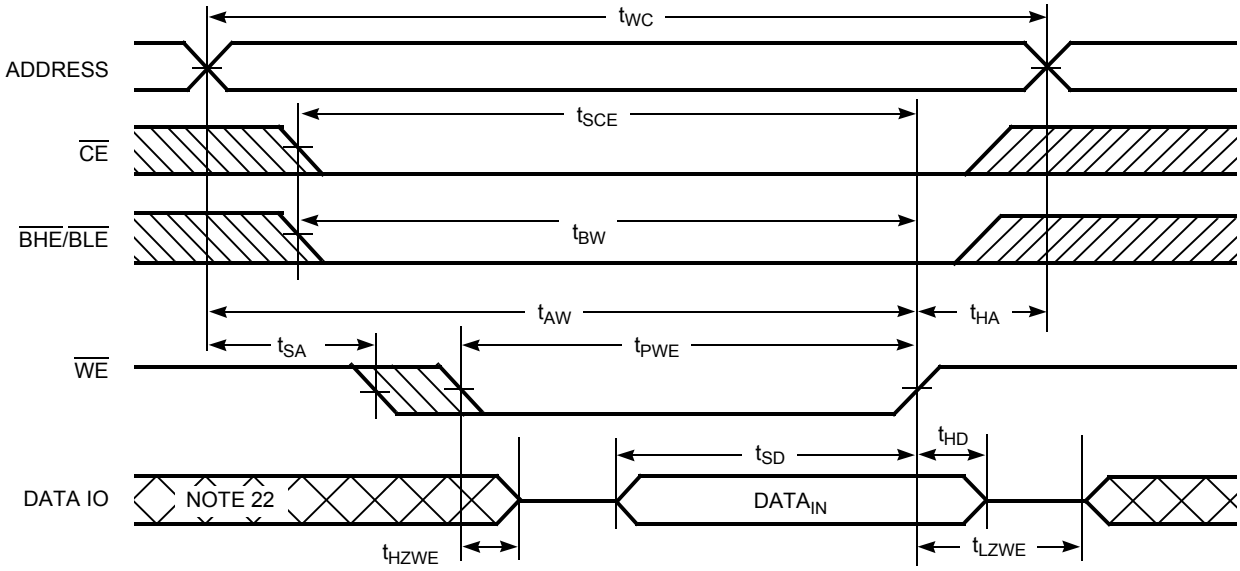
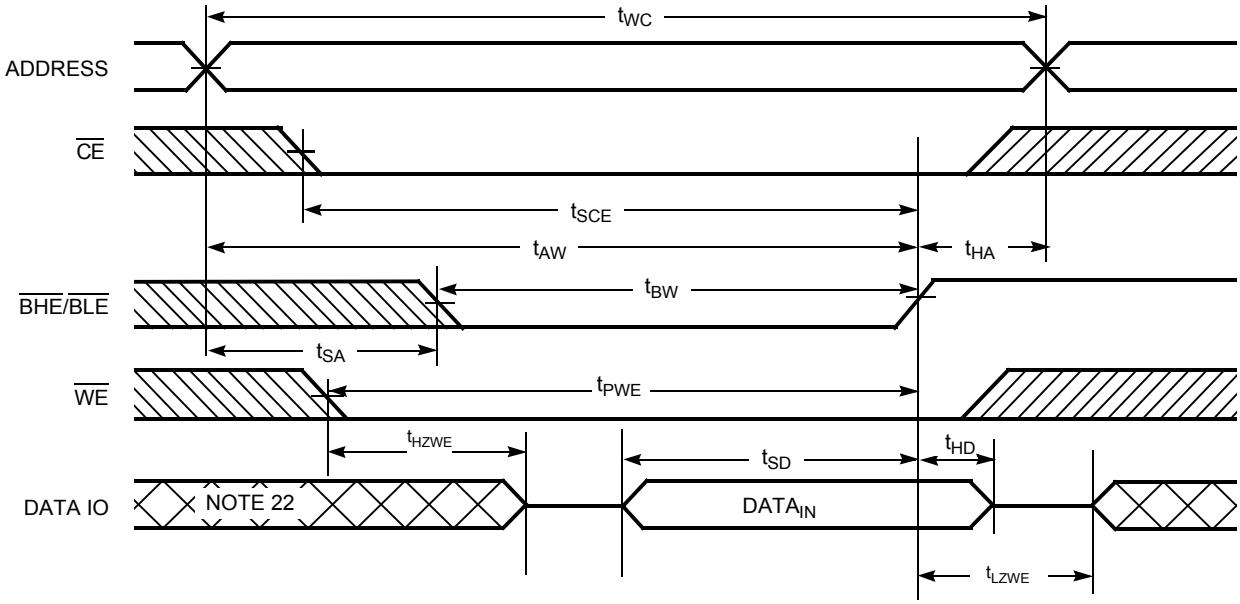



**Figure 10. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [21]**



## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs or Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | Deselect or Power Down | Standby ($I_{SB}$) |
| X | X | X | H | H | High Z | Deselect or Power Down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data Out ($IO_0$–$IO_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data Out ($IO_0$–$IO_7$); $IO_8$–$IO_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data Out ($IO_8$–$IO_{15}$); $IO_0$–$IO_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data In ($IO_0$–$IO_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data In ($IO_0$–$IO_7$); $IO_8$–$IO_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data In ($IO_8$–$IO_{15}$); $IO_0$–$IO_7$ in High Z | Write | Active ($I_{CC}$) |

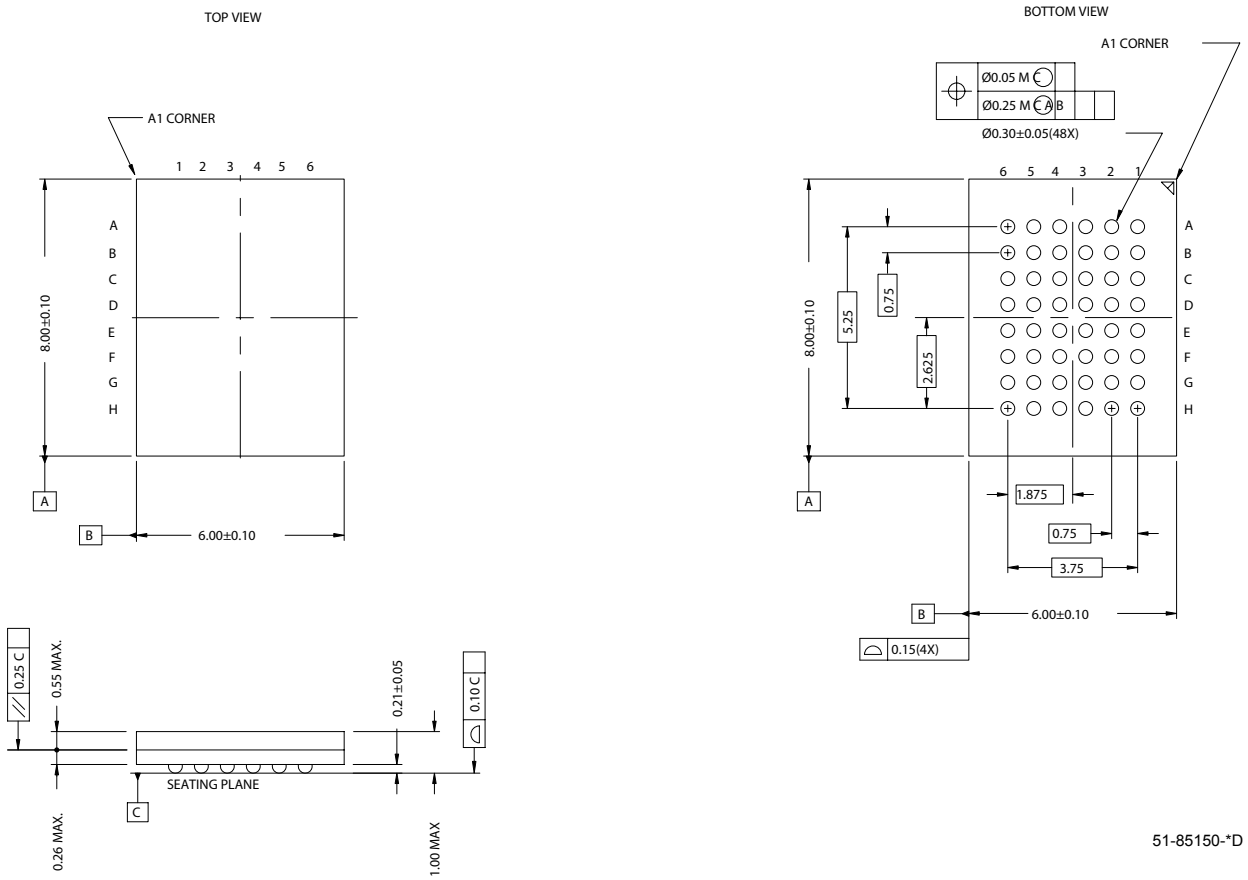
## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62137FV30LL-45BVXI | 51-85150 | 48-Ball VFBGA (Pb-free) | Industrial |
| | CY62137FV30LL-45ZSXI | 51-85087 | 44-Pin TSOP II (Pb-free) | |
| 45 | CY62137FV30LL-45ZSXA | 51-85087 | 44-Pin TSOP II (Pb-free) | Automotive-A |
| 55 | CY62137FV30LL-55ZSXE | 51-85087 | 44-Pin TSOP II (Pb-free) | Automotive-E |

Contact your local Cypress sales representative for availability of these parts.

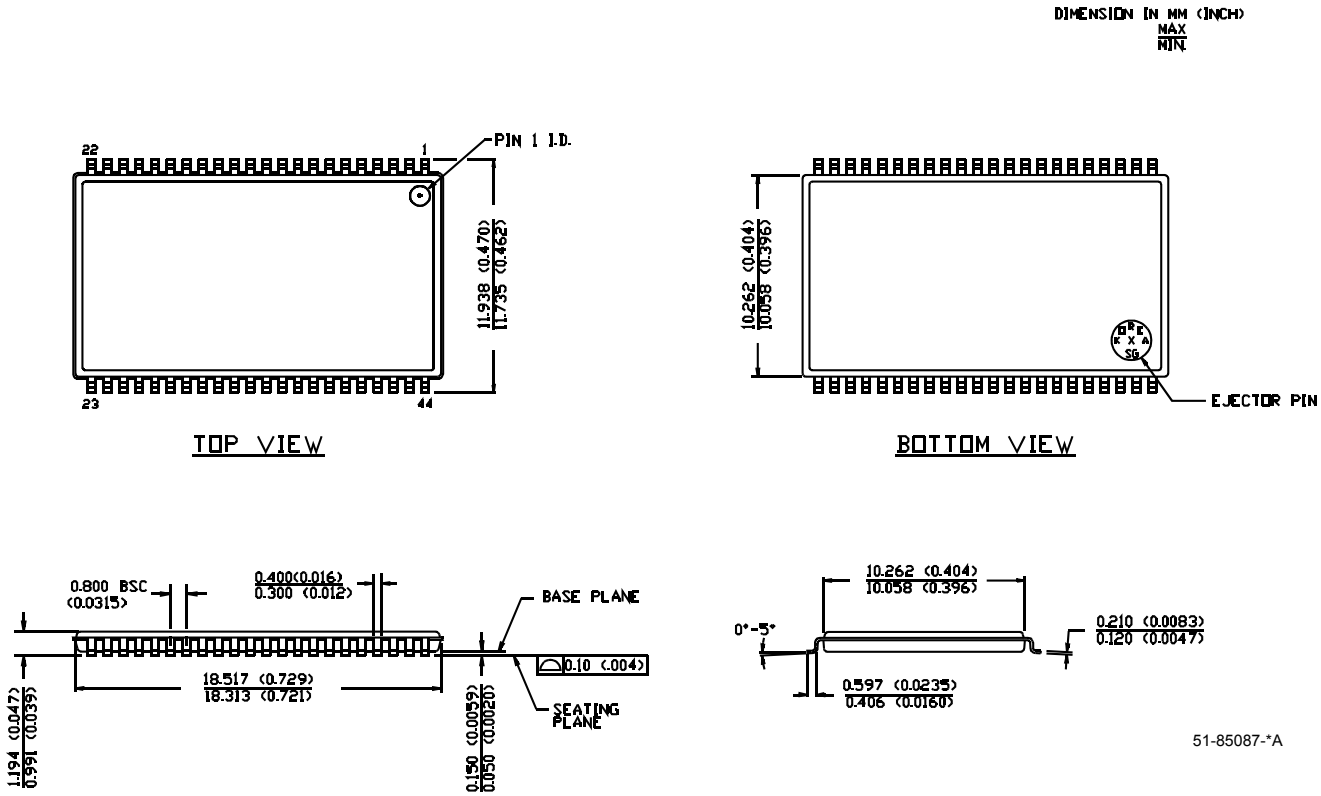
## Package Diagram

**Figure 11. 48-Ball VFBGA (6 x 8 x 1 mm)**



## Package Diagram (continued)

**Figure 12. 44-Pin TSOP II**



## Document History Page

| Document Title: CY62137FV30 MoBL® 2-Mbit (128K x 16) Static RAM<br>Document Number: 001-07141 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 449438 | See ECN | NXR | New datasheet |
| *A | 464509 | See ECN | NXR | Changed the $I_{SB2(typ)}$ value from 1.0 μA to 0.5 μA<br>Changed the $I_{SB2(max)}$ value from 4 μA to 2.5 μA<br>Changed the $I_{CC(typ)}$ value from 2 mA to 1.6 mA and $I_{CC(max)}$ value from 2.5 mA to 2.25 mA for f=1 MHz test condition<br>Changed the $I_{CC(typ)}$ value from 15 mA to 13 mA and $I_{CC(max)}$ value from 20 mA to 18 mA for f=1 MHz test condition<br>Changed the $I_{CCDR(typ)}$ value from 0.7 μA to 0.5 μA and $I_{CCDR(max)}$ value from 3 μA to 2.5 μA |
| *B | 566724 | See ECN | NXR | Converted from preliminary to final<br>Changed the $I_{CC(max)}$ value from 2.25 mA to 2.5 mA for test condition f=1 MHz<br>Changed the $I_{SB2(typ)}$ value from 0.5 μA to 1 μA<br>Changed the $I_{SB2(max)}$ value from 2.5 μA to 5 μA<br>Changed the $I_{CCDR(typ)}$ value from 0.5 μA to 1 μA and $I_{CCDR(max)}$ value from 2.5 μA to 4 μA |
| *C | 869500 | See ECN | VKN | Added Automotive-A and Automotive-E information<br>Updated Ordering Information Table<br>Added footnote 13 related to $t_{ACE}$ |
| *D | 901800 | See ECN | VKN | Added footnote 9 related to $I_{SB2}$ and $I_{CCDR}$<br>Made footnote 14 applicable to AC parameters from $t_{ACE}$ |
| *E | 1371124 | See ECN | VKN/AESA | Converted Automotive information from preliminary to final<br>Changed $I_{IX}$ min spec from –1 μA to –4 μA and $I_{IX}$ max spec from +1 μA to +4 μA<br>Changed $I_{OZ}$ min spec from –1 μA to –4 μA and $I_{OZ}$ max spec from +1 μA to +4 μA |