Edge672
500 MHz Pin Electronics Window Comparator and Load

EDGE HIGH-PERFORMANCE PRODUCTS — PRELIMINARY

Description

The Edge672 is a monolithic ATE pin electronics comparator and load solution manufactured in a high-performance complementary bipolar process. In automatic test equipment, the Edge672 incorporates a dynamic load and window comparator suitable for very fast, bidirectional channels in Memory, VLSI, and Mixed-Signal test systems.

The three-statable load is capable of sourcing and sinking 35 mA over an 11V common mode range. Source and sink currents are independently programmable. The load is configurable to support a clamping function, a termination function, plus any custom load configurations.

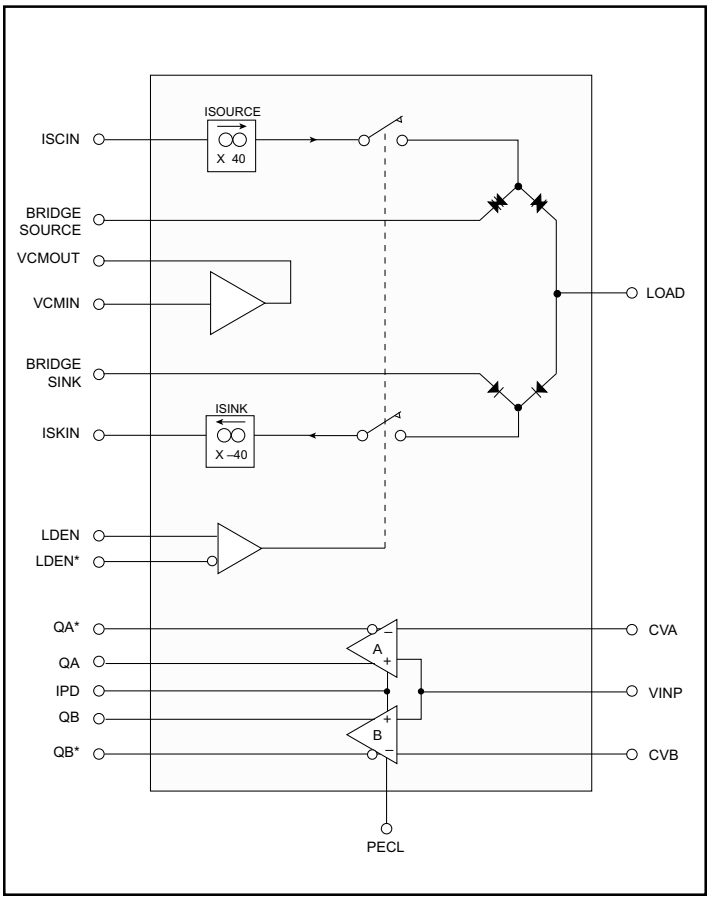
The comparator is capable of tracking very fast edges and passing sub-ns pulses over a 11V common mode range while maintaining excellent timing accuracy. The differential digital outputs are adjustable to accommodate ECL levels, PECL levels, or custom levels to interface directly with a CMOS ASIC.

The inclusion of a high performance load and comparator in a 32 pin TQFP (7 mm X 7 mm) package offers a highly integrated solution traditionally implemented with multiple integrated circuits or discrete components.

Features

- 11V Common Mode Range
- Programmable to ±35 mA
- Comparator Input Tracking > 6 V/ns with < ±25 ps dispersion
- Low Leakage (L+C) < 1 µA
- Comparator Input Power Down Mode (for extremely low leakage operation < 250 nA)
- Small footprint (32 pin TQFP)

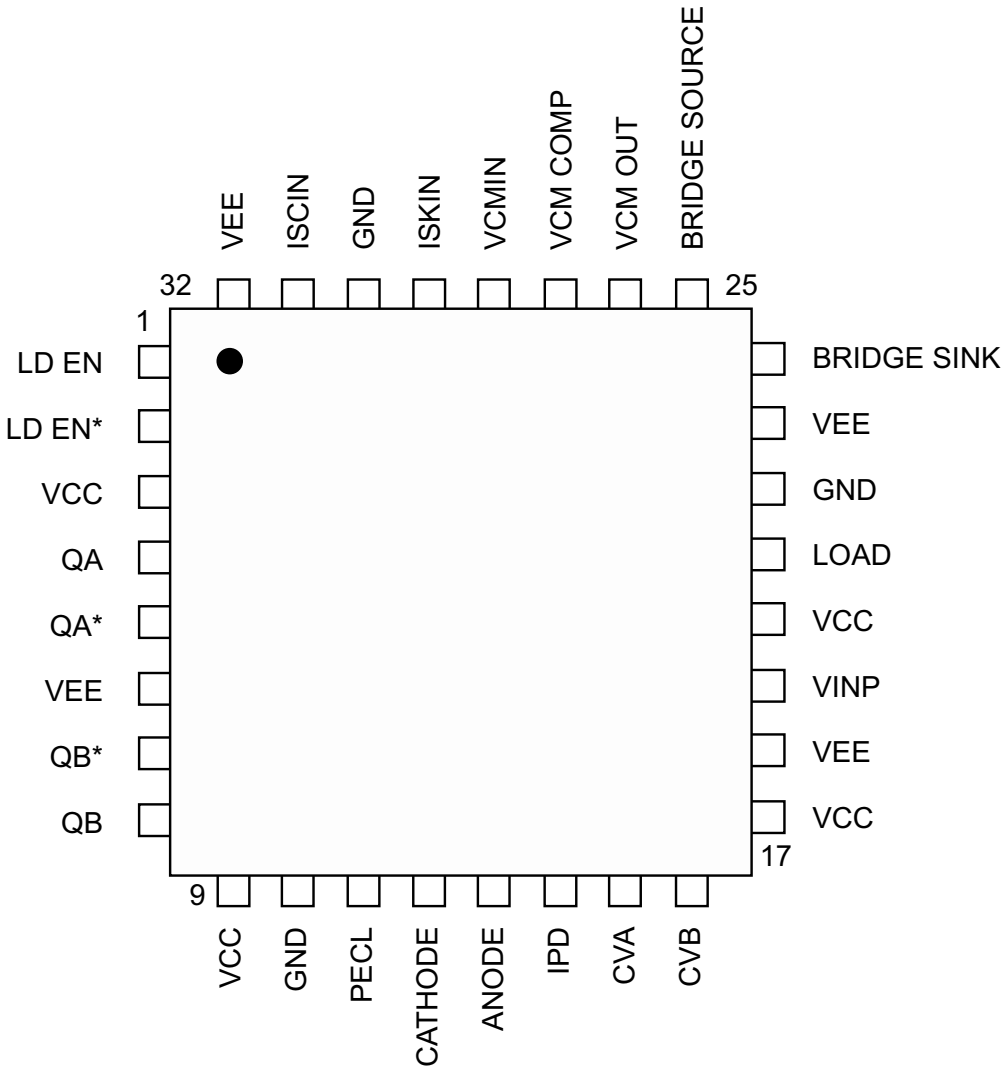
Functional Block Diagram



PIN Description

Pin Name	Pin #	Description
Load		
VCMIN	28	Analog input that programs the commutating voltage.
ISCIN ISKIN	31 29	Analog current inputs that program the load source and sink currents.
LDEN LDEN*	1 2	Wide voltage differential input pins that turn the load on and off.
VCMCOMP	27	Analog input pin. A .01 µF or greater caacitor to ground should be connected.
LOAD	21	Load diode bridge output.
VCMOUT	26	Analog voltage which drives the diode bridge.
BRIDGE SOURCE BRIDGE SINK	25 24	Upper and lower half (respectively) of the diode bridge.
Comparator		
VINP	19	Analog voltage input for the window comparator. The VINP connects to both of the noninverting (+) inputs of the comparators.
QA / QA* QB / QB*	4, 5 8, 7	Differential output pins from the window comparator.
CVA, CVB	15, 16	Analog input pins used to set the high and low levels for the window comparator.
IPD	14	TTl compatible input which activates the input power down mode of the window comparator.
Power		
VEE	6, 18, 23, 32	Negative power supply.
VCC	3, 9, 17, 20	Positive power supply.
GND	10, 22, 30	Device ground.
PECL	11	Analog power supply which sets the comparator output levels.
Test Pins		
CATHODE ANODE	12 13	Cathode and anode ends of a series of diodes used to monitor the die temperature.

PIN Description *(continued)*



Load

Introduction

The load section is capable of sourcing and sinking up to 35 mA, both statically and dynamically, or being placed in a high impedance state.

Load Enable

The load is controlled by the load enable input (LDEN / LDEN*). If LDEN is more positive than LDEN*, the output diode bridge will be active. If LDEN is more negative than LDEN*, the LOAD pin will be placed in a high impedance state.

Source and Sink Levels

The amount of current that the diode bridge can source and sink is adjustable from 0 mA to 35 mA. The source and sink levels are separate and independent.

ISCIN is a current input node which programs the bridge source current. There is a gain of 40 between the ISCIN current and the bridge source current. ISKIN is a current input node that programs the bridge sink current. There is a gain of –40 between the ISKIN current and the bridge sink current.

$$ISOURCE = 40 * ISCIN$$
$$ISINK = -40 * ISKIN$$

Caution: The ISKIN and ISCIN inputs are designed for positive current between 0 mA and .875 mA flowing into the Edge672. Care should be taken to insure that current is never required to flow out of the Edge672 on these two nodes.

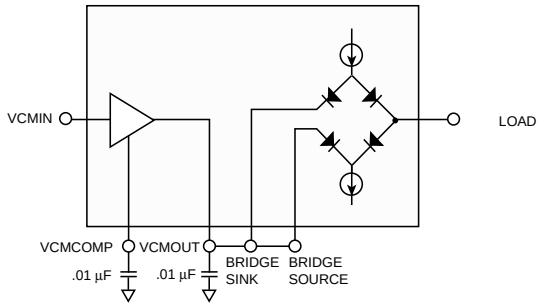


Figure 3. Commutating Voltage Compensation

Commutating Voltage

VCMIN is a high input impedance voltage input node that sets the voltage level at which the diode bridge switches from sourcing to sinking currents. If LOAD is more positive than VCMIN, the bridge will sink current from the DUT into the Edge672 (see Figure 1). If LOAD is more negative than VCMIN, the bridge will source current from the Edge672 into the DUT (see Figure 2).

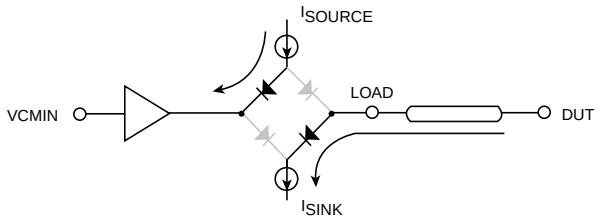


Figure 1. LOAD > VCMIN
The Edge 672 sinks DUT current.

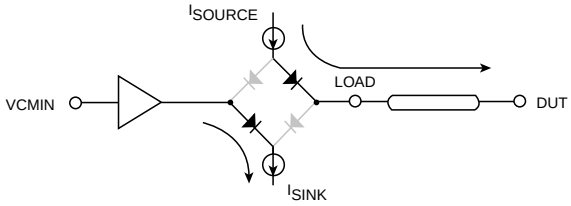


Figure 2. LOAD < VCMIN
The Edge 672 sources DUT current.

Commutating Voltage Compensation

The VCMOUT pin is the actual commutation voltage seen by the load diode bridge (see Figure 3). This node requires a fixed .01 µF capacitor (with good high frequency characteristics) to ground.

The VCMCOMP pin is an analog output pin that requires a fixed .01 µF chip capacitor (with good high frequency characteristics) to ground (See Figure 3). This capacitor is used to compensate an internal node on the on-chip op amp used to buffer the commutating voltage input.

Circuit Description *(continued)*

Load Configuration

The load is flexible in that VCMOUT, BRIDGE SINK, and BRIDGE SOURCE are all brought out to separate pins. This flexibility allows the load to be configured in several different ways.

The standard load topology, where VCMOUT, BRIDGE SINK, and BRIDGE SOURCE are all connected together (see Figure 4), behaves like the traditional active load.

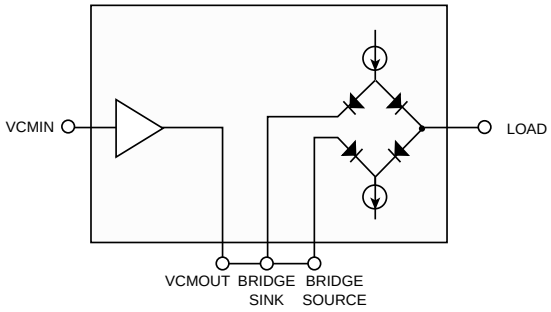


Figure 4. Standard Active Load Configuration

Clamping Function

The load can also act as set of programmable clamps that can absorb any DUT overshoot that would normally be present when the pin electronics are receiving a DUT signal. By connecting VCMOUT and BRIDGE SINK together, and then bringing in an externally buffered voltage to BRIDGE SOURCE (see Figure 5), VCMIN becomes the low voltage clamp and the external voltage becomes the high voltage clamp.

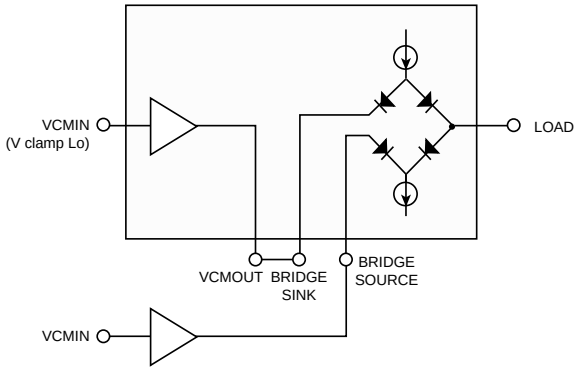


Figure 5. Load as a Programmable Clamp

Circuit Description *(continued)*

Window Comparator

Introduction

The Edge672 has two comparators connected on-chip as a window comparator to determine whether the DUT is in a high, low, or indeterminate state.

Functionality

The VINP pin is tied to the positive inputs of both comparators (see Figure 6).

Input Condition	Output Condition
VINP > CVA	QA = High; QA* = Low
VINP < CVA	QA = Low; QA* = High
VINP > CVB	QB = High; QB* = Low
VINP < CVB	QB = Low; QB* = High

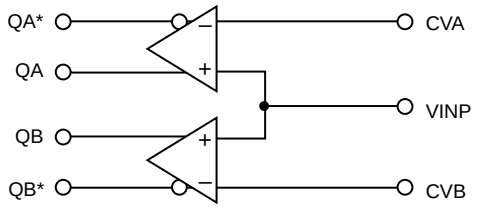


Figure 6. Comparator Functionality

Thresholds

CVA and CVB are the two comparator threshold levels. These inputs are high impedance voltage controlled inputs that determine at which VINP input voltage the comparator will change states.

Hysteresis

Hysteresis is a measure of the change in threshold voltage as a function of the comparator output state (see Figure 7). Typically, hysteresis is used to prevent multiple comparator output transitions due to slow input slew rates in a noisy environment. These slower inputs remain in the transition region for longer periods of time, allowing any noise present to cause repeated threshold crossings.

The Edge672 is designed with 4 mV of hysteresis. This hysteresis is nonadjustable and requires no external support. The amount of hysteresis was chosen to allow stable and reliable transitions in most system environments, without noticeably affecting the comparator performance.

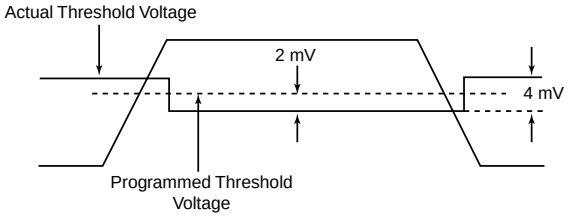


Figure 7. Hysteresis

The effects of hysteresis are visible in two categories - offset voltage and propagation delay. The amount of hysteresis must be large enough to overcome the system noise floor, yet small enough not to increase offset voltage effects significantly.

Input Protection

The VINP pin has an internal 50Ω series resistor and two over-voltage diodes capable of shunting up to 100 mA (see Figure 8) and, therefore, requires no external protection circuitry. The over-voltage input range that the comparator can withstand is determined by the power supply rails and the following equations:

$$VEE - .7 - (100\ mA * 50\Omega) < VINP < VCC + .7 + (100\ mA * 50\Omega)$$

or

$$VEE - 5.7V < VINP < VCC + 5.7V.$$

Circuit Description *(continued)*

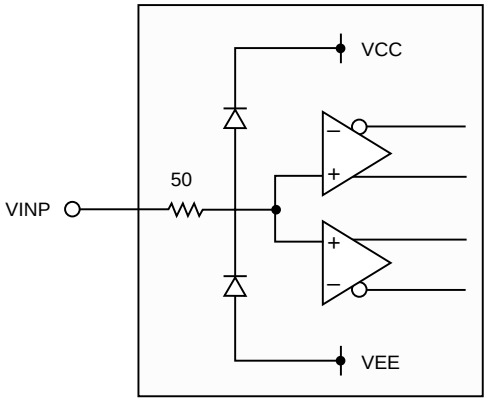


Figure 8. Input Protection

For a wider protected input range, an additional external series resistor may be added.

Comparator PECL Output Capability

PECL is a variable analog voltage power supply that determines the common mode voltage of the comparator digital outputs. With PECL connected to ground, the outputs generate standard differential ECL levels. However, the outputs will track the PECL input, remaining one diode drop below it as PECL is varied between ground and +5V. By setting PECL appropriately, a fully differential comparator output may interface directly to a CMOS ASIC without any translators.

Input Power Down

The comparator has a mechanism where it can drastically reduce the input bias current flowing into the VINP pin, while still maintaining a functional comparator. In this mode, however, the comparator slows down significantly and can no longer track fast edges, in particular, fast falling edges.

The IPD pin is a TTL compatible input which controls the two modes. With IPD = low, the comparator is in its normal high speed mode, supporting maximum AC performance.

With IPD = high, the comparator is in Power Down Mode. The input bias current decreases to < 250 nA. The comparator still functions, but can track edges only up to 25 mV/ns.

Thermal Monitor

An on-chip thermal monitor is accessible through the CATHODE and ANODE pins. These nodes connect to five diodes in series (see Figure 9) and may be used to accurately measure the junction temperature at any time.

An external bias current of 100 µA is injected through the string, and the measured voltage corresponds to a specific junction temperature with the following equation:

$$Tj[°C] = \{(ANODE - CATHODE)/5 - .7\} / (-.00208).$$

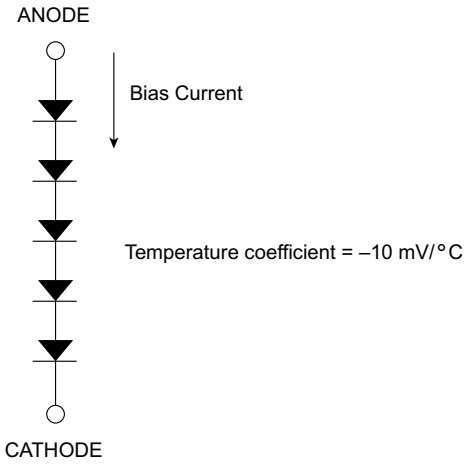


Figure 9. Thermal Diode String

Circuit Description *(continued)*

Delay Dispersion

Given a constant temperature and voltage environment (within the bounds of the recommended operating conditions), the propagation delay dispersion (TSD) indicates how much variation in propagation delay time can be expected for one comparator over a wide range of input conditions. Thus, the propagation delay of a comparator can be described as:

$$Tpd \pm TSD$$

where TPD is the nominal delay that will vary with temperature and voltage, and part-to-part. In many ATE applications, Tpd is calibrated or compensated for on a channel-by-channel basis. TSD includes factors that normally may be difficult to calibrate, and therefore directly impact overall system timing accuracy.

Propagation delay dispersion is defined as the maximum deviation of the propagation delay taken at the eight measurement points (see Figure 10) for 1V and 3 V input signals described below. The parameters of interest are:

- Slew rate
- Edge direction
- Overdrive
- Common mode voltage.

Low dispersion numbers indicate the accuracy of a system under a variety of input conditions, and are an important figure of merit for any comparator.

While not production tested, the Edg672 is designed specifically to exhibit low dispersion. The typical Edge672 will show less than 25 ps Tpd dispersion.

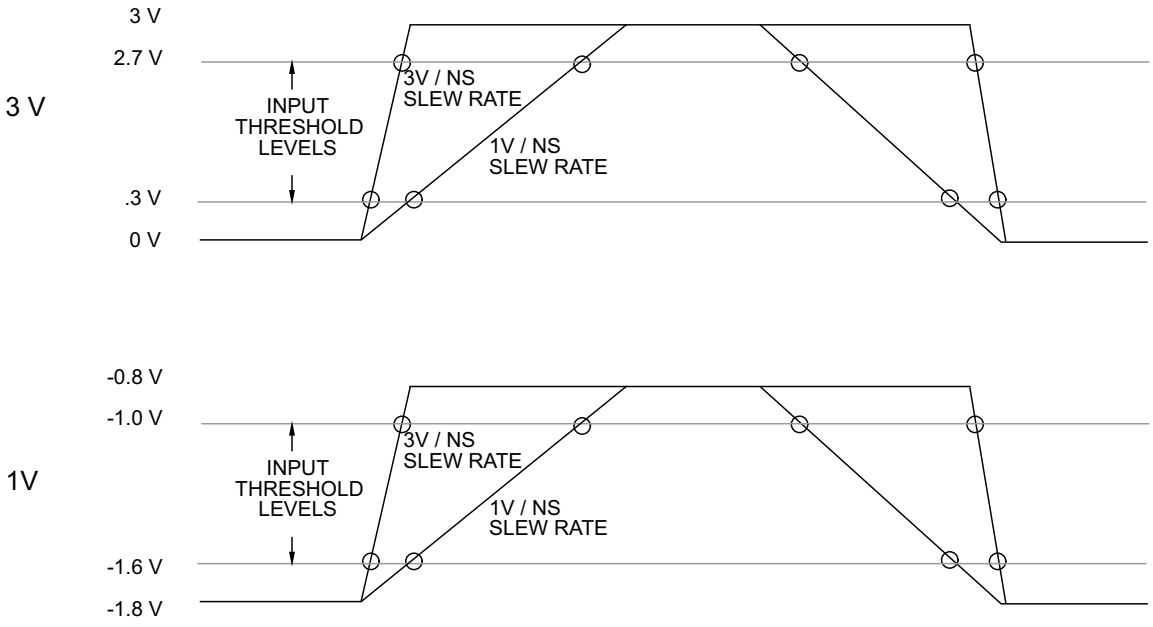
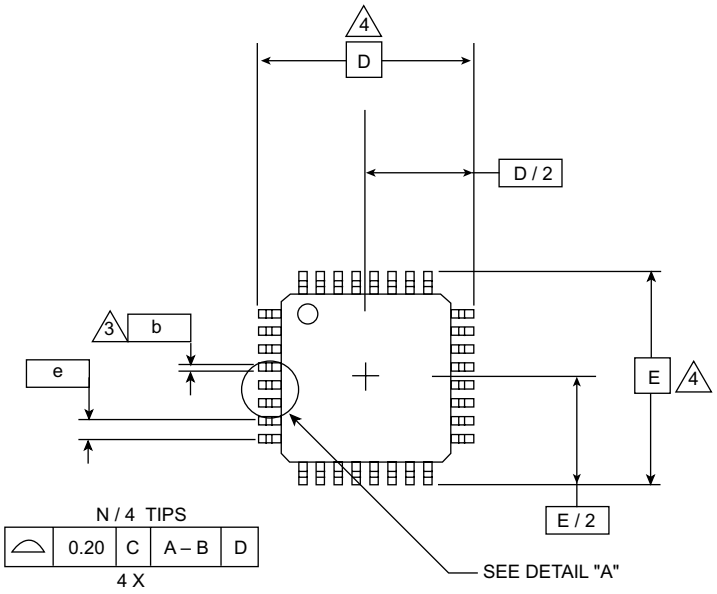


Figure 10. Dispersion Measurement Conditions

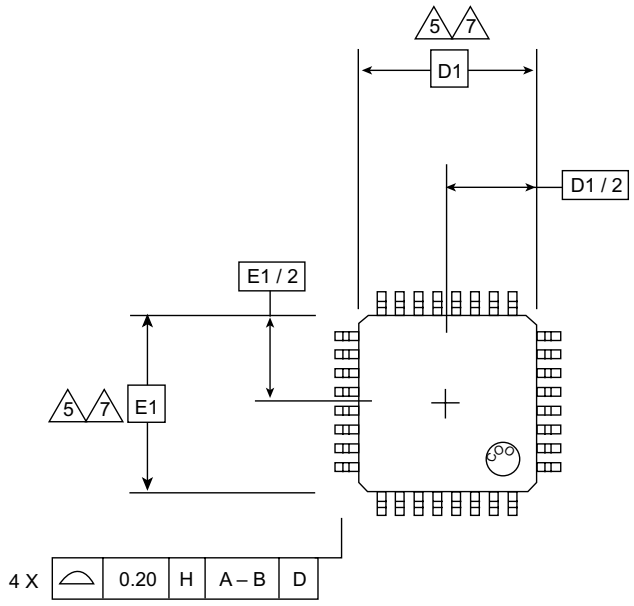
Package Information

32-Pin TQFP
7 mm x 7 mm

TOP VIEW

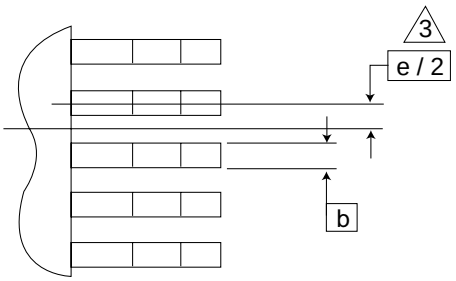


BOTTOM VIEW

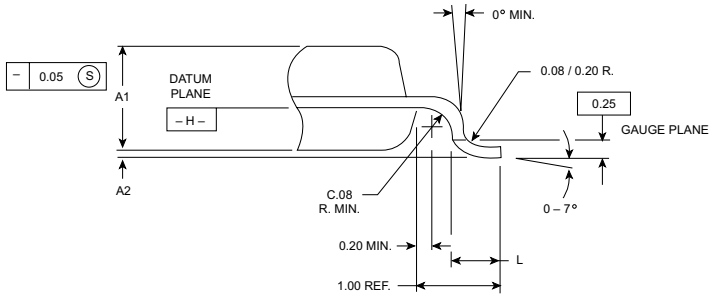


Package Information *(continued)*

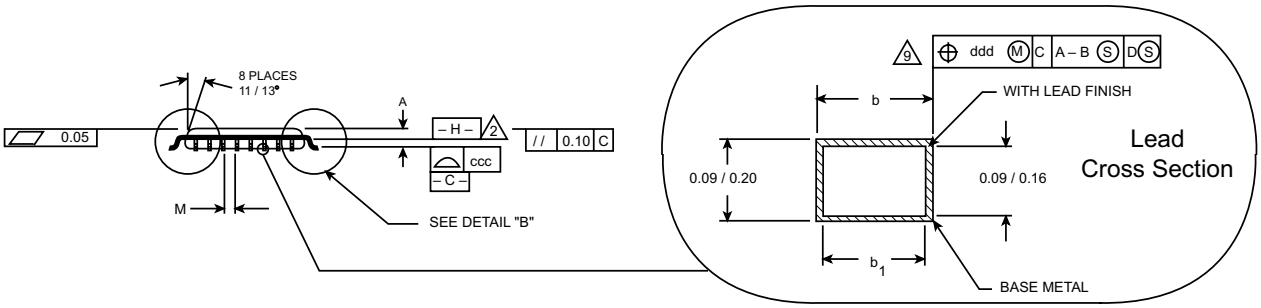
DETAIL "A"



DETAIL "B"



SECTION C–C



Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion.
6. "N" is the total # of terminals.
7. These dimensions to be determined at the datum plane -H-.
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.30 millimeters.
12. This outline conforms to JEDEC publication 95, registration MO-136, variations AC, AE, and AF.

JEDEC VARIATION

AC				
Sym	**Min**	**Nom**	**Max**	**Note**
A			1.60	
A1	0.05	0.10	0.15	
A2	1.35	1.40	1.45	
D		9.00 BSC		4
D1		7.00 BSC		7, 8
E		9.00 BSC		4
E1		7.00 BSC		7, 8
L	0.45	0.60	0.75	
M	0.15			
N		32		
e		0.80 BSC		
b	0.30	0.37	0.45	9
b1	0.30	0.35	0.40	
ccc			0.10	
ddd			0.20	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	8.5	11.5	12.0	V
Negative Power Supply	VEE	-8.5	-5.2	-4.5	V
Total Analog Supply	VCC - VEE	13.0	16.7	17.0	V
Comparator Output Positive Supply	PECL	0	3.3	5.0	V
Junction Temperature	TJ			+110	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Positive Supply (Relative to GND)	VCC	0		+13.0	V
Negative Supply (Relative to GND)	VEE	-9.0		0	V
Total Power Supply	VCC - VEE			+20.0	V
Comparator Output Positive Supply	PECL	0		+6.0	V
Digital Input Voltages	LDEN, LDEN*	VEE		+6.0	V
Differential Digital Input Voltages	LDEN - LDEN*	-5.0		+5.0	V
Digital Output Currents	QA, QA*, QB, QB*	0		50	mA
Comparator Input to Threshold	VINP - CVA	-13		+13	V
	VINP - CVB	-13		+13	V
Load to Commutating Voltage	LOAD - VCMIN	-10		+10	V
Analog Voltages	VCMIN	VEE		VCC	V
	LOAD, VINP	VEE		VCC	V
	CVA, CVB	VEE		VCC	V
	BRIDGE SOURCE	VEE		VCC	V
	BRIDGE SINK	VEE		VCC	V
Analog Input Currents	ISCIN	0		2.0	mA
	ISKIN	0		2.0	mA
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Process Temperature (< 30 hours)				+160	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Load					
Commutating Voltage					
Differential Load Range	LOAD - VCMIN	-6.0		+6.0	V
Programmable Range	VCMIN	VEE + 2.9		VCC - 2.9	V
Offset Voltage	VCOUT - VCMIN	-100		+100	mV
VCMIN Input Current		-100	5	+100	µA
Accuracy					
ISC Offset (Note 1)		+4	+100	+150	µA
ISK Offset (Note 1)		-150	-100	+4	µA
Gain (sourcing current)	ILOAD / ISCIN	35	37	40	
Gain (sinking current)	ILOAD / ISKIN	35	39	42	
Input Currents		0		.875	mA
Linearity (Note 2)	INL	-600		+600	µA
HiZ Leakage (LDEN = False) (Note 3)		-1	±.1	+1	µA
Output Impedance (Note 4)	ROUT	5.0	7.5	15	Ω
Digital Inputs	LDEN, LDEN*				
Input Current		-500		+500	µA
Input Voltage Range		0.0		+3.5	V
Differential Input Swing		0.25		+3.0	V
Programming Current Input Voltage Compliance (Note 5)	V_ISKIN, V_ISCIN	-100		+100	mV

DC test conditions (unless otherwise specified): "Recommended Operating Conditions".

Note 1: Offset is measured with ISCIN or ISKIN equal to 6 µA, producing an absolute output current of 100 µA nominal.

Note 2: Error = Measured IOUT vs. calculated IOUT. Calculated IOUT = (I * LSB) + Offset.
LSB = (Fullscale – Offset) / 9. I = Index = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

Index	ISCIN, ISKIN
0	6 µA
1	100 µA
2	200 µA
3	300 µA
4	400 µA
5	500 µA
6	600 µA
7	700 µA
8	800 µA
9	900 µA

Note 3: Tested @
1) LOAD = –3V, VCMIN = +3V
2) LOAD = +6.5V, VCMIN = +0.5V.

Note 4: Tested @ LOAD = +2V, IOUT = 5 mA and 15 mA.

Note 5: Tested @ ISCIN, ISKIN = 6 µA, 50 µA, 100 µA, 875 µA.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Comparator					
Threshold voltage	CVA, CVB	VEE + 2.9		VCC - 2.9	V
Input Voltage Range	VINP	VEE + 2.9		VCC - 2.9	V
Input Differential Voltage	VINP - CVA, B	-11		+11	V
Threshold Input Current		-50		+50	µA
IPD Pin Input Current		-150		+10	µA
VINP Input Current					
Normal Operation IPD = 0 (Note 1)	IBIAS	-1		+1	µA
VINP = VCC - 2.9V, CVA,B = VCC - 13.9V	IBIAS	-3		+3	µA
VINP = VEE + 2.9V, CVA,B = VEE + 13.9V	IBIAS	-3		+3	µA
Offset Voltage	VOS	-50		+50	mV
Common Mode Rejection Ratio	CMRR		60		dB
Power Supply Rejection Ratio	PSRR		60		dB
Comparator Hysteresis			4		mV
Digital Output Swing	|QA - QA*|	600	700	1,000	mV
	|QB - QB*|	600	700	1,000	mV
Common Mode Voltage	(QA + QA*) / 2	PECL - 1.5		PECL - 1.1	V
	(QB + QB*) / 2	PECL - 1.5		PECL - 1.1	V
Power Supply (Load + Comp)					
Positive Supply Current	ICC	35	50	75	mA
Negative Supply Current	IEE	55	75	95	mA
PECL Supply Current	IDD	35	55	90	mA

DC test conditions (unless otherwise specified): "Recommended Operating Conditions".

Note 1: Tested @ VINP = +7.0V and –1.0V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Load					
Propagation Delay					
Inhibit to Iout (Note 2)	Tpd (on)	1.0	3.0	5.0	ns
Iout to Inhibit (Note 2)	Tpd (off)	1.0	3.0	5.0	ns
Output Capacitance					
Load Active	Cout		5.5		pf
Load Off	Cout		2.5		pF
Comparator					
Propagation Delay (Notes 1, 2)	Tpd	1.0	2.0	4.0	ns
Propagation Delay Dispersion (Note 2)					
800 mV		-100	<±25	+100	ps
3V		-100	<±25	+100	ps
5V		-100	<±25	+100	ps
Input Slew Rate Tracking (Note 2)					
IPD = 0		5.0	6.0		V/ns
IPD = 1		25			mV/ns
Input Capacitance	Cin		1.5		pF
Output Rise and Fall Times (20% to 80%)	Tr, Tf		250		ps
Minimum Pulse Width (Note 2)				1.5	ns

DC test conditions (unless otherwise specified): "Recommended Operating Conditions".

Note 1: Assumes normal operating mode of IPD = 0.
Note 2: Guaranteed by characterization. This parameter is not production tested.

Ordering Information

Model Number	Package
E672BTF	32-Pin 7mm x 7mm TQFP
EVM672BTF	Evaluation Module

Contact Information

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Phone: (858)695-1808 FAX (858)695-2633