

DESCRIPTION

The HY51V4800B is the new generation and fast dynamic RAM organized 524,288 x 8-bits. The HY51V4800B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY51V4800B to be packaged in a 400 mil 28 pin plastic SOJ, TSOP-II, and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated-test equipments. System oriented-feature includes single power supply of 3.3V $\pm$ 10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
- Max. battery back-up 0.72mW(L-part)
Max. CMOS standby 0.54mW(L-part)
3.6mW

Max. TTL standby 3.6mW

Max. Self refresh 0.72mW(SL-part)

Max. operating

Speed	Power
60	360.0mW
70	306.0mW
80	270.0mW

- Single power supply of 3.3V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

Speed	t _{TRC}	t _{CAC}	t _{PC}
60	60ns	15ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	50ns

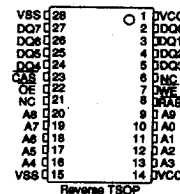
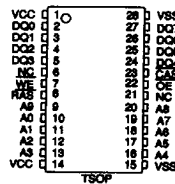
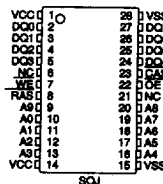
- Fast page mode operation
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden & Self refresh
- 1024 refresh cycles / 128ms(L-part)
1024 refresh cycles / 16ms

PIN DESCRIPTION

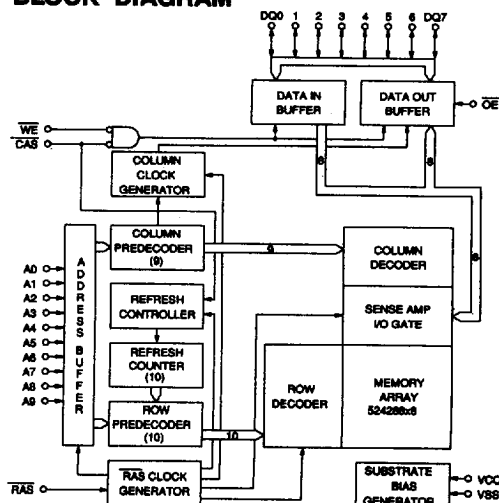
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A9*	Address Input
DQ0-DQ7	Data Input/Output
Vcc	Power (+ 3.3V)
Vss	Ground

*A9 is applied to Row address input only.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-0.5 to 4.6	V
VCC	Voltage on Vcc Relative to Vss	-0.5 to 4.6	V
Ios	Short Circuit Output Current	20	mA
Pd	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	3.0	3.3	3.6	V
VIH	Input High Voltage	2.0	-	VCC+ 0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS≤ VIN≤ 6.5V, All other pins not under test= VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS≤ VOUT≤ 5.5V RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trC= trC (min.)	60 70 80	- - -	100 85 75	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	1	mA	
ICC3	VCC Supply Current, RAS-only refresh	trC= trC (min.)	60 70 80	- - -	100 85 75	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpC= tpC (min.)	60 70 80	- - -	45 40 35	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	L-Part	-	1 0.15	mA	
ICC6	VCC Supply Current, CAS-before-RAS refresh	trC= trC (min.)	60 70 80	- - -	100 85 75	mA	1,3
ICC7	VCC Supply Current, Battery back Up (L-part only)	trC = 125μs, tRAS ≤ 1μs CAS= CBR cycling or 0.2V OE & WE = VCC-0.2V or 0.2V A0-A9 = VCC-0.2V or 0.2V DQ0-7 = 0.2V, VCC-0.2V or open		-	200	μA	1,4,5
ICC8	VCC Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as ICC7		-	200	μA	6
VOL	Output Low Voltage	IOL= 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH= -2.0mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, and ICC6 depend on cycle rate.
2. ICC1, ICC3, ICC4 and ICC6 are dependent on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. ICC1, ICC3, ICC6, Address can be changed maximum two times while RAS= VIL. ICC4, Address can be changed maximum once while CAS= VIH.
4. Only tRAS(max.) = 1μs is applied to refresh of battery backup but tRAS(max.) = 10 μs is applied to normal functional operation.
5. ICC5(max.) = 0.15mA and ICC7 are applied to applied L-parts (HY51V4800BLJC, HY51V4800BLTC, HY51V4800BLRC, HY51V4800BSLJC, HY51V4800BSLTC, and HY51V4800BSLRC).
6. ICC8 is applied to SL-parts only (HY51V4800BSLJC, HY51V4800BSLTC and HY51V4800BSLRC).

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3,13

HY51V4800BJC/BTC/BRC/BLJC/BLTC/BLRC/BSLJC/BSLTC/BSLRC										
#	SYMBOL	PARAMETER	-60		-70		-80		UNIT	NOTE
			MAX.	MIN.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	170	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	40	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	80	-	105	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4,15
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	RAS Hold Time	15	-	20	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	15	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	17
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	14
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	14
32	tWCR	Write Command Hold Time from RAS	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	20	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	20	-	20	-	20	-	ns	16
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	12
		L-part	-	128	-	128	-	128	ms	11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8,14

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY51V4800BJC/BTC/BRC/BLJC/BLTC/BLRC BSLJC/BSLTC/BSLRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	35	-	40	-	40	-	ns	8
42	tRWD	RAS to WE Delay Time	85	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	55	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	14
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	14
47	tCPT	CAS Precharge Time(CBR Counter Test)	30	-	35	-	40	-	ns	17
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	-	15	-	20	-	20	ns	
50	tOED	OE to Data Delay	15	-	20	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	20	0	20	ns	5
52	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	40	-	40	-	50	-	ns	
55	tRASS	RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	μs	
56	tRPS	RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
57	tCHS	CAS Hold Time from RAS (Self Refresh)	-50	-	-50	-	-50	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HY51V4800B could begin an active cycle. These condition results in higher than necessary current demands from the power supply during power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.
4. Measured at VOH= 2.0V and VOL= 0.8V with a load equivalent to 2 TTL loads and 100pF.
5. tOFF(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edges in early write cycles and to WE leading edge in Read-Modify-Write cycles.
8. twCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS $\geq$ twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD $\geq$ tRWD(min.), tCWD $\geq$ tCWD(min.), tAWD $\geq$ tAWD(min.), and tCPWD $\geq$ tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)= 128ms is applied to L-Parts (HY51V4800BLJC/BSLJC, HY51V4800BLTC/BSLTC and HY51V4800BLRC/BSLRC).
12. A burst of 1024CAS-before-RAS refresh cycles must be executed within 16ms(128ms for L-part) after exiting self refresh.
13. When CAS goes low, all 8-bits data are written into the device.
14. These parameters are determined by the earlier falling edge of CAS.
15. These parameters are determined by the later rising edge of CAS.
16. tcWL must be satisfied by CAS for 8-bits access cycles.
17. tCP and tCPT are measured when CAS is high state.

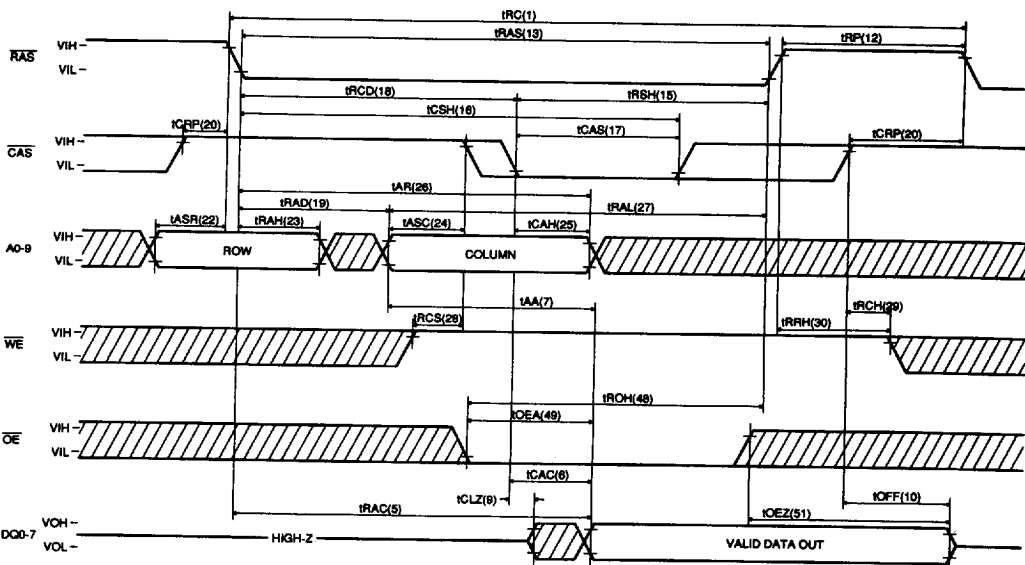
CAPACITANCE

(TA= 25°C, VCC= 5V $\pm$ 10%, VSS= 0V, f= 1MHz, unless otherwise noted.)

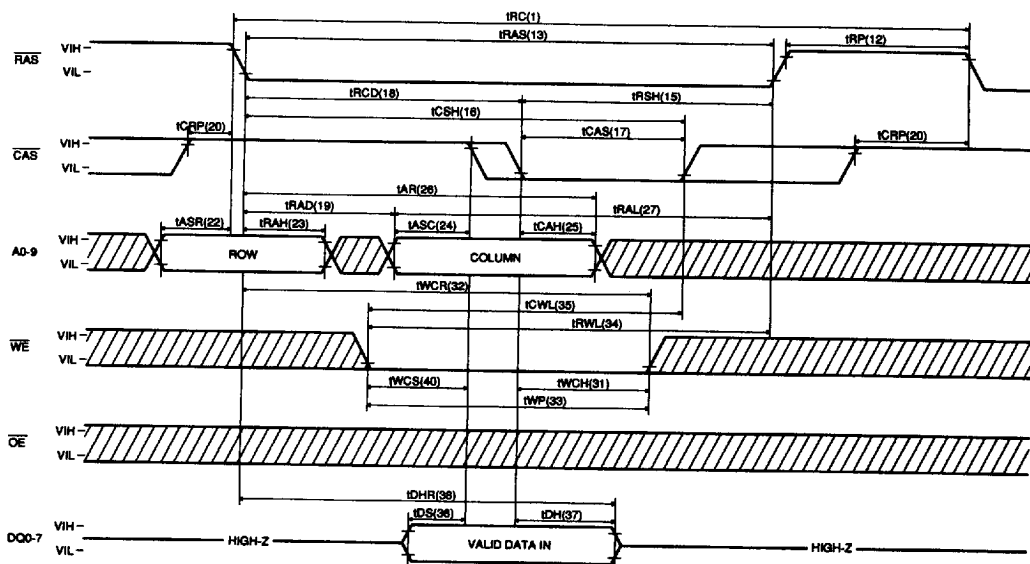
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	5	pF
CIN2	Input Capacitance (RAS, CAS, WE, OE)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ7)	-	7	pF

TIMING DIAGRAM

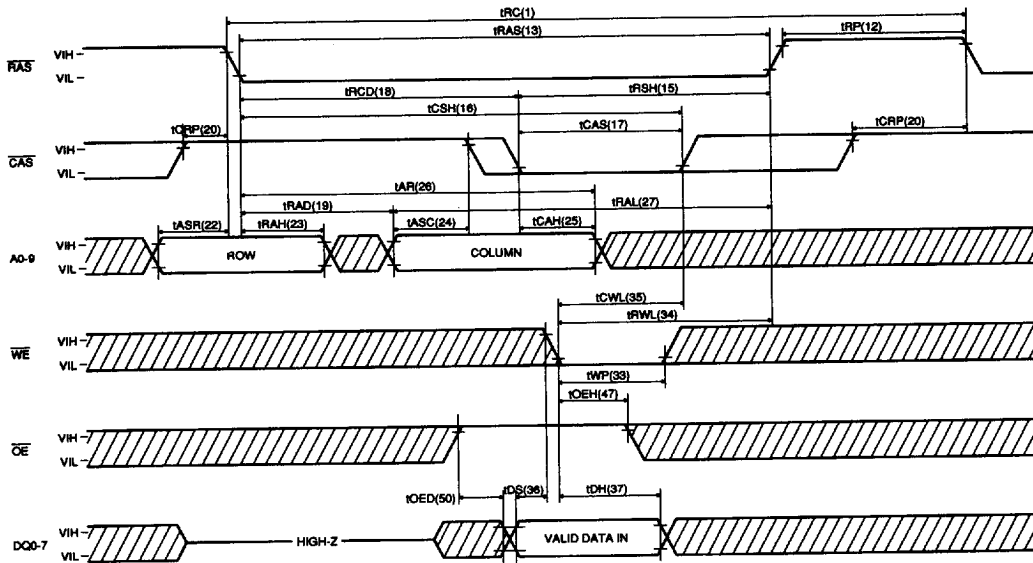
READ CYCLE



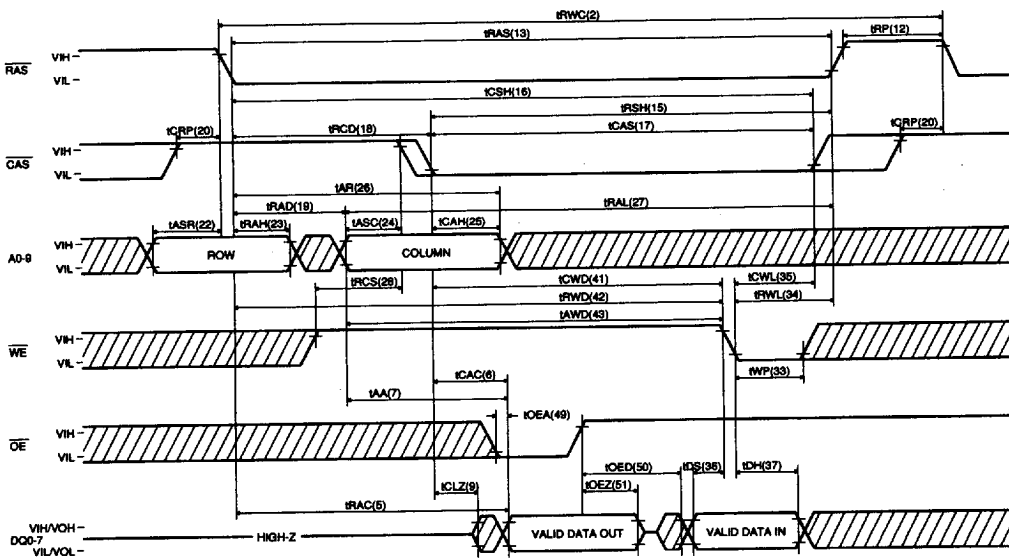
EARLY WRITE CYCLE



WRITE CYCLE (OE CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



The timing diagram illustrates the relationship between the 64K1602 LCD controller and the 64K1601 LCD panel. The signals shown are:

- RAS**: Row Address Strobe, with parameters $t_{RASP}(14)$ and $t_{RSH}(15)$.
- CAS**: Column Address Strobe, with parameters $t_{RCD}(18)$, $t_{CAS}(17)$, $t_{CP}(21)$, $t_{RSH}(15)$, $t_{CAS}(17)$, $t_{CP}(21)$, $t_{RSH}(15)$, and $t_{CRP}(20)$.
- A0-9**: Address bus, with parameters $t_{ASR}(22)$, $t_{RAH}(23)$, $t_{ASC}(24)$, $t_{CAH}(25)$, $t_{ASC}(24)$, $t_{CAH}(25)$, $t_{ASC}(24)$, $t_{CAH}(25)$, and $t_{RAL}(27)$.
- WE**: Write Enable, with parameters $t_{RCS}(28)$, $t_{AA}(7)$, $t_{RCH}(29)$, $t_{RCS}(28)$, $t_{RCH}(29)$, $t_{RCS}(28)$, $t_{RCH}(29)$, and $t_{RRH}(30)$.
- OE**: Output Enable, with parameters $t_{RAC}(5)$, $t_{CAC}(6)$, $t_{IOEA}(48)$, $t_{CAC}(6)$, $t_{IOEA}(49)$, $t_{CAC}(6)$, $t_{IOEA}(48)$, and $t_{IOEA}(48)$.
- DQ0-7**: Data bus, with parameters $t_{CLZ}(9)$, $t_{OFF}(10)$, $t_{OEZ}(51)$, $t_{CLZ}(9)$, $t_{OFF}(10)$, $t_{OEZ}(51)$, $t_{CLZ}(9)$, and $t_{OFF}(10)$.

The diagram shows the timing of these signals relative to each other, with shaded areas indicating the valid data period and the timing of the address and control signals.

[illegible]

The timing diagram illustrates the relationship between various signals and their durations for the 64K1602 device. The signals and their durations are as follows:

- RAS:** $t_{RSP}(12)$, $t_{RSH}(15)$, $t_{RCD}(18)$, $t_{RAS}(17)$, $t_{RCP}(20)$
- CAS:** $t_{CAS}(17)$, $t_{CWD}(41)$, $t_{CWL}(35)$, $t_{CWP}(33)$
- A0-9:** $t_{A0-9}(22)$, $t_{A0-9}(24)$, $t_{A0-9}(25)$, $t_{A0-9}(27)$
- WE:** $t_{WE}(28)$, $t_{WE}(34)$, $t_{WE}(35)$
- OE:** $t_{OE}(49)$, $t_{OE}(50)$, $t_{OE}(51)$
- IO:** $t_{IO}(37)$, $t_{IO}(38)$, $t_{IO}(39)$

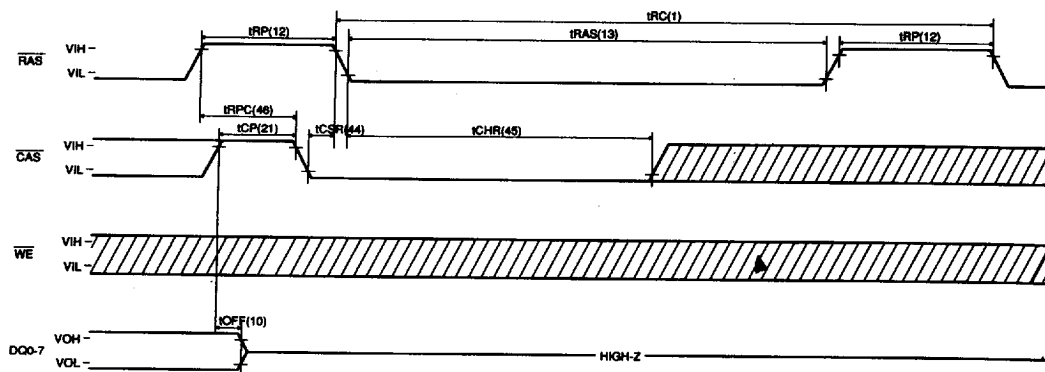
The diagram also shows the timing of the data bus signals (VH/VOL, VIL/VOL) and the output signals (OUT, IN) relative to the clock signals (RAS, CAS, WE, OE).

The diagram illustrates the timing relationships for RAS, CAS, and A0-A9 signals. The RAS signal is shown with a high pulse and a low pulse. The CAS signal is shown with a high pulse and a low pulse. The A0-A9 signal is shown as a shaded block labeled 'ROW'. The timing parameters are defined as follows:

- $t_{RC}(1)$: RAS to CAS delay
- $t_{RAS}(13)$: RAS pulse width
- $t_{RP}(12)$: RAS precharge time
- $t_{CRP}(20)$: CAS to RAS precharge time
- $t_{RPC}(46)$: RAS precharge to CAS delay
- $t_{ASR}(22)$: A0-A9 setup time
- $t_{RAH}(23)$: A0-A9 hold time

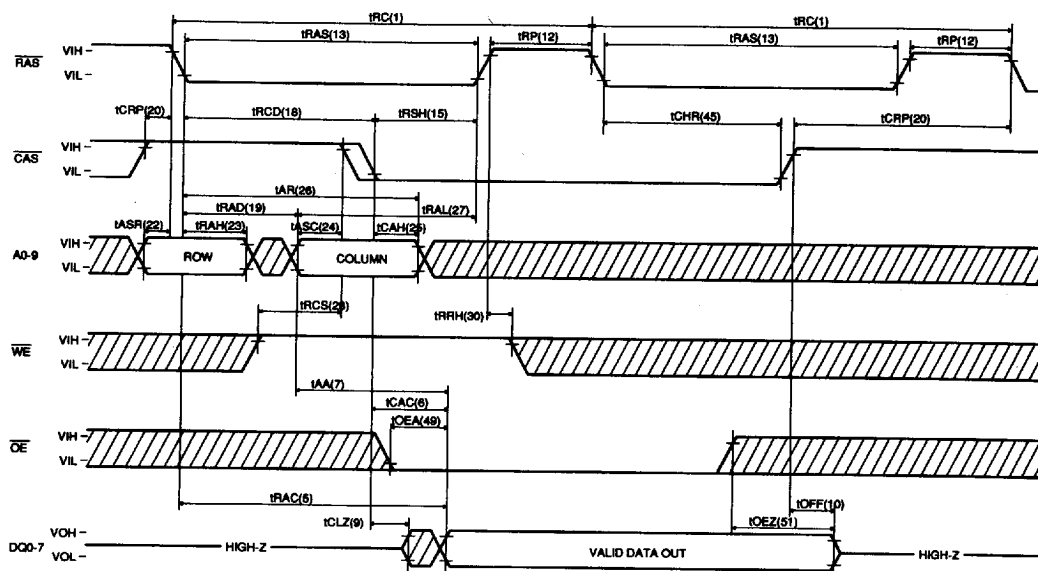
NOTE : OE and WE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

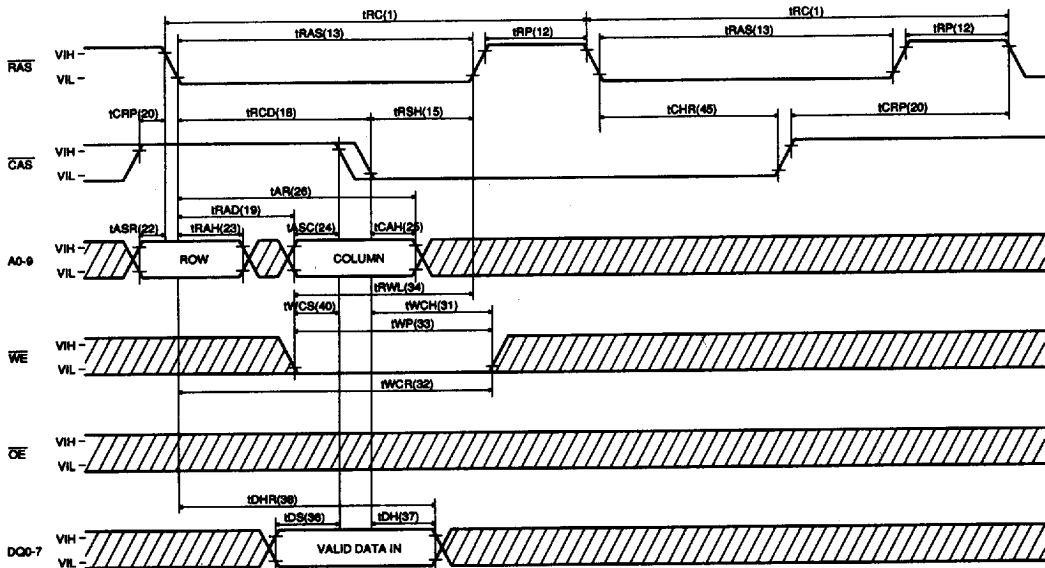


NOTE : A0-9 and OE = "H" or "L"

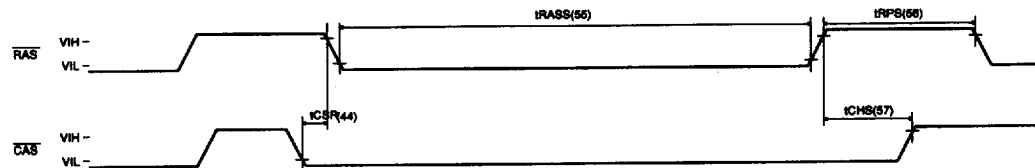
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

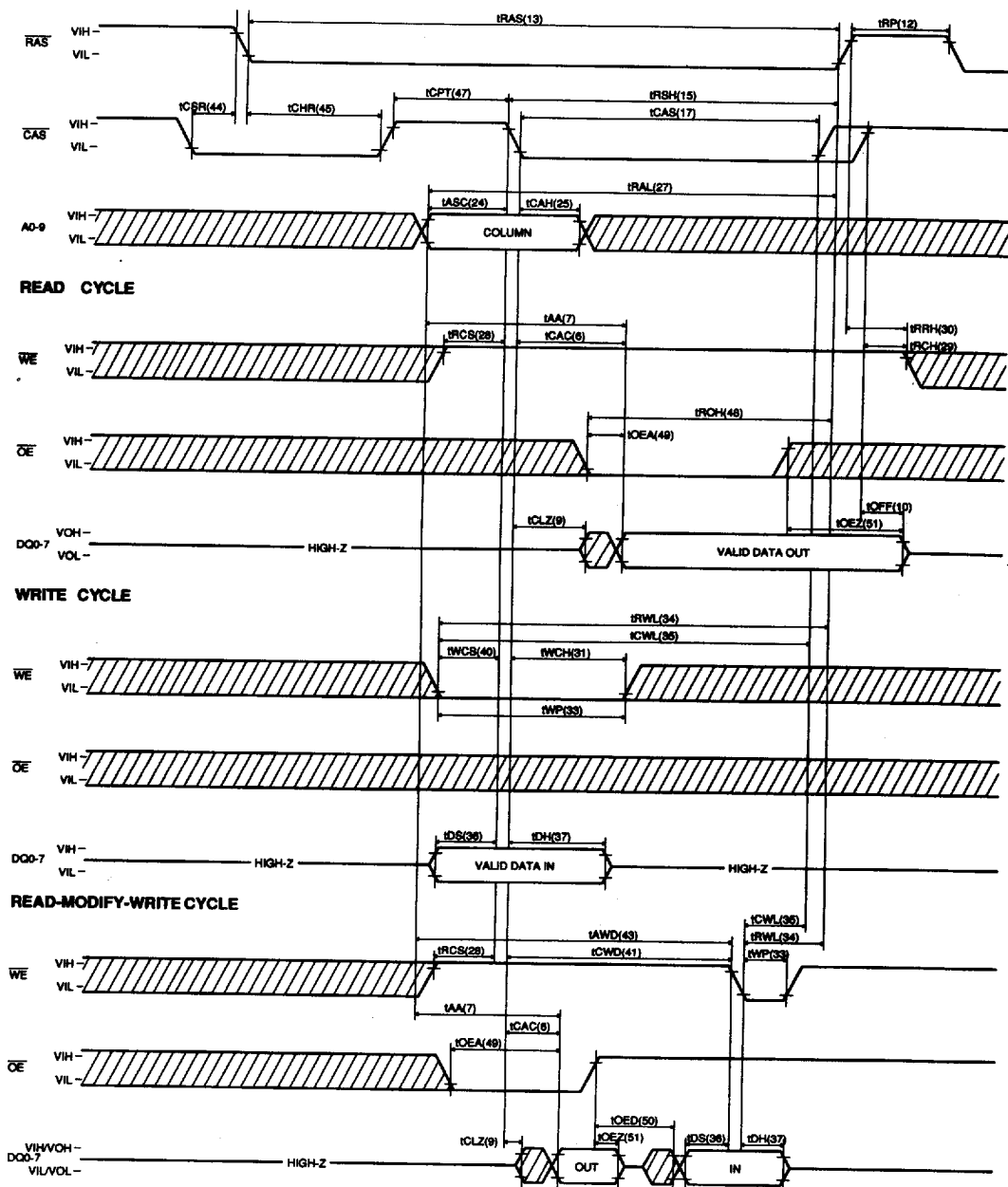


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-9, $\overline{WE}$ and $\overline{OE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



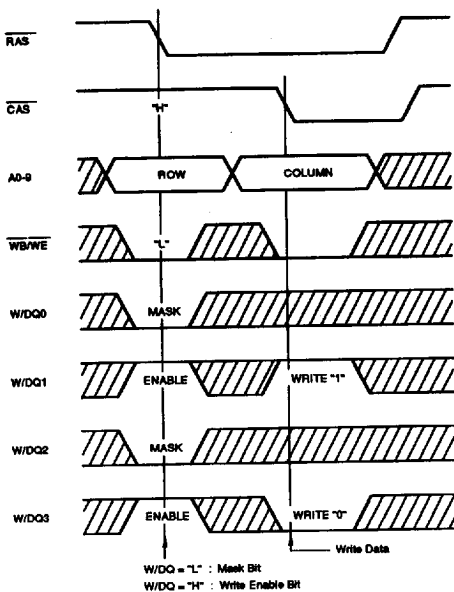
WRITE-PER-BIT FUNCTION

The Write-Per-Bit function selectively controls the internal write enable circuit of the HY51V4810B. When **WB/WE** is held "Low" at the falling edge of **RAS** during a random access operation, the write mask is enabled. At the same time, the mask data on the **W/DQ** pins is located onto the write mask register (WMR). When a "0" is sensed on any of the **W/DQ** pins, their corresponding write circuits are disabled and new data will not be written. When "1" is sensed on any of the **W/DQ** pins, their corresponding write circuit will remain enabled so that new data is written. The truth table of the Write-Per-Bit function and an example of the Write-Per-Bit function illustrating its application to displays are shown below.

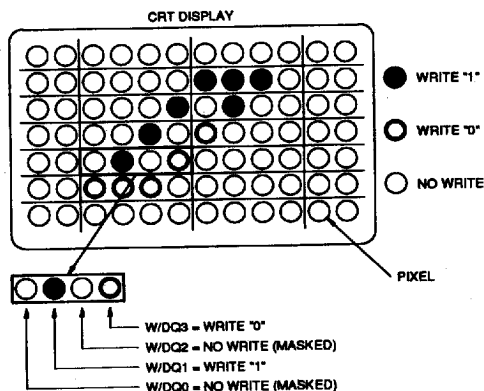
TRUTH TABLE FOR WRITE-PER-BIT FUNCTION

at the falling edge of RAS			Function
CAS	WB/WE	W/DQ0-7	
H	H	Don't Care	Write Enable
H	L	1	Write Enable
		0	Write Mask

WRITE-PER-BIT TIMING DIAGRAM

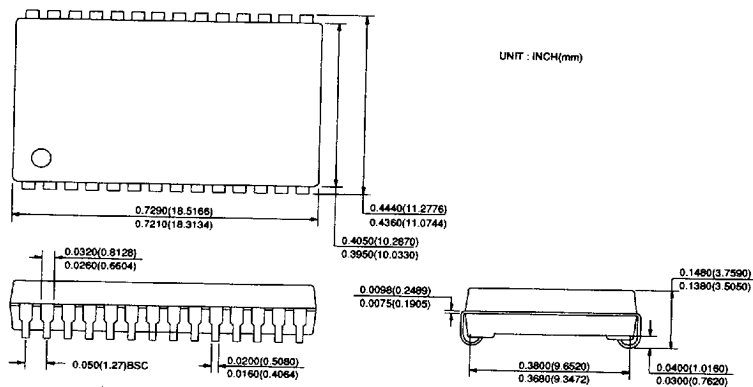


CORRESPONDING BIT MAP

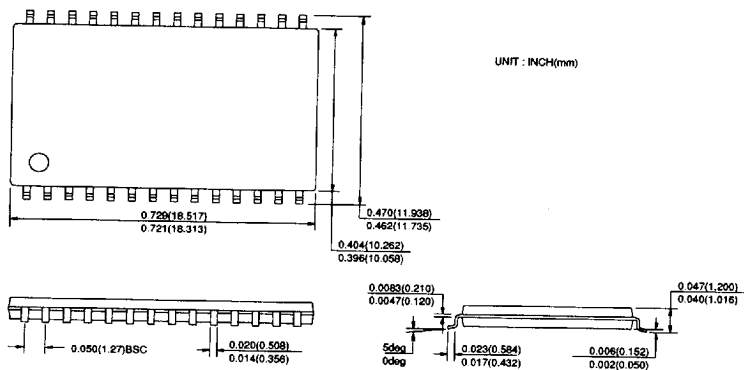


PACKAGE INFORMATION

400mil 28pin Small Outline J-form Package (JC)



400mil 28pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY51V4800BJC	60/70/80		SOJ
HY51V4800BSLJC	60/70/80	L-part	SOJ
HY51V4800BSLJC	60/70/80	SL-part	SOJ
HY51V4800BTC	60/70/80		TSOP-II
HY51V4800BLTC	60/70/80	L-part	TSOP-II
HY51V4800BSLTC	60/70/80	SL-part	TSOP-II
HY51V4800BRC	60/70/80		TSOP-II(R)
HY51V4800BLRC	60/70/80	L-part	TSOP-II(R)
HY51V4800BSLRC	60/70/80	SL-part	TSOP-II(R)