SIEMENS

4M x 16-Bit Dynamic RAM
(8k, 4k & 2k Refresh)

HYB 3164160AT(L) -40/-50/-60
HYB 3165160AT(L) -40/-50/-60
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Advanced Information

- 4 194 304 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast Page Mode operation
- Performance:

		-40	-50	-60	
t_{RAC}	$\overline{RAS}$ access time	40	50	60	ns
t_{CAC}	$\overline{CAS}$ access time	10	13	15	ns
t_{AA}	Access time from address	20	25	30	ns
t_{RC}	Read/write cycle time	75	90	110	ns
t_{PC}	Fast page mode cycle time	30	35	40	ns

- Single + 3.3 V (± 0.3V) power supply
- Low power dissipation:

	-40	-50	-60	
HYB3166160AT(L)	900	558	396	mW
HYB3165160AT(L)	756	468	324	mW
HYB3164160AT(L)	612	378	270	mW

  7.2 mW standby (TTL)
  3.24 mW standby (MOS)
  720 µW standby for L-version
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR), $\overline{RAS}$-only refresh, hidden refresh and self refresh (L-version only)
- 2 $\overline{CAS}$ / 1 $\overline{WE}$ byte control
- 8192 refresh cycles /128 ms , 13 R/ 9C addresses (HYB 3164160AT)
  4096 refresh cycles / 64 ms , 12 R/ 10C addresses (HYB 3165160AT)
  2048 refresh cycles / 32 ms , 11 R/ 11C addresses (HYB 3166160AT)
- 256 msec refresh period for L-versions
- Plastic Package: P-TSOPII-50 400 mil

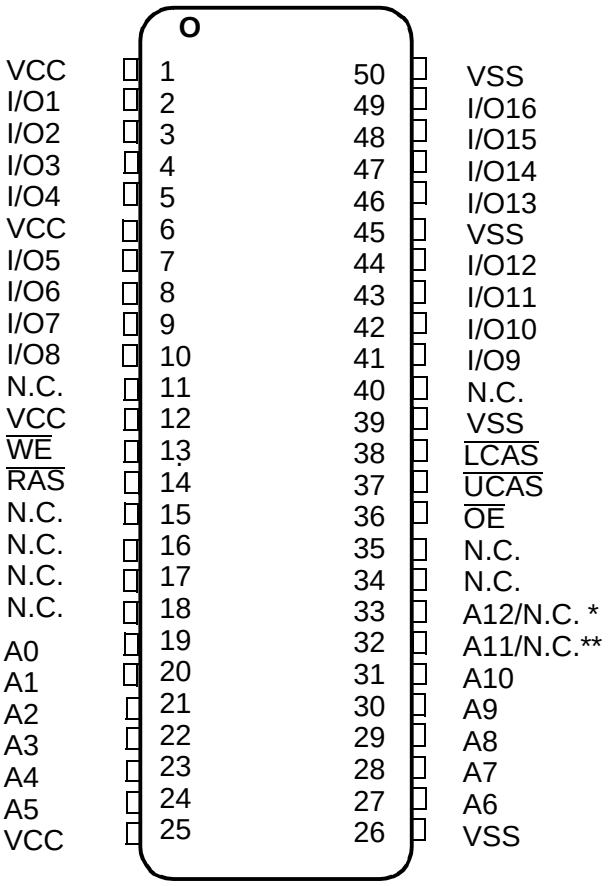
This device is a 64 MBit dynamic RAM organized 4 194 304 by 16 bits. The device is fabricated on an advanced second generation 64Mbit 0,35µm-CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. This DRAM operates with a single 3.3 +/-0.3V power supply and interfaces with either LVTTL or LVCMOS levels. Multiplexed address inputs permit the HYB 3164(5)160AT to be packaged in a 400 mil wide TSOP-50 package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. The HYB3164(5/6)160ATL parts (L-version) have a very low power „sleep mode“ supported by Self Refresh.

Ordering Information

Type	Ordering Code	Package		Descriptions
8k-refresh versions:				
HYB 3164160AT-40		P-TSOPII-50	400 mil	DRAM (access time 40 ns)
HYB 3164160AT-50		P-TSOPII-50	400 mil	DRAM (access time 50 ns)
HYB 3164160AT-60		P-TSOPII-50	400 mil	DRAM (access time 60 ns)
HYB 3164160ATL-50		P-TSOPII-50	400 mil	DRAM (access time 50 ns)
HYB 3164160ATL-60		P-TSOPII-50	400 mil	DRAM (access time 60 ns)
4k-refresh versions:				
HYB 3165160AT-40		P-TSOPII-50	400 mil	DRAM (access time 40 ns)
HYB 3165160AT-50		P-TSOPII-50	400 mil	DRAM (access time 50 ns)
HYB 3165160AT-60		P-TSOPII-50	400 mil	DRAM (access time 60 ns)
HYB 3165160ATL-50		P-TSOPII-50	400 mil	DRAM (access time 50 ns)
HYB 3165160ATL-60		P-TSOPII-50	400 mil	DRAM (access time 60 ns)
2k-refresh versions:				
HYB 3166160AT-40		P-TSOPII-50	400 mil	DRAM (access time 40 ns)
HYB 3166160AT-50		P-TSOPII-50	400 mil	DRAM (access time 50 ns)
HYB 3166160AT-60		P-TSOPII-50	400 mil	DRAM (access time 60 ns)
HYB 3166160ATL-50		P-TSOPII-50	400 mil	DRAM (access time 50 ns)
HYB 3166160ATL-60		P-TSOPII-50	400 mil	DRAM (access time 60 ns)

Pin Configuration

P-TSOPII-50 (400 mil)



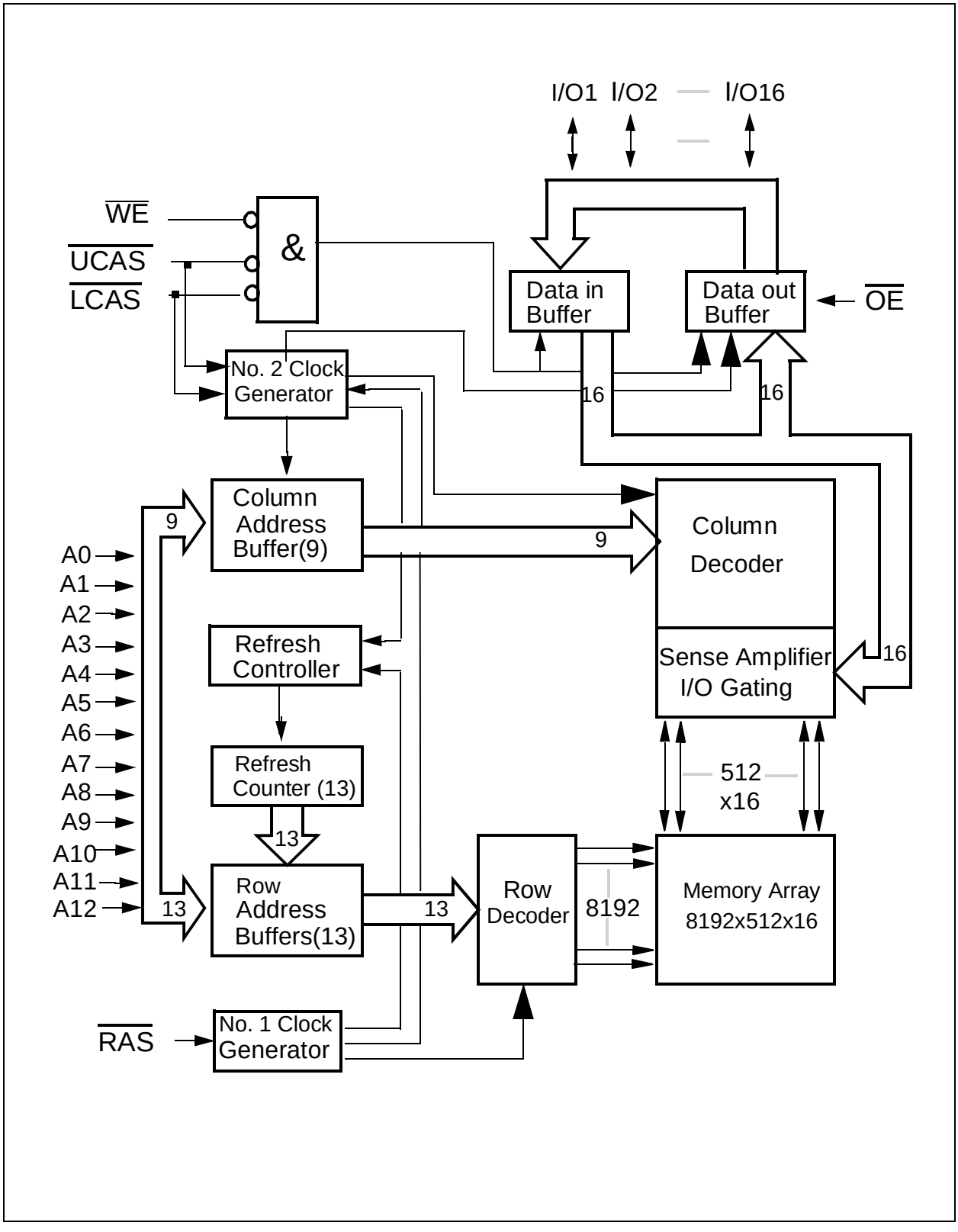
* Pin 33 is A12 for HYB 3164160AT(L) and N.C. for HYB 3165(6)160AT(L)
** Pin 32 is A11 for HYB 3164(5)160AT(L) and N.C. for HYB 3166160AT(L)

Pin Names

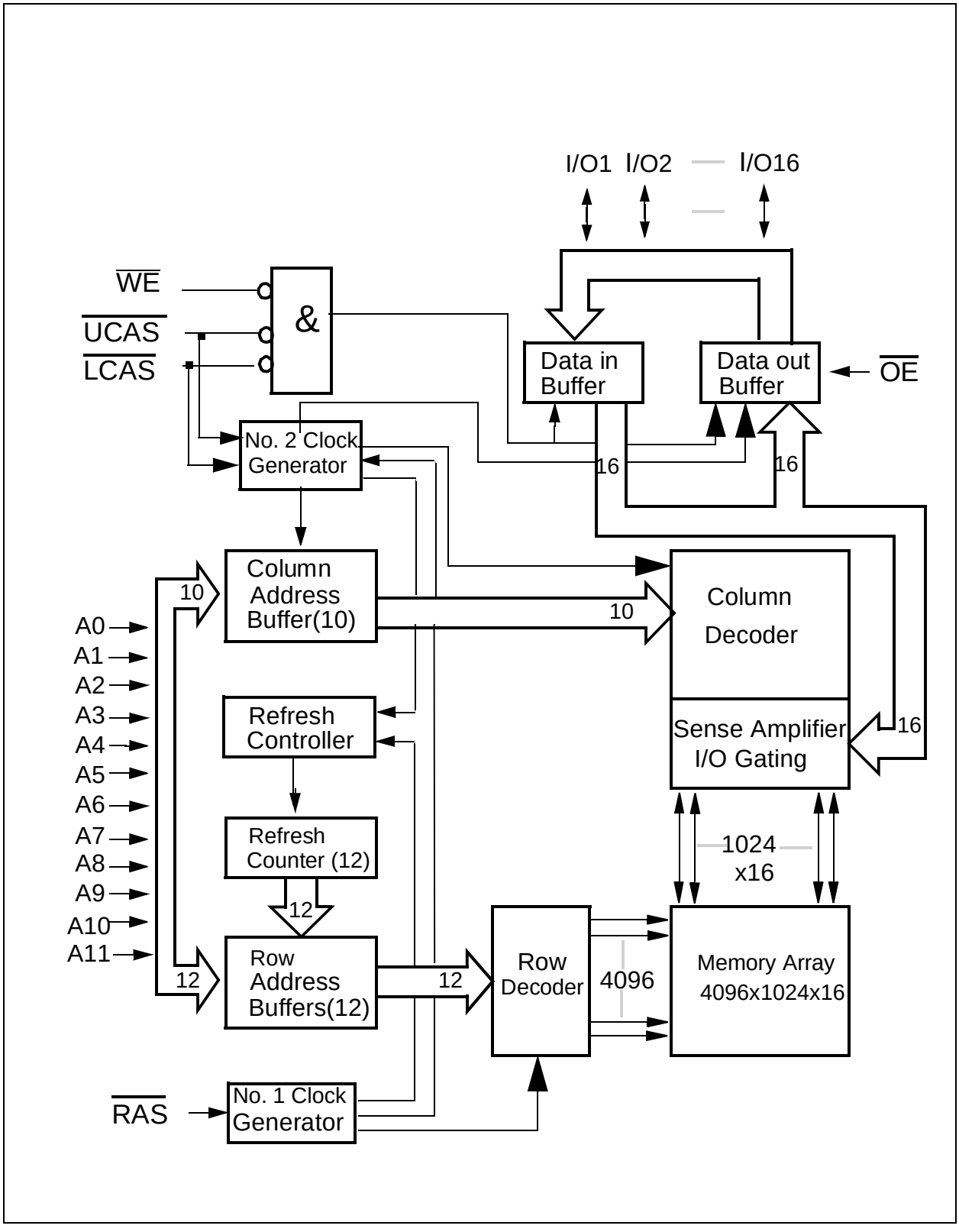
A0-A12	Address Inputs for 8k-refresh version HYB 3164160AT(L)
A0-A11	Address Inputs for 4k-refresh version HYB 3165160AT(L)
A0-A10	Address Inputs for 2k-refresh version HYB 3166160AT(L)
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$,$\overline{LCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
Vcc	Power Supply (+ 3.3V)
Vss	Ground

TRUTH TABLE

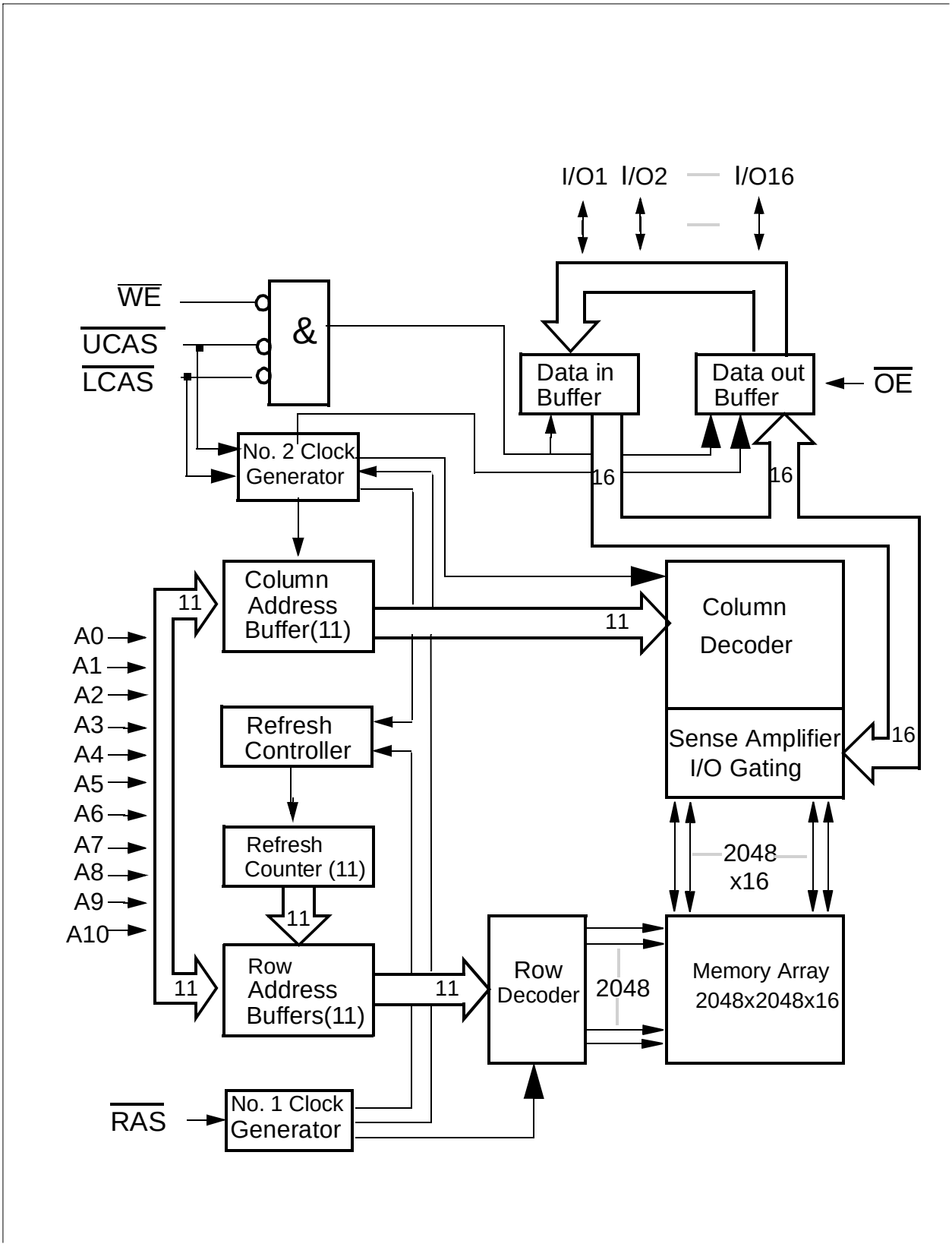
FUNCTION		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	ROW ADD	COL ADD	I/O1-I/O16
Standby		H	H - X	H - X	X	X	X	X	High Impedance
Read:Word		L	L	H	H	L	ROW	COL	Data Out
Read:Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte:Data Out Upper-Byte:High-Z
Read:Upper Byte		L	H	L	H	L	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out
Write:Word (Early-Write)		L	L	L	L	X	ROW	COL	Data In
Write:Lower Byte (Early-Write)		L	L	H	L	X	ROW	COL	Lower Byte:Data Out Upper-Byte:High-Z
Write:Upper Byte (Early Write)		L	H	L	L	X	ROW	COL	Lower Byte:High-Z Upper Byte:Data Out
Read-Modify-Write		L	L	L	H - L	L - H	ROW	COL	Data Out, Data In
Fast Page Mode Read (Word)	1st Cycle	L	H - L	H - L	H	L	ROW	COL	Data Out
Fast Page Mode Read (Word)	2nd Cycle	L	H - L	H - L	H	L	n/a	COL	Data Out
Fast Page Mode Early Write(Word)	1st Cycle	L	H - L	H - L	L	X	ROW	COL	Data In
Fast Page Mode Early Write(Word)	2nd Cycle	L	H - L	H - L	L	X	n/a	COL	Data In
Fast Page Mode RMW	1st Cycle	L	H - L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
Fast Page Mode RMW	2st Cycle	L	H - L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
RAS only refresh		L	H	H	X	X	ROW	n/a	High Impedance
CAS-before-RAS refresh		H - L	L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	L	X	X	n/a	High Impedance
Hidden Refresh (Read)		L-H-L	L	L	H	L	ROW	COL	Data Out
Hidden Refresh (Write)		L-H-L	L	L	L	X	ROW	COL	Data In



Block Diagram for HYB 3164160AT(L)



Block Diagram for HYB 3165160AT(L)



Block Diagram for HYB 3166160AT(L)

Absolute Maximum Ratings

Operating temperature range.....0 to 70 °C

Storage temperature range.....– 55 to 150 °C

Input/output voltage.....-0.5 to min (Vcc+0.5,4.6) V

Power supply voltage.....-0.5V to 4.6 V

Power dissipation.....1.3 W

Data out current (short circuit).....50 mA

Note

Stresses above those listed under „Absolute Maximum Ratings“ may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1)
Input low voltage	V_{IL}	– 0.3	0.8	V	1)
Output high voltage (LVTTL) Output „H“ level voltage (Iout = -2mA)	V_{OH}	2.4	–	V	
Output low voltage (LVTTL) Output „L“level voltage (Iout = +2mA)	V_{OL}	–	0.4	V	
Output high voltage (LVCMOS) Output „H“ level voltage (Iout = -100uA)	V_{OH}	Vcc-0.2	-	V	
Ouput low voltage (LVCMOS) Output „L“ level voltage (Iout = +100uA)	V_{OL}	-	0.2	V	
Input leakage current,any input (0 V < Vin < Vcc , all other pins = 0 V	$I_{I(L)}$	– 2	2	µA	
Output leakage current (DO is disabled, 0 V < Vout < Vcc)	$I_{O(L)}$	– 2	2	µA	

DC-Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	refresh version			Unit	Note
		2k	4k	8k		
Operating Current	I_{CC1}					
-40 ns version		250	155	110	mA	2) 3) 4)
-50 ns version		210	130	90	mA	
-60 ns version		170	105	75	mA	
($\overline{RAS}$, $\overline{CAS}$, address cycling: tRC = tRC min.)						
Standby Current ($\overline{RAS}$=$\overline{CAS}$= Vih)	I_{CC2}	2	2	2	mA	–
$\overline{RAS}$ Only Refresh Current:	I_{CC3}					
- -40 ns version		250	155	110	mA	2) 4)
-50ns version		210	130	90	mA	
-60 ns version		170	105	75	mA	
(RAS cycling: CAS = VIH: tRC = tRC min.)						
Fast Page Mode Current:	I_{CC4}					
-40 ns version		70	70	70	mA	2) 3) 4)
-50 ns version		60	60	60	mA	
-60 ns version		50	50	50	mA	
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: tPC=tPC min.)						
Standby Current ($\overline{RAS}$=$\overline{CAS}$= Vcc-0.2V)	I_{CC5}	900	900	900	µA	–
Standby Current (L-Version) ($\overline{RAS}$=$\overline{CAS}$= Vcc-0.2V)	I_{CC5}	200	200	200	µA	–
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}					
-40 ns version		250	155	155	mA	2) 4)
-50 ns version		210	130	130	mA	
-60 ns version		170	105	105	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling: tRC = tRC min.)						
Self Refresh Current (L-version only)	I_{CC7}	400	400	400	µA	
(CBR cycle with tRAS>TRASSmin, $\overline{CAS}$ held low, $\overline{WE}$ = Vcc-0.2V, Address and Din=Vcc-0.2V or 0.2V)						

AC Characteristics (note: 6,7,8) AC64-2F

T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3V

Parameter	Symbol	-40		-50		-60		Unit	Note
		min.	max.	min.	max.	min.	max.		
Common Parameters									
Random read or write cycle time	t_{RC}	75	–	90	–	110	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	40	100k	50	100k	60	100k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	100k	13	100k	15	100k	ns	
$\overline{RAS}$ precharge time	t_{RP}	25	–	30	–	40	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	5	–	7	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	5	–	7	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	30	17	37	20	45	ns	
$\overline{RAS}$ to column address delay	t_{RAD}	10	20	12	25	15	30	ns	
$\overline{RAS}$ hold time	t_{RSH}	10	–	13	–	15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	–	50	–	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
Transition time (rise and fall)	t_T	1	30	1	30	1	30	ns	7
Refresh period for 8k-refresh	t_{REF}	–	128	–	128	–	128	ms	
Refresh period for 4k-refresh	t_{REF}	–	64	–	64	–	64	ms	
Refresh period for 2k-refresh	t_{REF}	–	32	–	32	–	64	ms	
Refresh period for L-versions	t_{REF}	–	256	–	256	–	256	ms	
Read Cycle									
Access time from $\overline{RAS}$	t_{RAC}	–	40	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	10	–	13	–	15	ns	8, 9
Access time from column address	t_{AA}	–	20	–	25	–	30	ns	8, 10
$\overline{OE}$ access time	t_{OEA}	–	10	–	13	–	15	ns	8
Column address to $\overline{RAS}$ lead time	t_{RAL}	20	–	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	11

AC Characteristics *(cont'd)*(note: 6,7,8) AC64-2F

T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3V

Parameter	Symbol	-40		-50		-60		Unit	Note
		min.	max.	min.	max.	min.	max.		
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	–	10	–	13	–	15	ns	12
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	–	10	–	13	–	15	ns	12
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	t_{CDD}	10	–	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	10	–	13	–	15	–	ns	14
Write Cycle									
Write command hold time	t_{WCH}	5	–	7	–	10	–	ns	
Write command pulse width	t_{WP}	5	–	7	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	–	13	–	15	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	–	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	0	–	ns	16
Data hold time	t_{DH}	5	–	7	–	10	–	ns	16
$\overline{CAS}$ delay time from Din	t_{DZC}	0	–	0	–	0	–	ns	13
Read-Modify-Write Cycle									
Read-write cycle time	t_{RWC}	105	–	126	–	150	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	55	–	68	–	80	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	25	–	31	–	35	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	35	–	43	–	50	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	5	–	7	–	10	–	ns	
Fast Page Mode Cycle									
Fast page mode cycle time	t_{PC}	30	–	35	–	40	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	25	–	30	–	35	ns	8
$\overline{RAS}$ pulse width	t_{RAS}	40	200k	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHPC}	25	–	30	–	35	–	ns	

AC Characteristics *(cont'd)*(note: 6,7,8) AC64-2F

T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3V

Parameter	Symbol	-40		-50		-60		Unit	Note
		min.	max.	min.	max.	min.	max.		
Fast Page Mode Read-Modify-Write Cycle									
Fast page mode read-write cycle time	t_{PRWC}	60	–	71	–	80	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	40	–	48	–	55	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle									
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	5	–	5	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	5	–	5	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	5	–	5	–	10	–	ns	
Self Refresh Cycle (L-version only)									
$\overline{RAS}$ pulse width	t_{RASS}	100k	–	100k	–	100k	–	ns	17
$\overline{RAS}$ precharge time	t_{RPS}	75	–	90	–	110	–	ns	17
$\overline{CAS}$ hold time	t_{CHS}	-50	–	-50	–	-50	–	ns	17

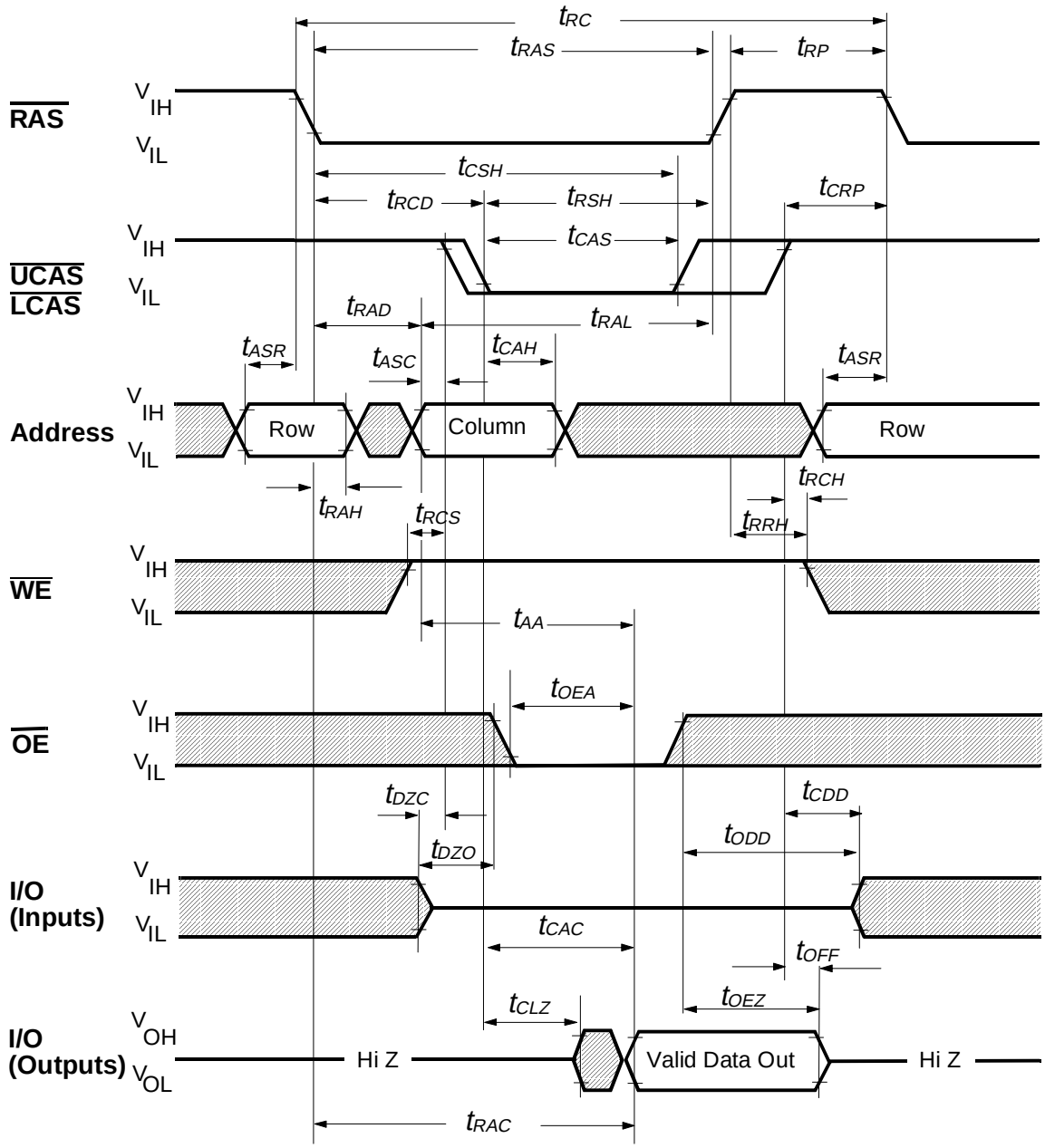
Capacitance

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

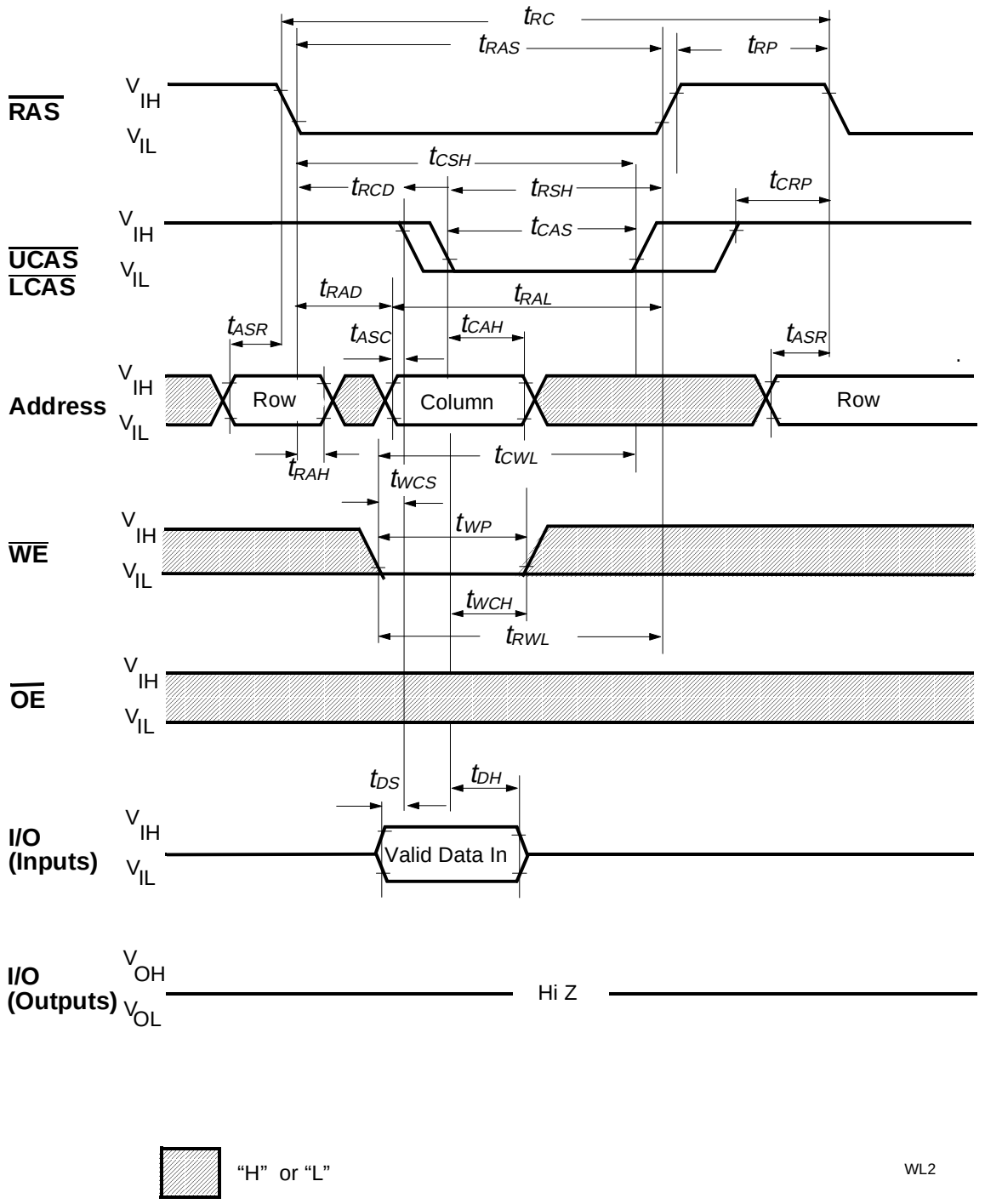
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,A12)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O8)	C_{IO}	–	7	pF

Notes:

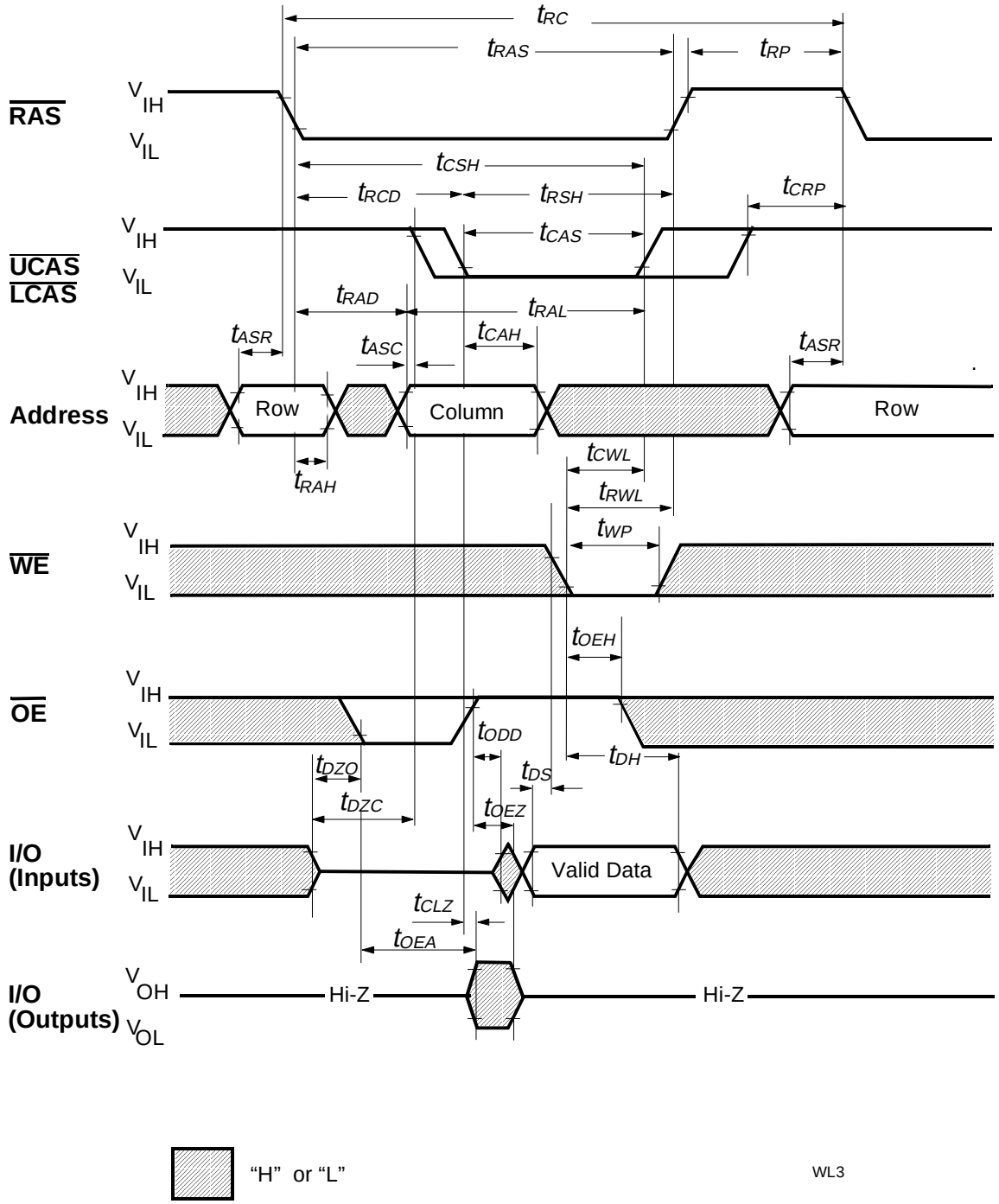
1) All voltages are referenced to VSS.
   Vih may overshoot to Vcc + 2.0 V for pulse widths of < 4ns with 3.3V. Vil may undershoot to -2.0V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
2) ICC1, ICC3, ICC4 and ICC6 and ICC7 depend on cycle rate.
3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
4) Address can be changed once or less while $\overline{RAS}$ = Vil.In the case of ICC4 it can be changed once or less during a fast page mode cycle (tpc).
5) An initial pause of 100 µs is required after power-up followed by 8 $\overline{RAS}$-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6) AC measurements assume tT = 5 ns.
7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.
8) Measured with the specified current load and 100 pF at Voh = 2.0 V and Vol = 0.8 V.
9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
11) Either tRCH or tRRH must be satisfied for a read cycle.
12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
13) Either tDZC or tDZO must be satisfied.
14) Either tCDD or tODD must be satisfied.
15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if tRWD > tRWD (min.), tCWD > tCWD (min.), tAWD > tAWD (min.) and tCPWD > tCPWD (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
16) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
   If row addresses are being refresh in an evenly distributed manner over the refresh iterval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.
   If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
UCAS
LCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row
Column
Row
tRCH
tRAH
tRCS
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O
(Inputs)
tCAC
tOFF
tOEZ
tCLZ
I/O
(Outputs)
VOH
VOL
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"
WL1

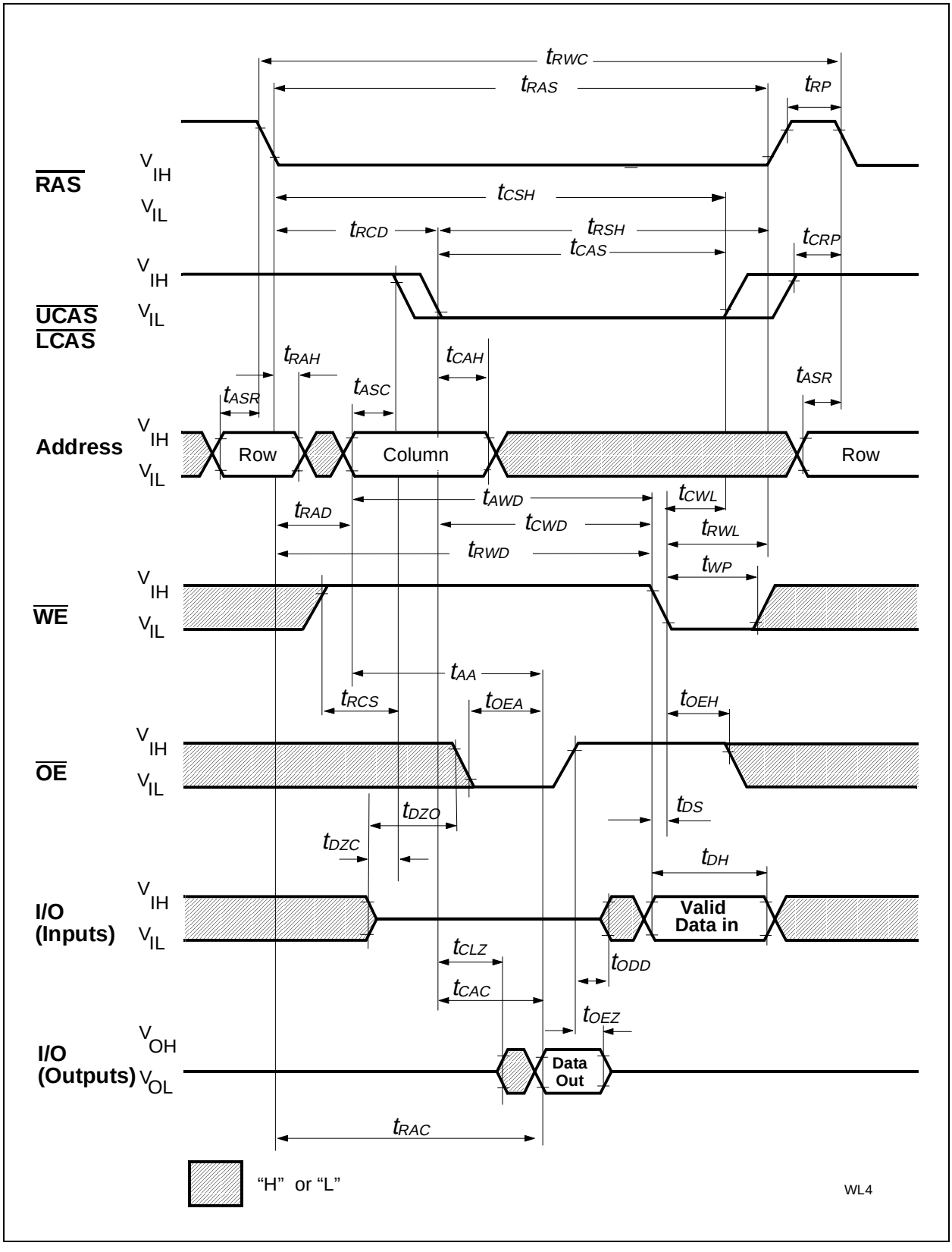
Read Cycle



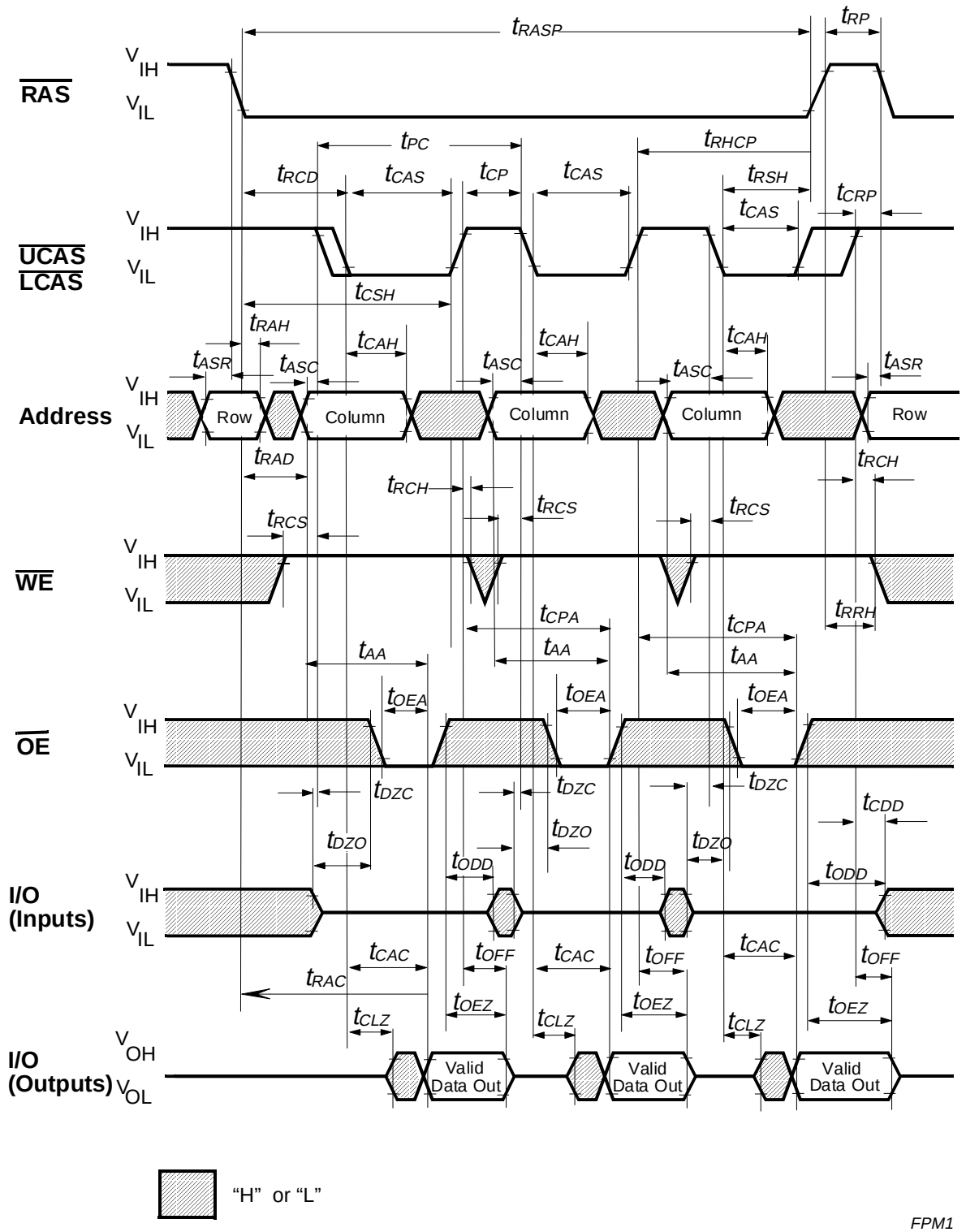
Write Cycle (Early Write)



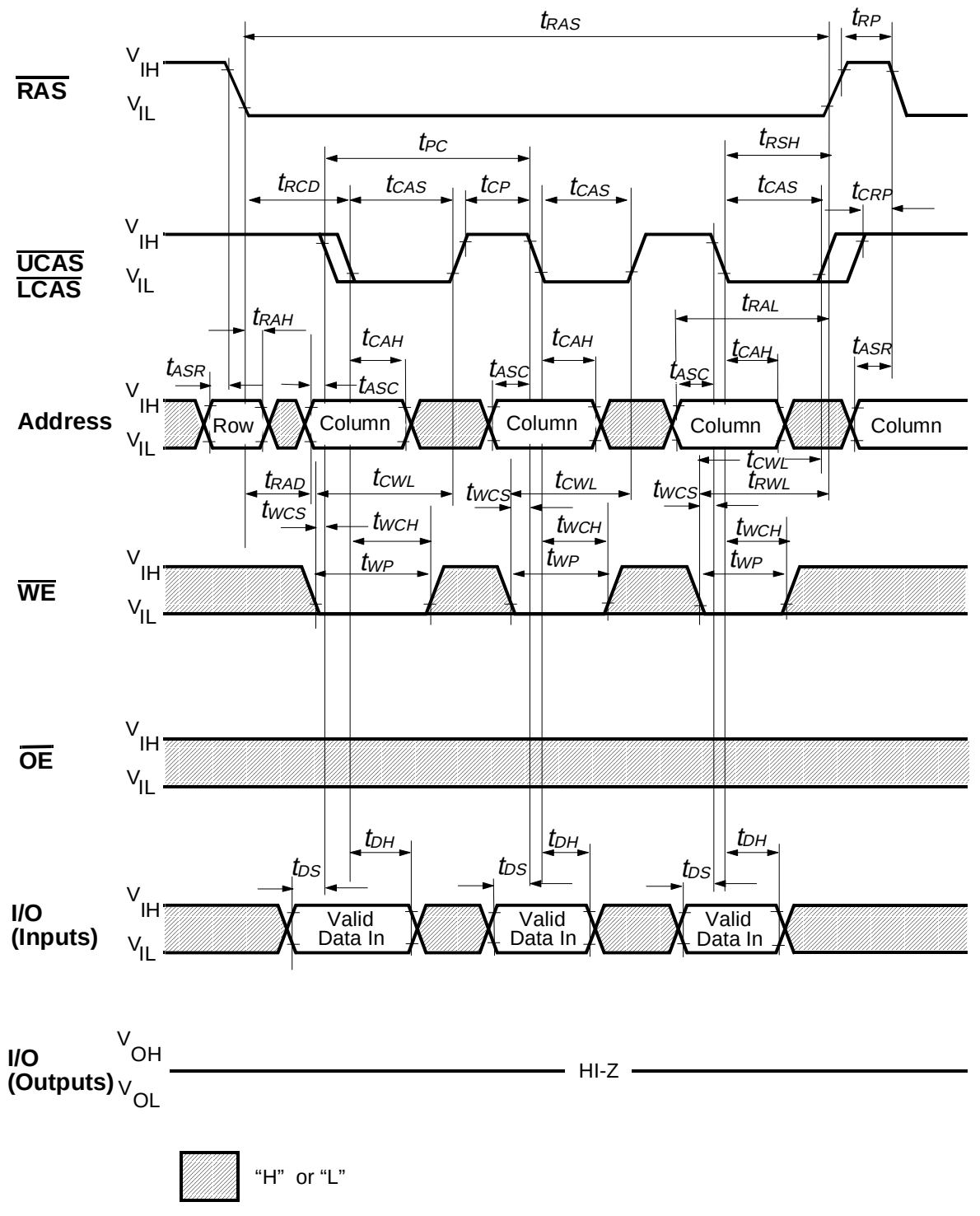
Write Cycle ($\overline{OE}$ Controlled Write)



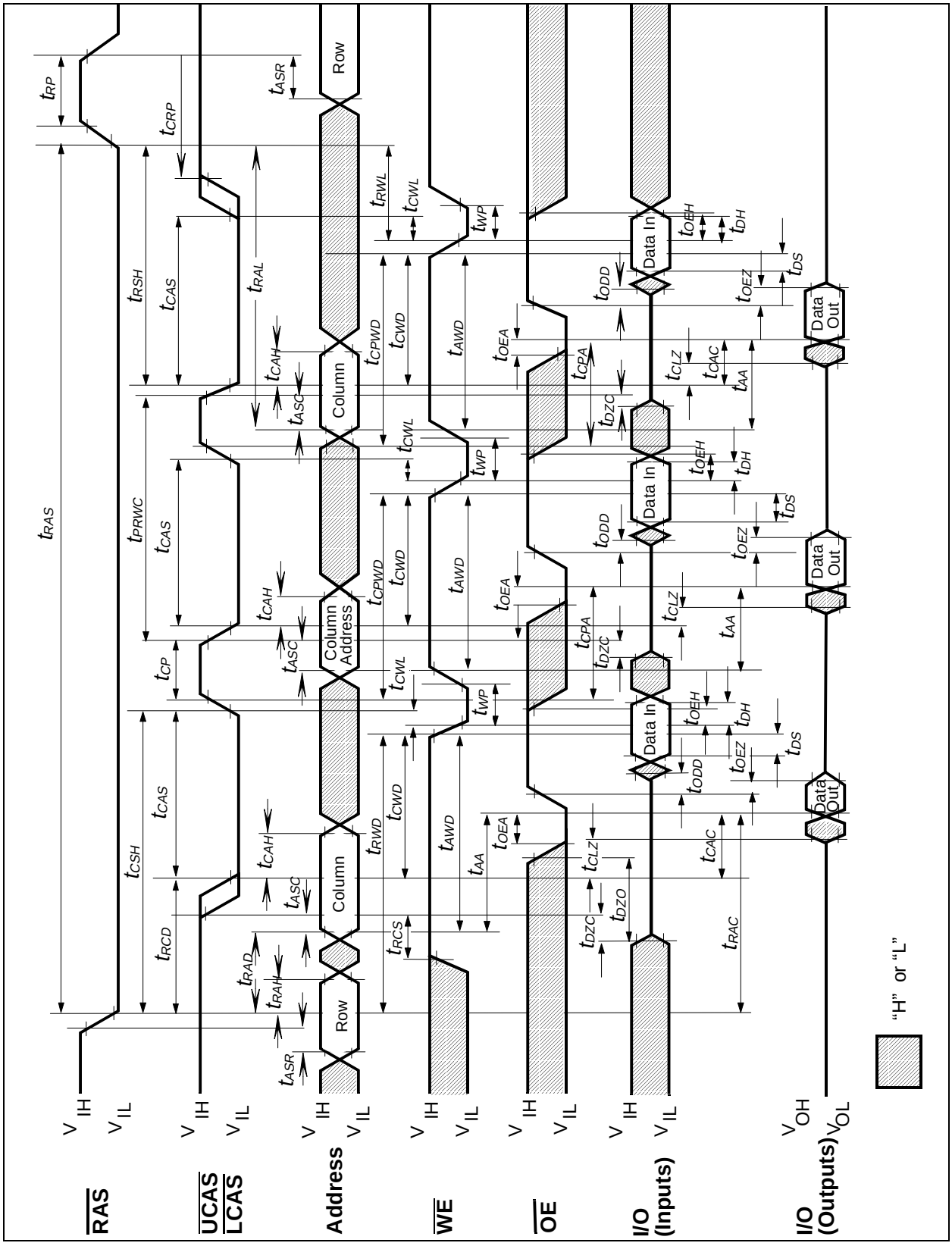
Read-Write (Read-Modify-Write) Cycle



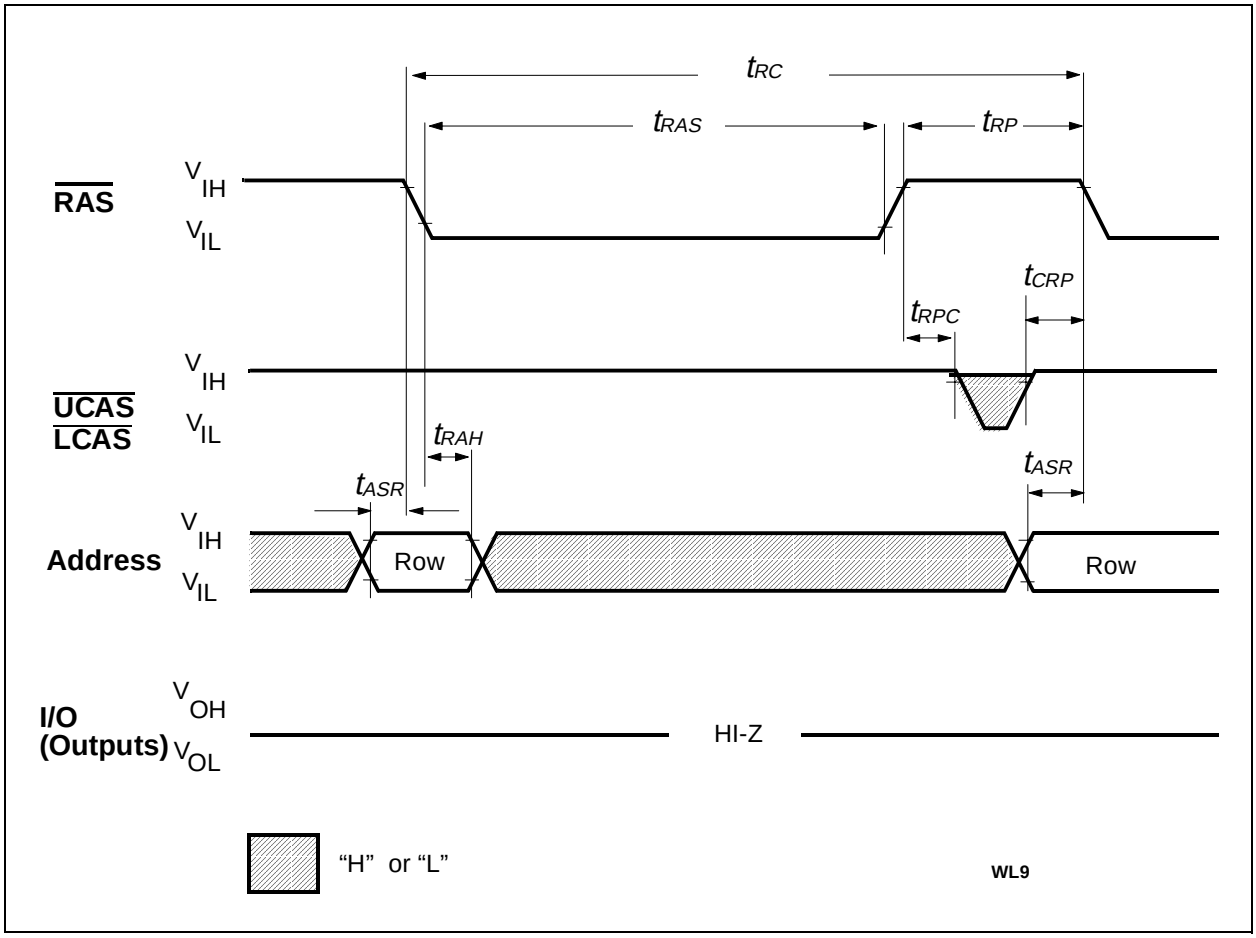
Fast Page Mode Read Cycle



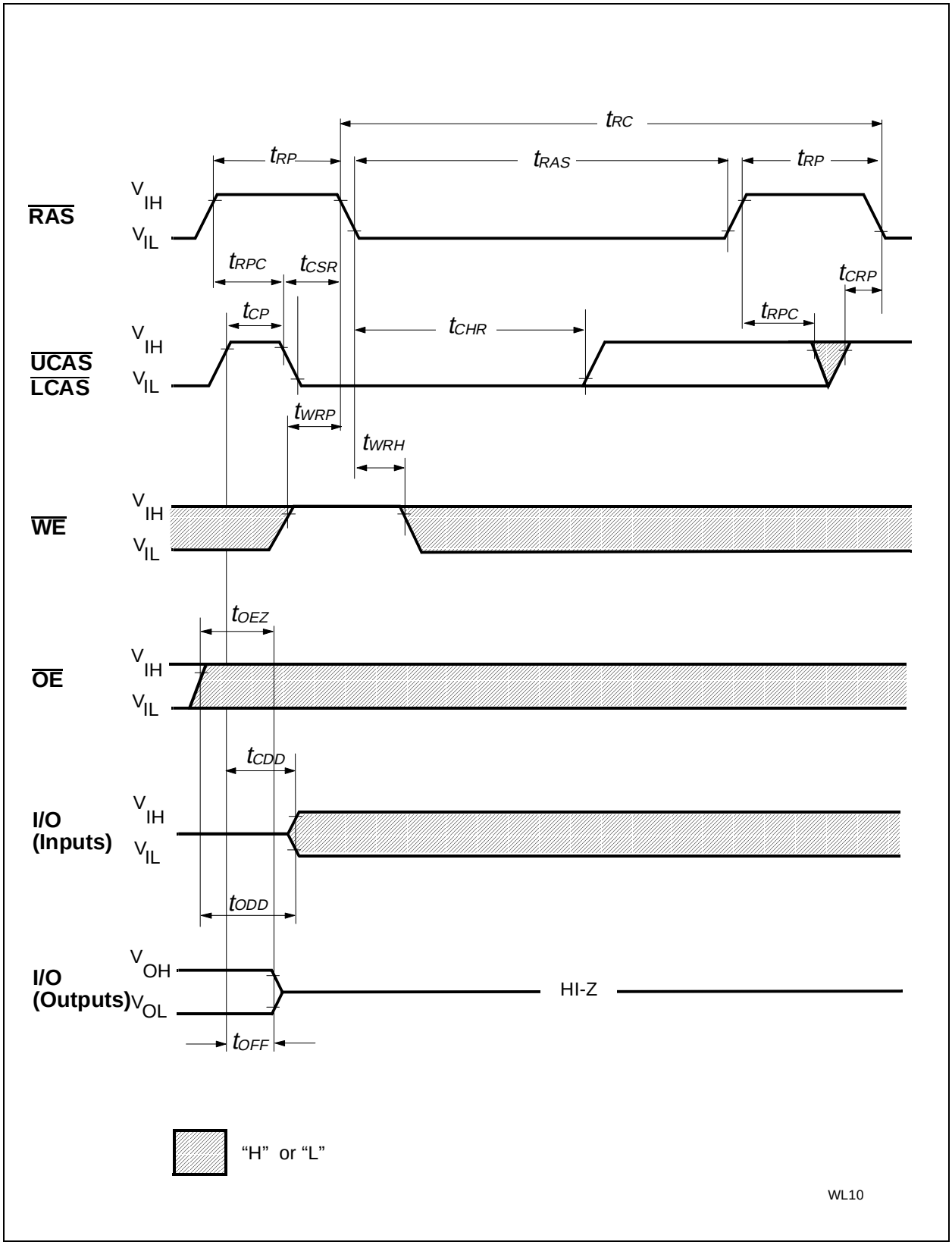
Fast Page Mode Early Write Cycle



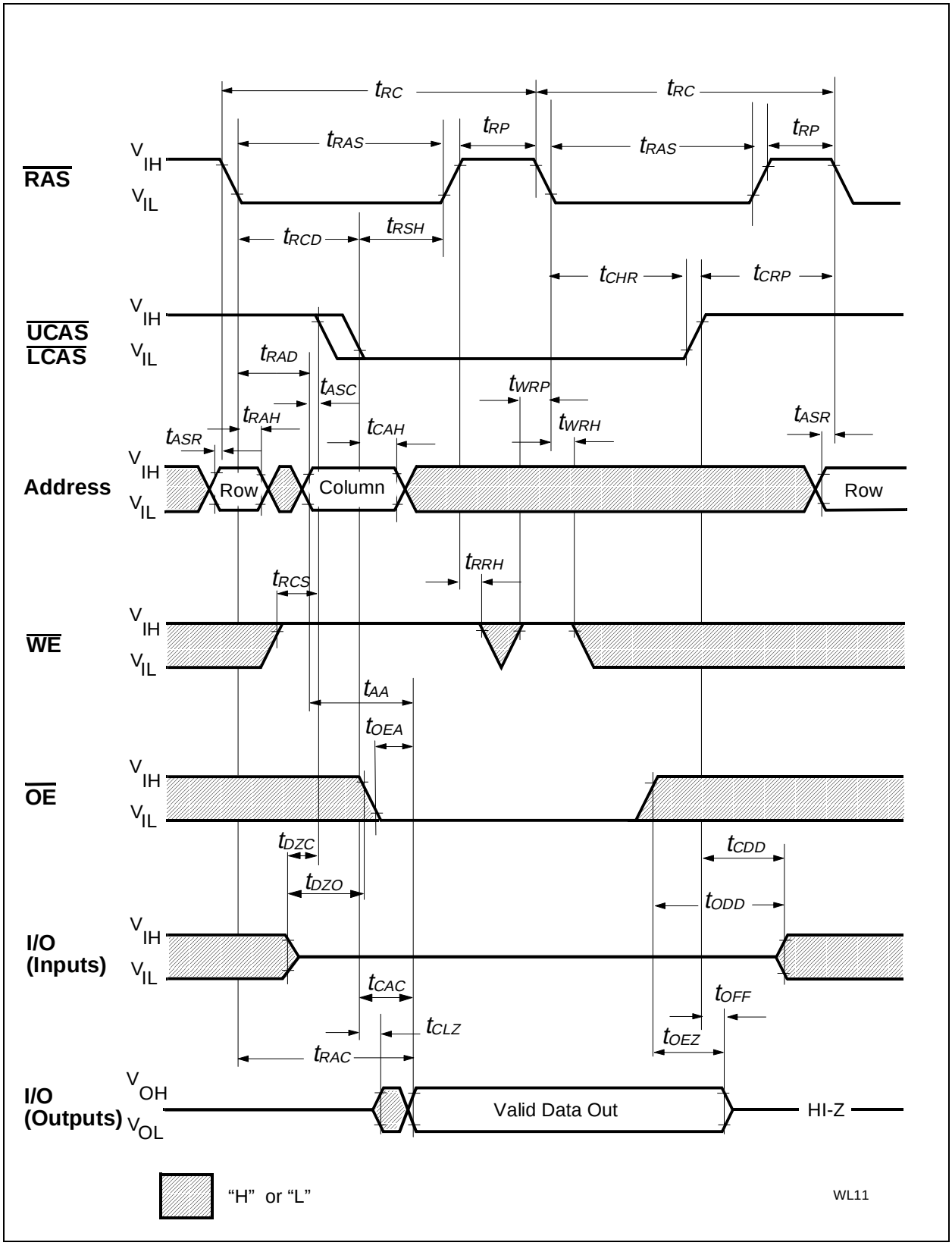
Fast Page Mode Read-Modify-Write Cycle



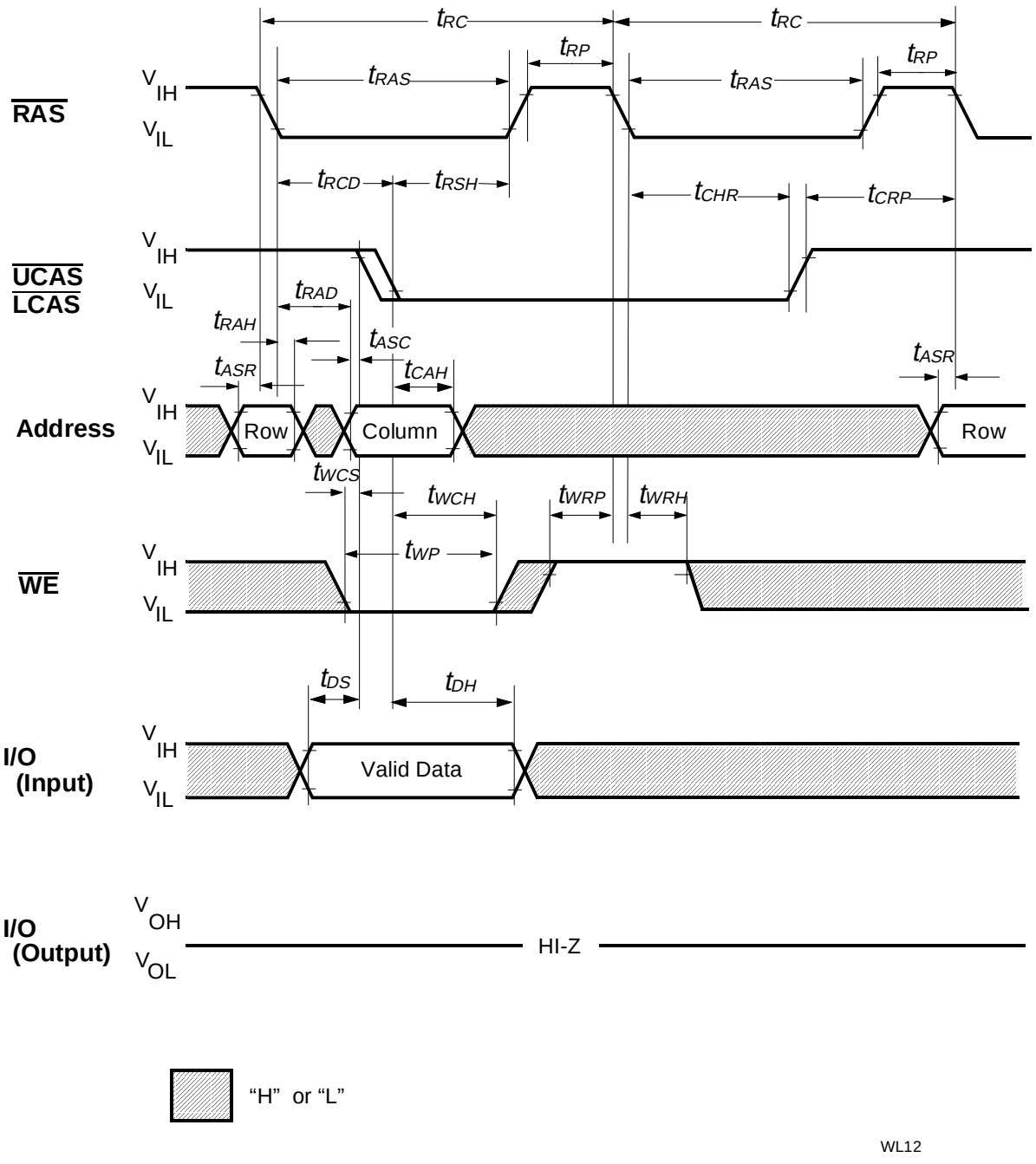
$\overline{\text{RAS}}$-Only Refresh Cycle



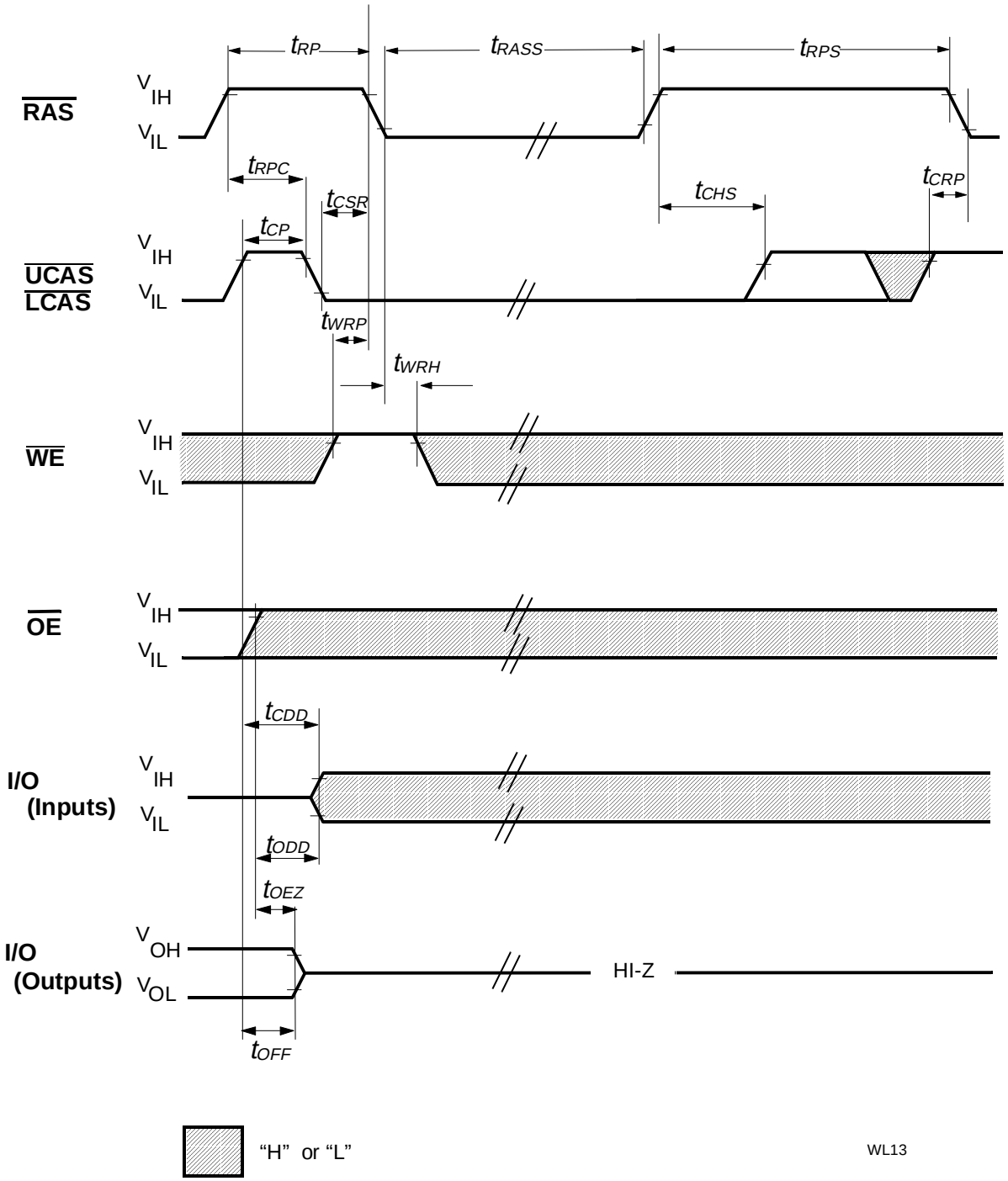
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



Hidden Refresh Cycle (Read)



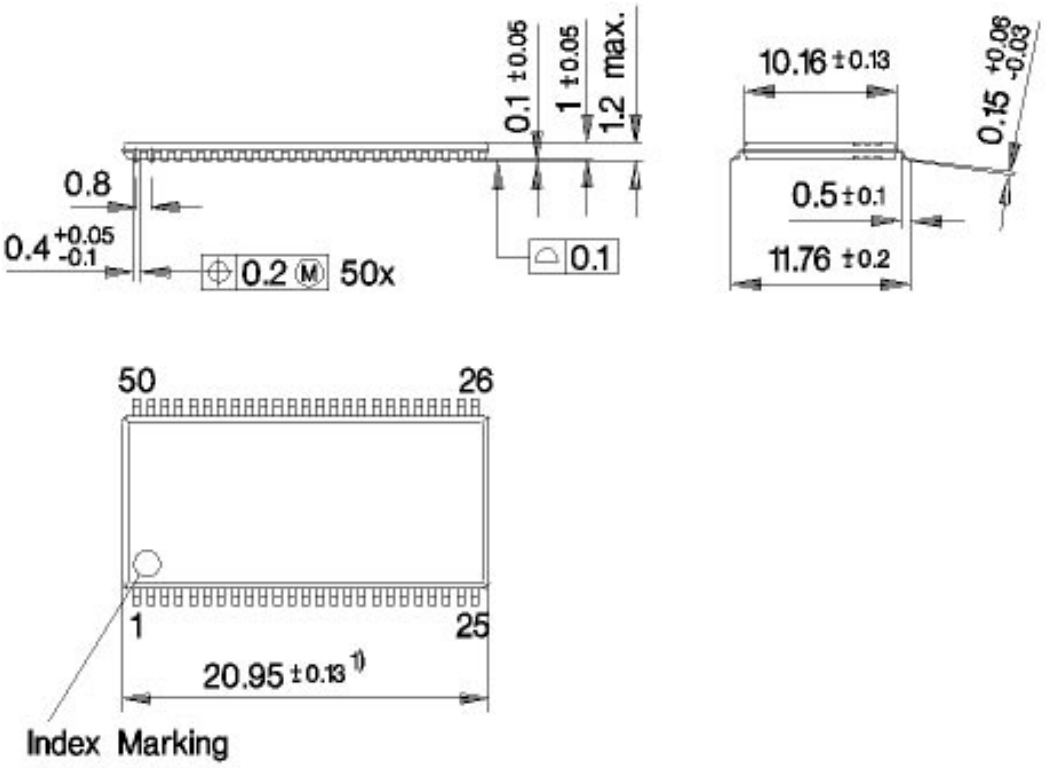
Hidden Refresh Write Cycle



CAS-before-RAS Self Refresh („Sleep Mode“)

Package Outlines

Plastic Package P-TSOPII-50
(400 mil width, 0.8 mm lead pitch, thin small outline, SMD)



1) Does not include plastic or metal protrusion of 0.25 max. per side