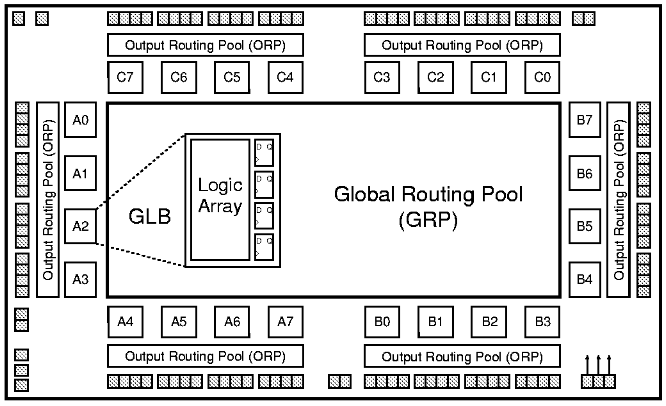
ispLSI® and pLSI® 2096

High Density Programmable Logic

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **4000 PLD Gates**
  - **96 I/O Pins, Six Dedicated Inputs**
  - **96 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E^2CMOS® TECHNOLOGY**
  - **f_{max} = 125 MHz Maximum Operating Frequency**
  - **t_{pd} = 7.5 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **In-System Programmable (ISP™) 5-Volt Only**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Enhanced Pin Locking Capability**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **Superior Quality of Results**
  - **Tightly Integrated with Leading CAE Vendor Tools**
  - **Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI and pLSI 2096 are High Density Programmable Logic Devices. The devices contain 96 Registers, 96 Universal I/O pins, six Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2096 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 2096 offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2096 device, but multiplexes three input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 2096 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…C7 (see figure 1). There are a total of 24 GLBs in the ispLSI and pLSI 2096 devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

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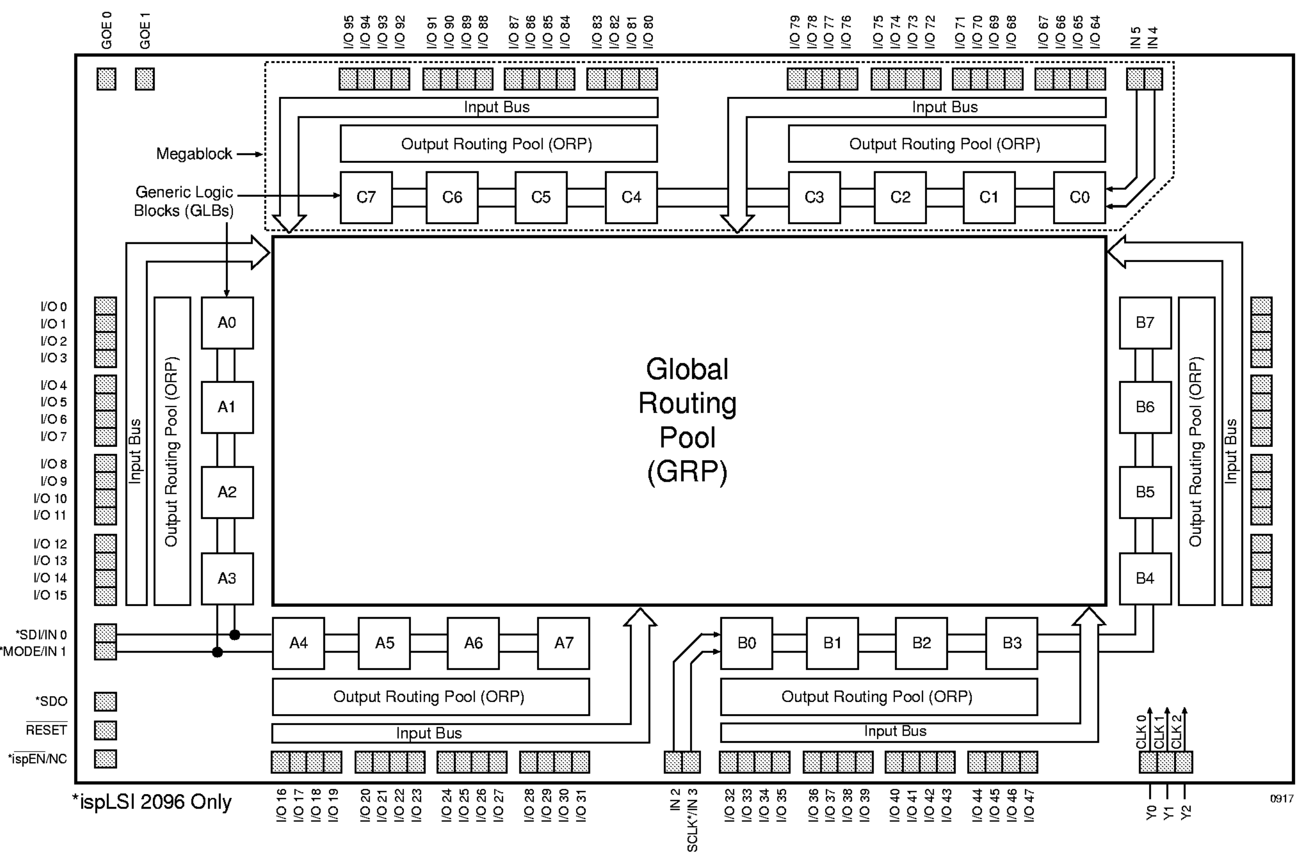
Functional Block Diagram

Figure 1. ispLSI and pLSI 2096 Functional Block Diagram



The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the two ORPs. Each ispLSI and pLSI 2096 device contains three Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 2096 devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} .... -0.5 to +7.0V

Input Voltage Applied........................ -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature .... -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (TJ) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{cc}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{cc}+1	V

Table 2 - 0005/2096

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O and Dedicated Input Capacitance	8	pf	V_{CC} = 5.0V, $V_{I/O,\ IN}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006a

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

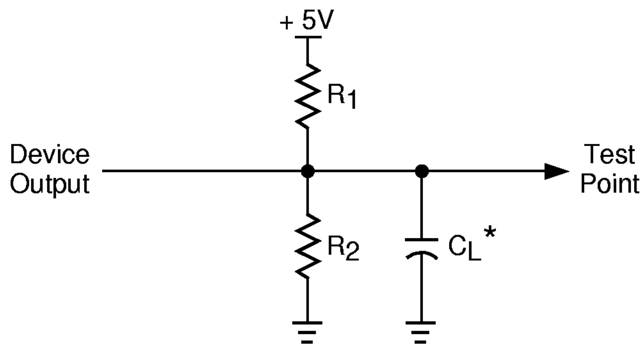
Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Output Timing Reference Levels	1.5V	
Output Load	See Figure 2	

Table 2-0003/2096

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*CL includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2-0004/2096

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{\text{ispEN}}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V	Commercial	–	150	295	mA
		f_{CLOCK} = 1 MHz	Industrial	–	150	–	mA

Table 2-0007/2096

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-125		-100		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	10.0	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	125	–	100	–	81.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	100	–	77.0	–	57.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	125	–	100	–	83.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.0	–	6.5	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.0	–	5.0	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	6.0	–	8.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	4.5	–	6.0	–	8.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	–	17.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Product Term OE, Enable	–	12.0	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Product Term OE, Disable	–	12.0	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE, Enable	–	7.0	–	9.0	–	12.0	ns
t_{goedis}	C	17	Global OE, Disable	–	7.0	–	9.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	5.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	5.0	–	6.0	–	ns

Table 2-0030/2096

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

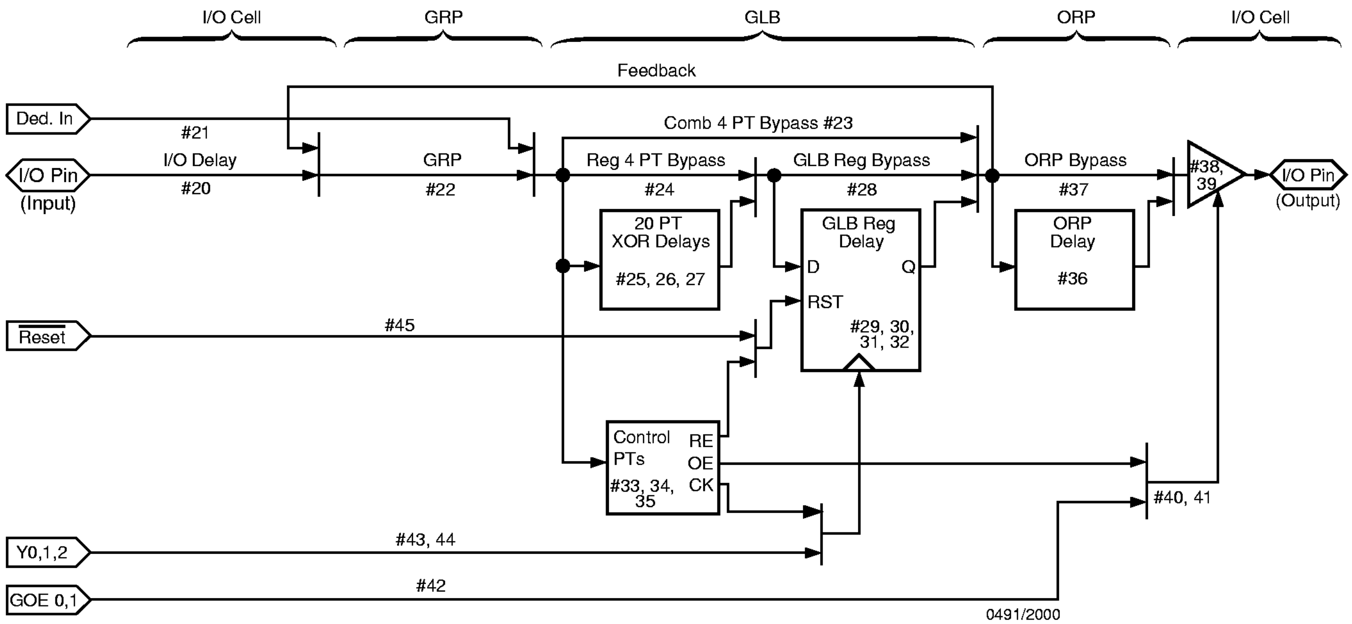
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-125		-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{io}	20	Input Buffer Delay	–	0.2	–	0.5	–	1.8	ns
t_{din}	21	Dedicated Input Delay	–	1.5	–	2.2	–	4.4	ns
GRP									
t_{grp}	22	GRP Delay	–	1.3	–	1.7	–	2.6	ns
GLB									
t_{4ptbpc}	23	4 Product Term Bypass Comb. Path Delay	–	4.5	–	5.8	–	8.1	ns
t_{4ptbpr}	24	4 Product Term Bypass Reg. Path Delay	–	5.0	–	5.8	–	6.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	5.7	–	6.8	–	8.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	6.0	–	7.3	–	8.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	6.5	–	8.0	–	9.8	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.5	–	0.5	–	1.3	ns
t_{gsu}	29	GLB Register Setup Time before Clock	0.8	–	1.2	–	1.4	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	3.0	–	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.2	–	0.3	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.1	–	1.3	–	1.6	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	4.8	–	6.1	–	8.6	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	7.3	–	8.6	–	9.0	ns
t_{ptck}	35	GLB Product Term Clock Delay	3.3	5.6	4.1	7.1	5.6	10.2	ns
ORP									
t_{orp}	36	ORP Delay	–	0.8	–	1.4	–	2.0	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.3	–	0.4	–	0.5	ns
Outputs									
t_{ob}	38	Output Buffer Delay	–	1.2	–	1.6	–	2.0	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	3.2	–	4.2	–	4.6	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	3.2	–	4.2	–	4.6	ns
t_{goe}	42	Global Output Enable	–	3.8	–	4.8	–	7.4	ns
Clocks									
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. Clock)	2.3	2.3	2.7	2.7	3.6	3.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.3	2.3	2.7	2.7	3.6	3.6	ns
Global Reset									
t_{gr}	45	Global Reset to GLB	–	6.9	–	9.2	–	11.4	ns

Table 2-0036/2096

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI and pLSI 2096 Timing Model



Derivations of tsu, th and tco from the Product Term Clock

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
	=	(#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
3.5 ns	=	(0.2 + 1.3 + 6.0) + (0.8) - (0.2 + 1.3 + 3.3)
th	=	Clock (max) + Reg h - Logic
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
	=	(#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
2.6 ns	=	(0.2 + 1.3 + 5.6) + (3.0) - (0.2 + 1.3 + 6.0)
tco	=	Clock (max) + Reg co + Output
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#20+ #22+ #35) + (#31) + (#36 + #38)
9.3 ns	=	(0.2 + 1.3 + 5.6) + (0.2) + (0.8 + 1.2)

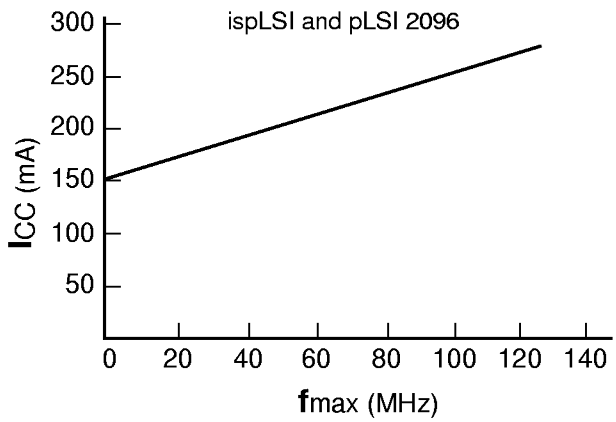
Note: Calculations are based upon timing specifications for the ispLSI and pLSI 2096-125L.

Table 2-0042/2096

Power Consumption

Power Consumption in the ispLSI and pLSI 2096 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of six 16-bit counters
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 2096 using the following equation:

I_{CC}(mA) = 20 + (# of PTs * 0.67) + (# of nets * Max freq * 0.011)

Where:

- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/2096

Pin Description

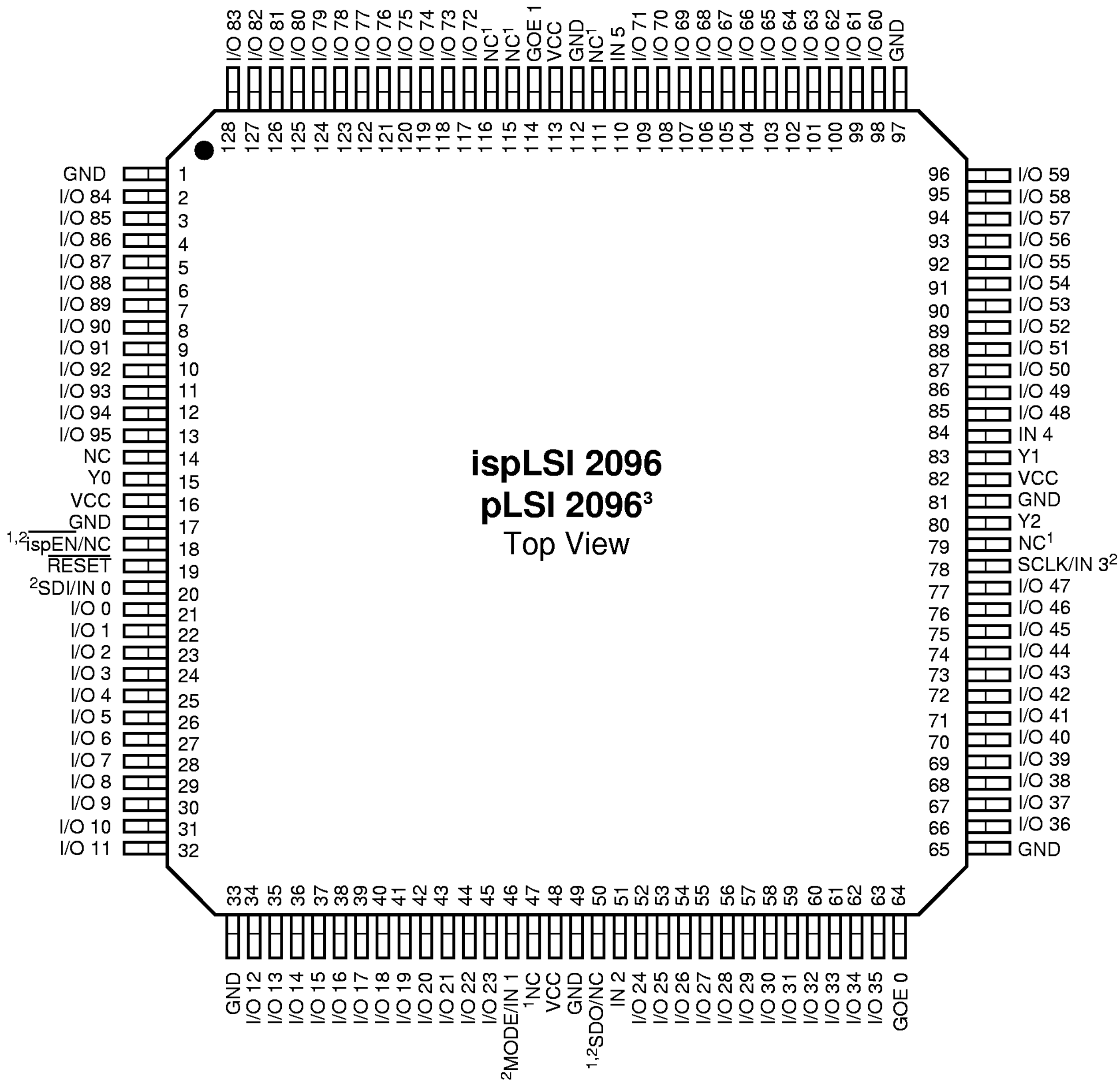
NAME	PQFP & TQFP* PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	21, 22, 23, 24, 25, 26 27, 28, 29, 30, 31, 32 34, 35, 36, 37, 38, 39 40, 41, 42, 43, 44, 45 52, 53, 54, 55, 56, 57 58, 59, 60, 61, 62, 63 66, 67, 68, 69, 70, 71 72, 73, 74, 75, 76, 77 85, 86, 87, 88, 89, 90 91, 92, 93, 94, 95, 96 98, 99, 100, 101, 102, 103 104, 105, 106, 107, 108, 109 117, 118, 119, 120, 121, 122 123, 124, 125, 126, 127, 128 2, 3, 4, 5, 6, 7 8, 9, 10, 11, 12, 13	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0, GOE 1	64, 114	Global Output Enables input pins.
IN 2, IN 4, IN 5	51, 84, 110	Dedicated input pins to the device.
$\overline{\text{ispEN}}$/NC[1,2]	18	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0[2]	20	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN0 also is used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE/IN 1[2]	46	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO/NC[1,2]	50	Output - When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 3[2]	78	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
$\overline{\text{RESET}}$	19	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1, Y2	15 83, 80	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
GND	1, 17, 33, 49, 65, 81, 97, 112	Ground (GND)
VCC	16, 48, 82, 113	V_{CC}
NC[1]	14, 47, 79, 111, 115, 116	No Connect.

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability for ispLSI 2096 only.

Table 2-0002-2096

Pin Configuration

ispLSI and pLSI 2096 128-pin PQFP and TQFP Pinout Diagram



1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability for ispLSI 2096 only (except pins 18 and 50, which are ispEN and SDO only, respectively).
3. pLSI 2096 available in 128-pin PQFP package only.

0124-2096

Part Number Description

(is)pLSI 2096 – XXX X X X

Device Family — (is)pLSI

Device Number — 2096

Speed
- 125 = 125 MHz **f**max
- 100 = 100 MHz **f**max
- 80 = 81 MHz **f**max

Grade
- Blank = Commercial
- I = Industrial

Package
- T = TQFP
- Q = PQFP

Power
- L = Low

212-80B isp/2096

ispLSI and pLSI 2096 Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 2096-125LQ	128-Pin PQFP
	125	7.5	ispLSI 2096-125LT	128-Pin TQFP
	100	10	ispLSI 2096-100LQ	128-Pin PQFP
	100	10	ispLSI 2096-100LT	128-Pin TQFP
	81	15	ispLSI 2096-80LQ	128-Pin PQFP
	81	15	ispLSI 2096-80LT	128-Pin TQFP
pLSI	125	7.5	pLSI 2096-125LQ	128-Pin PQFP
	100	10	pLSI 2096-100LQ	128-Pin PQFP
	81	15	pLSI 2096-80LQ	128-Pin PQFP

Table 2-0041A/2096

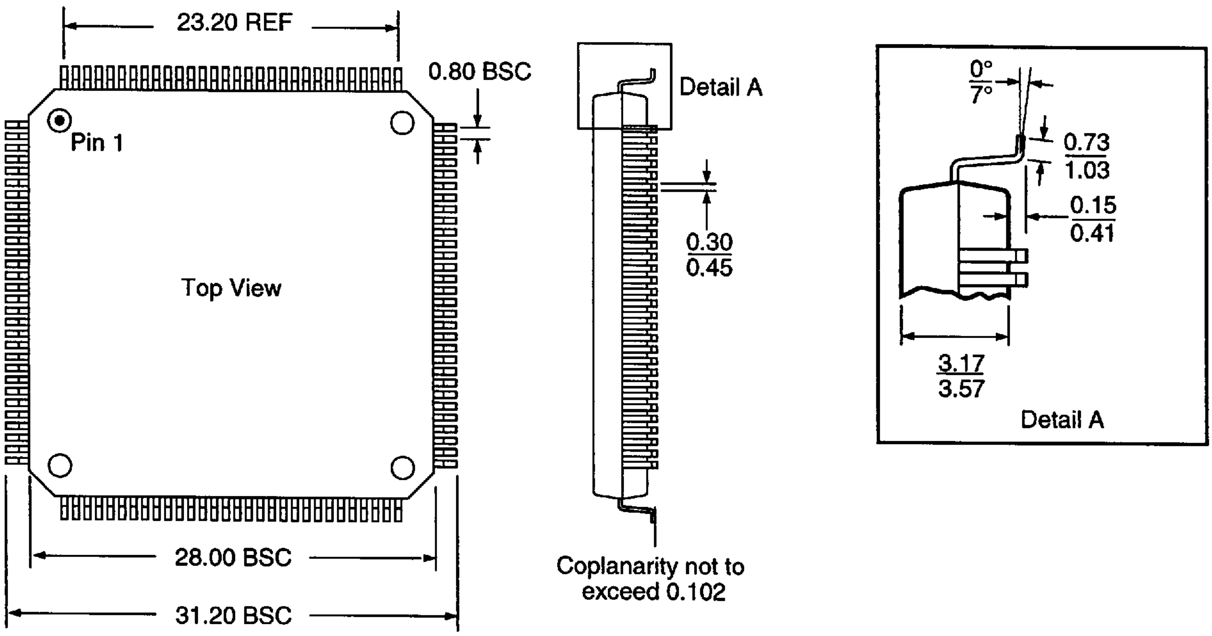
INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	81	15	ispLSI 2096-80LQI	128-Pin PQFP
	81	15	ispLSI 2096-80LTI	128-Pin TQFP

Table 2-0041B/2096

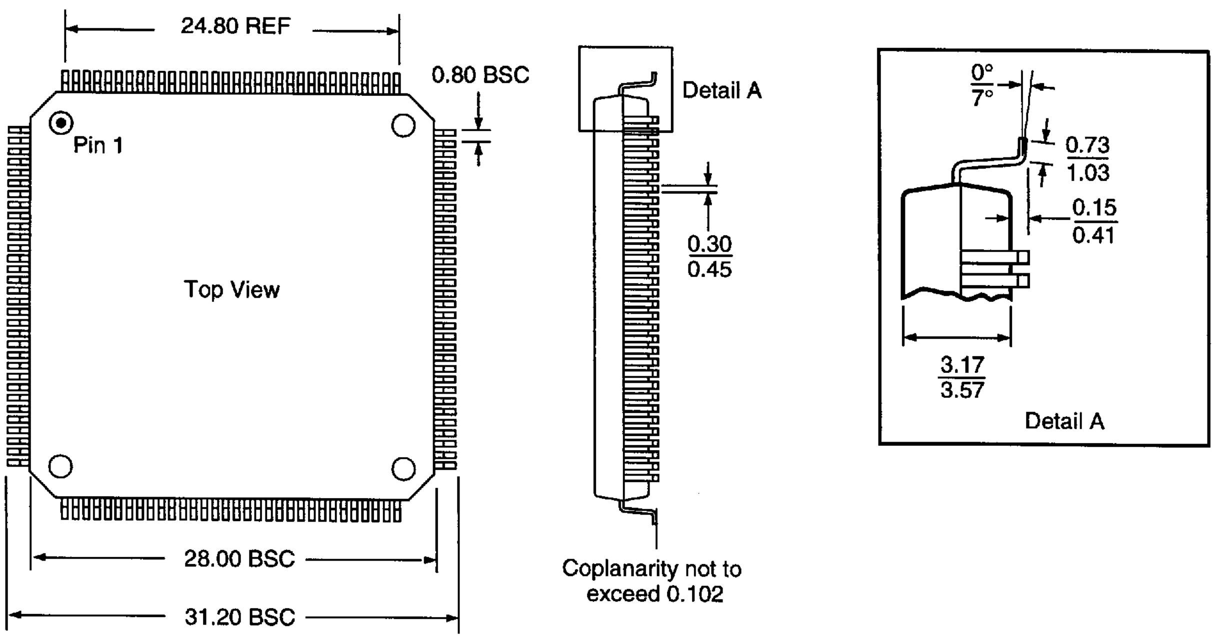
120-Pin PQFP Package

Dimensions in Millimeters MIN. / MAX.



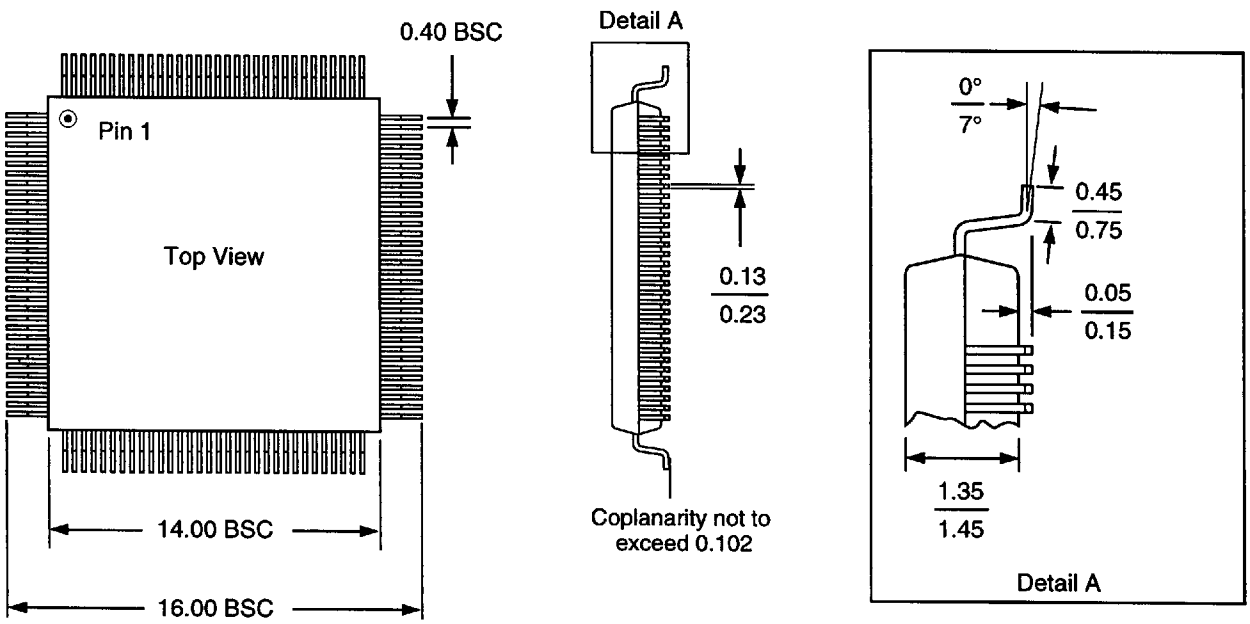
128-Pin PQFP Package

Dimensions in Millimeters MIN. / MAX.



128-Pin TQFP Package

Dimensions in Millimeters MIN. / MAX.



133-Pin CPGA Package

Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)