Description

The EG&G Reticon RF6651ANP-011 is a high performance, monolithic, switched-capacitor filter designed for testing telephone and telecommunication systems. The device contains three filters fabricated using double-poly CMOS technology, and is offered in a 24-pin, 600 mil package. Pinout configurations with a functional block diagram is shown in Figure 1, and a pin description is in Table 1.

This CMOS version of the RF5651A features lower noise, lower DC offset, lower clock feedthrough, reduced power consumption, and more precise control of clock-to-corner ratios. A temperature-tested version, RF6651ANP-012, is available; its temperature characteristics are given in Table 3 and shown in Figures 7 through 20. Another version with a relaxed notch specification, RF6651ANP-020, is also available.

Key Features

- Combination filter set
  - C-Message filter meeting Bell System specifications
  - 1010 Hz notch filter meeting IEEE specifications
  - Program Weighing filter meeting ANSI/IEEE Std 743-1984 specifications
- Three uncommitted op amps for user-designated functions
- Operates from a TV color burst crystal or from an external TTL/CMOS clock
- Low power, low noise CMOS switched-capacitor technology
- Latchup free

Typical Applications

- Typical tests this chip can implement are signal-to-noise ratios, harmonic distortion, and idle-channel noise. The low power and improved performance of this chip make it highly suitable for portable test equipment.
- Testing and measurement instrumentation for the US telephone system, both voice and data communication channels.
- Portable, low-power instrumentation.

Device Operation

This device operates at either ±5V (±10%) power supplies or a single +10V supply. It requires either an external TTL (or CMOS) 3.58 MHz clock or a 3.58 MHz TV color burst crystal (parallel resonance variety), as shown in Figure 2. A TTL input clock must be used only with symmetrical (split) ±5V supplies. A CMOS input clock can be used with either split supplies or a single +10V supply. Note that since switched-capacitor filters are clock-tunable, any variation in clock frequency or accuracy will alter the tuning of the filters.

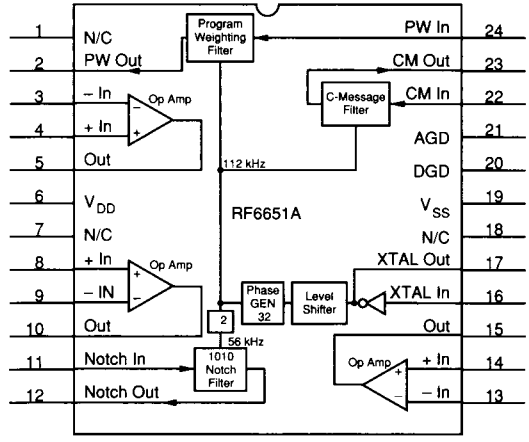

Figure 1. Pinout Configuration and Functional Block Diagram

There are three uncommitted op amps for user-defined functions such as gain adjustment, antialiasing, or smoothing filters. All op amps, including those at the output of each filter, are buffered and capable of driving a resistive load greater than 20KΩ and/or a capacitive load of up to 50 pF.

Filter characteristics are given in Table 2 and shown in Figures 3, 4, and 5. A basic application circuit is shown in Figure 6. If the on-chip op-amps are used for input antialiasing or output smoothing, the user must compensate for the phase characteristics of such filtering.

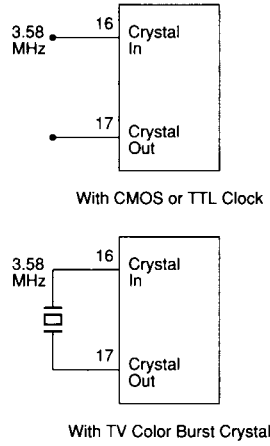

Figure 2. Clocking Circuits

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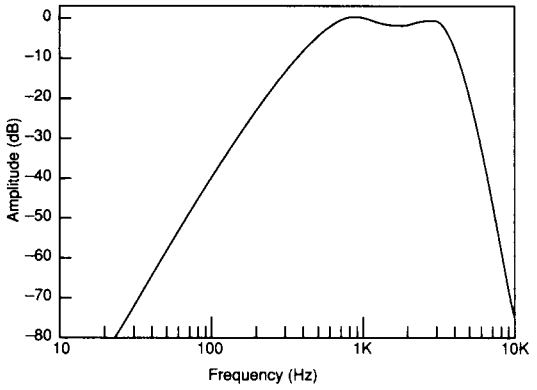

Figure 3. Typical C-Message Response

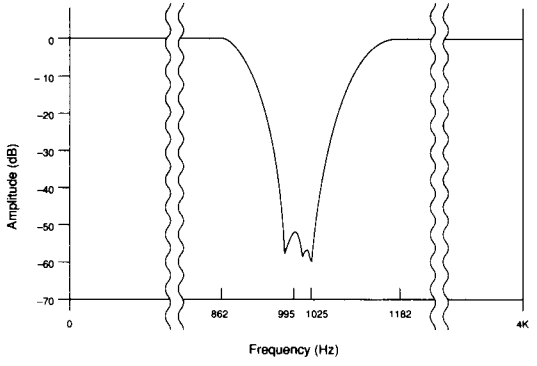

Figure 4. Typical 1010 Hz Notch Response

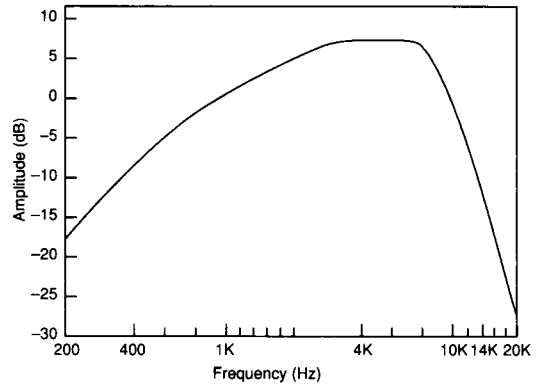

Figure 5. Typical Program Weighting Response

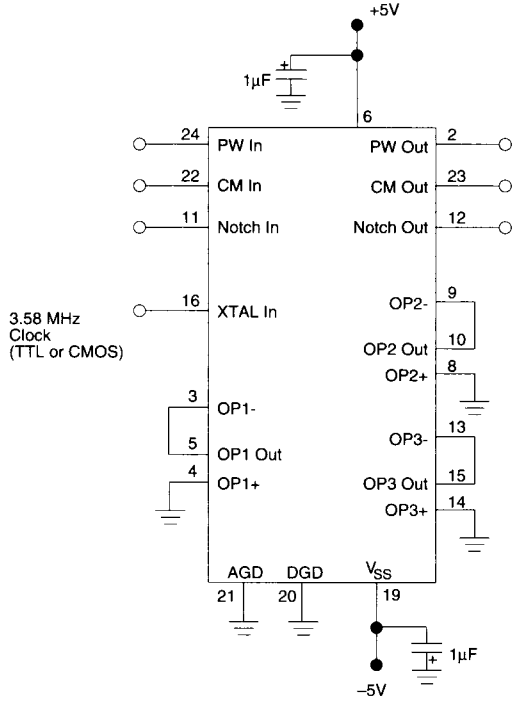

Figure 6. Basic Circuit

Typical Temperature Characteristics

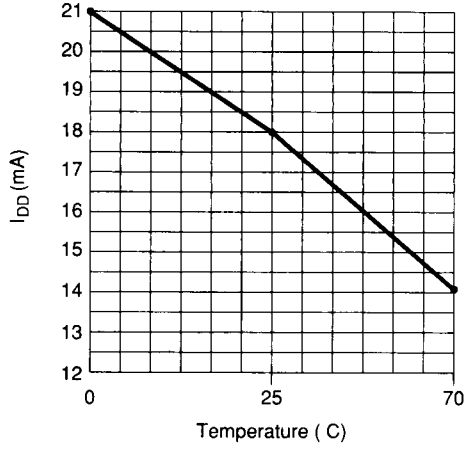

Figure 7. I_{DD} versus Temperature

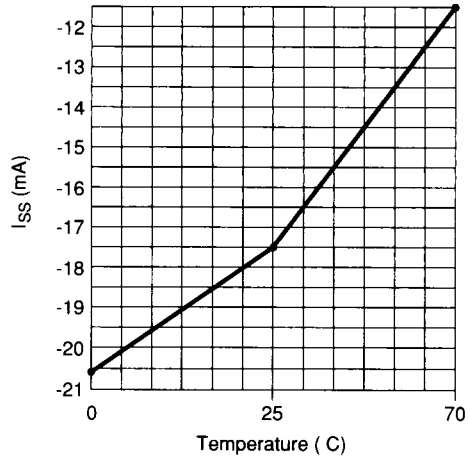

Figure 8. I_{SS} versus Temperature

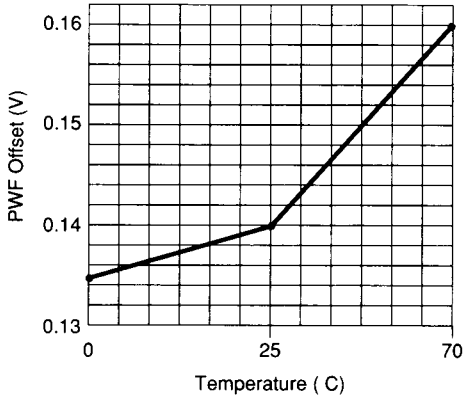

Figure 9. PWF Offset vesus Temperature

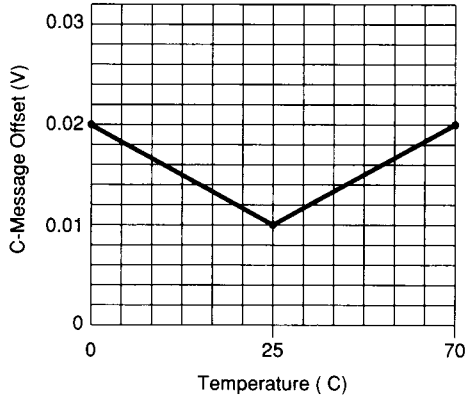

Figure 10. C-Message Filter Offset versus Temperature

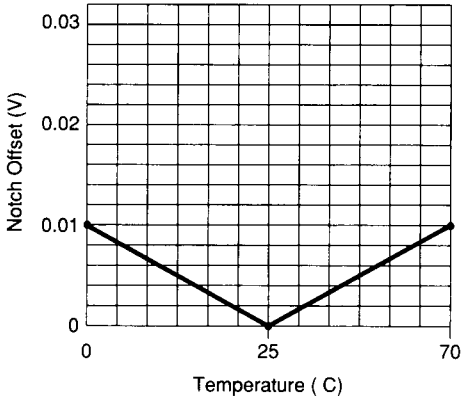

Figure 11. Notch Filter Offset versus Temperature

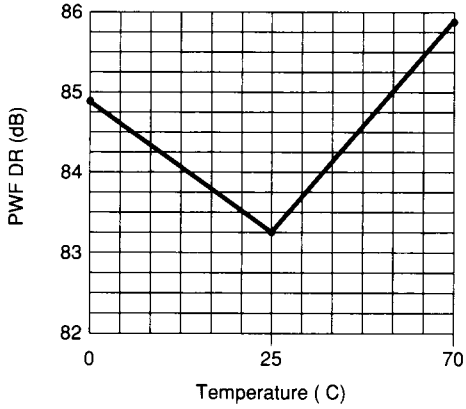

Figure 12. PWF Dynamic Range versus Temperature

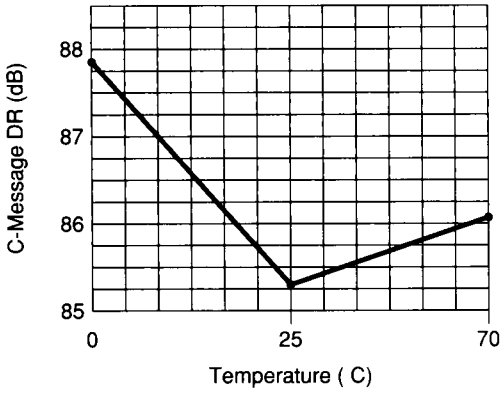

Figure 13. C-Message Filter Dynamic Range versus Temperature

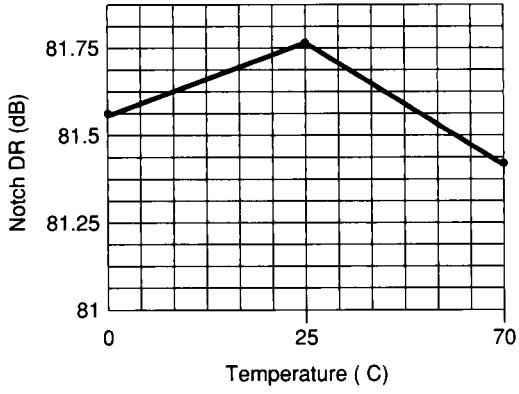

Figure 14. Notch Filter Dynamic Range versus Temperature

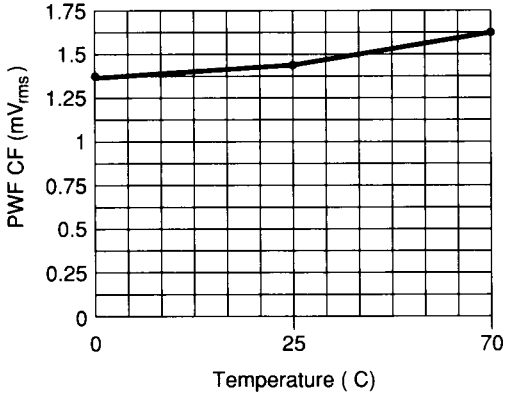

Figure 15. PWF Clock Feedthrough versus Temperature

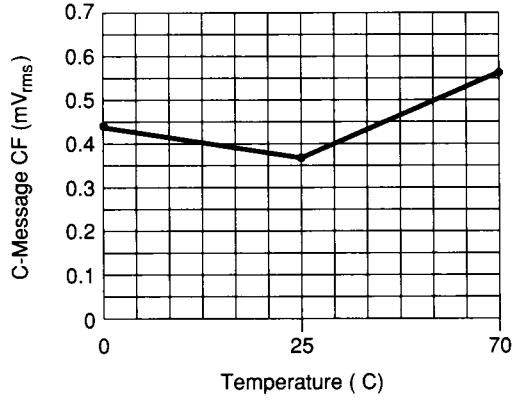

Figure 16. C-Message Filter Clock Feedthrough versus Temperature

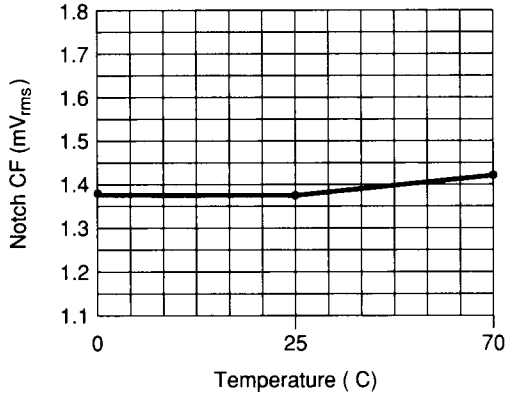

Figure 17. Notch Filter Clock Feedthrough versus Temperature

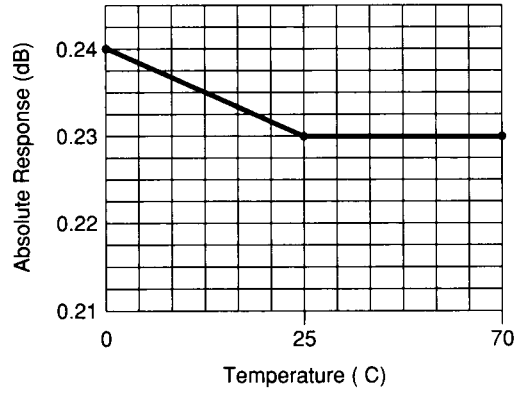

Figure 18. PWF 1 kHz Response versus Temperature

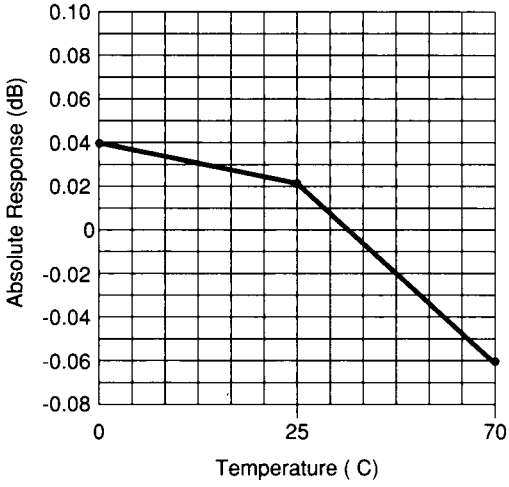

Figure 19. C-Message 1 kHz Response versus Temperature

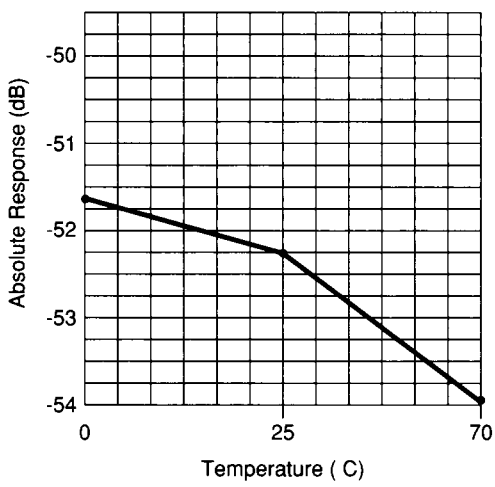

Figure 20. 1010 Notch 1 kHz Response Plot versus Temperature

Table 1. Pin Description

Sym	Pin No.	Description
-	1	Not connected
PW Out	2	Program weighting filter output capable of driving resistances >20 KΩ
OP1-	3	Op amp 1 inverting input
OP1+	4	Op amp 1 noninverting input
OP1 Out	5	Op amp 1 output
V_{DD}	6	Positive voltage supply
-	7	Not connected
OP2+	8	Op amp 2 noninverting input
OP2-	9	Op amp 2 inverting input
OP2 Out	10	Op amp 2 output
Notch In	11	1010 Hz Notch filter input
Notch Out	12	1010 Hz Notch filter output
OP3-	13	Op amp 3 inverting input
OP3+	14	Op amp 3 noninverting input
OP3 Out	15	Op amp 3 output
Xtal In	16	Connection to crystal or to external clock (CMOS or TTL)
Xtal Out	17	Connection to crystal or open
-	18	Not connected
V_{SS}	19	Negative voltage supply
DGD	20	Digital ground; must be at $(V_{DD} + V_{SS})/2$
AGD	21	Analog ground; must be at $(V_{DD} + V_{SS})/2$
CM In	22	C-Message filter input
CM Out	23	C-Message filter output
PW In	24	Program weighting filter input

Table 2. Guaranteed Device Characteristics

@ 25°C, V_{DD} = 5V, V_{SS} = -5V, f_c = 3.58 MHz (unless otherwise indicated)

Parameter	Sym	Conditions and Comments	Min	Typ	Max	Unit
Supply voltages	V_{DD}	Symmetrical (split) supplies	+4.5	+5	+5.5	V DC
	V_{SS}		-4.5	-5	-5.5	V DC
Supply currents	I_{DD}	No load			20	mA
	I_{SS}		No load	-20		mA
Input clock levels [1,2]	V_{IL}	Low level (reference is DGD)	V_{SS}		0.8	V DC
	V_{IH}	High level	2.2		V_{DD}	V DC
Output signal	V_o [1]		V_{SS} +1.5		V_{DD} -1.5	V DC
Output load	C_{OUT} [1]	Output load capacitance			50	pF
	R_{Out} [1]	Output load resistance	20			KΩ
Output noise	e_n	1010 Hz notch	-		0.4	mV_{rms}
		Program weighting	-		0.4	mV_{rms}
		C-Message (15 kHz bandwidth, offset not included)	-		0.4	mV_{rms}
Dynamic range	DR	All filters	75	-	-	dB
Crosstalk		All filters	70	-	-	dB
Total harmonic distortion	THD [5]	1010 Hz Notch (V_{in} = 1 V_{rms})			0.3	%
		Program weighting (V_{in} = 1 V_{rms})			0.3	%
		C-Message (1 kHz)			0.3	%
Clock feedthrough	CF	All filters	-		10	mV_{rms}
1010 notch response		0 to 400 Hz	-0.5		0.5	dB
		400 to 862 Hz [4]	-3		0.5	dB
		995 to 1025 Hz			-50.0	dB
		1182 to 1700 Hz	-3		0.5	dB
		>1700 Hz	-0.5		0.5	dB
Program weighting response [3]		200 Hz	-19.5		-15.5	dB
		400 Hz	-11.0		-7.0	dB
		1000 Hz	-1.0		+1.0	dB
		4000 Hz	5.5		7.5	dB
		8000 Hz	1.0		7.0	dB
C-Message response		100 Hz	-44.5		-40.5	dB
		200 Hz	-27.0		-23.0	dB
		300 Hz	-18.5		-14.5	dB
		500 Hz	-8.5		-6.5	dB
		1000 Hz	-0.2		0.2	dB
		1500 Hz	-2.2		-0.2	dB
		2000 Hz	-2.0			dB
		3000 Hz	-5.0		-1.0	dB
		5000 Hz	-31.5		-25.5	dB
Output DC offset		1010 Hz notch	-50		50	mV
		Program weighting	-300		300	mV
		C-Message	-50		50	mV
Operational amplifier characteristics [1]		Output voltage swing	2.4	-	-	V_{rms}
		Open loop gain		80		dB
		Bandwidth		1		MHz
	C_{Out}[1]	Output load capacitance	-	-	50	pF
	R_{Out}[1]	Output load resistance	20	-	-	KΩ

Notes:

1 Guaranteed by design, not tested.

2 TTL input clock must be used only with symmetrical (split) ±5V power supplies. CMOS input clock or crystal can be used with either split supplies or a single +10V supply.

3 Program weighting filter input voltage should not exceed 1.3V_{rms}.

4 For version RF6651ANP-020, the maximum response in this range is +0.75 dB.

5 Measurement made at 1 kHz, f_c = 1.19 MHz which is equivalent to the response at 3 kHz.

Table 3. Specifications at 0°C and 70°C [1]
(V_{DD} = 5V, V_{SS} = -5V, f_c = 3.58 MHz)

Parameter	Sym	0°		70°C		Units
		Min	Max	Min	Max	
Supply current	I_{DD}		27.5		20	mA
	I_{SS}	-27.5		-20		
Output noise (C-Message)	e_n		0.4		0.5	mV_{rms}
1010 notch response						
400 - 862 Hz		-3	0.8	-3	0.7	dB
995 - 1025 Hz			-48		-48	dB
Program weighting response						
200 Hz		-21.0	-15.5	-20.5	-15.5	dB
C-Message response						
100 Hz		-45.5	-36.5	-45.5	-36.5	dB
200 Hz		-27.5	-22.0	-27.5	-22.0	dB
300 Hz		-18.5	-14.0	-18.5	-14.0	dB
500 Hz		-8.5	-6.5	-8.5	-6.5	dB
5000 Hz		-31.5	-25.5	-31.5	-25.5	dB

Note:
[1] Specifications not listed in Table 3 are identical to those in Table 2.

Table 4. Absolute Minimum/Maximum Ratings

	Min	Max	Units
Input voltage — any terminal with respect to substrate	-0.4	15	V
Output short-circuit duration — any terminal	Indefinite		
Operating temperature	0	70	°C
Storage temperature	-55	125	°C
Lead temperature (soldering, 10 sec.)		300	°C

Caution: Observe MOS Handling and Operating Procedures

Note: This table shows stress ratings *exclusively*. Functional operation of this product under any conditions beyond those listed under standard operating conditions is not suggested by the table. Permanent damage may result if the device is subject to stresses beyond these absolute min/max values. Moreover, reliability may be diminished if the device is run for protracted periods at absolute maximum values.

Although devices are internally gate-protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/ on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

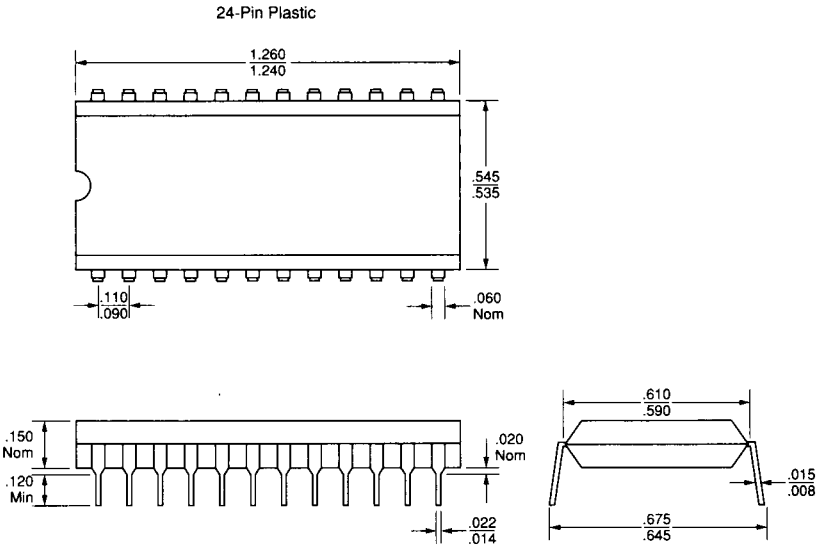

Figure 21. Package Dimensions

Ordering Information

Part Number	Description of Part
RF6651ANP-011	IEEE specification at 25°C
RF6651ANP-020	IEEE specification at 25°C with relaxed notch filter specification
RF6651ANP-012	IEEE specification at 25°C. Tested at 0°C and 70°C

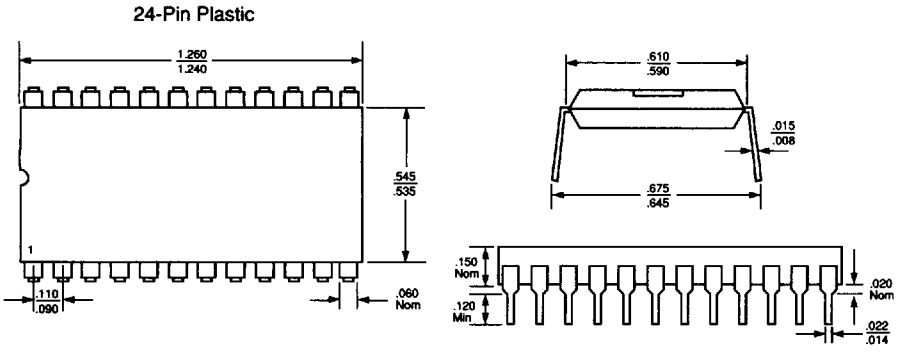

Figure 6. Package Dimensions

Ordering Information

Part Number	Description
RF5651ANP-011	Triple filter combination, including C-Message filter, program weighting filter, and 1010 Hz notch filter