DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD98401

LOCAL ATM SAR CHIP

The μPD98401 is a high performance ATM segmentation and reassembly chip (SAR chip), designed to be used by workstations, computers, front-end processors, network hubs and routers for interfacing to an ATM network. The chip conforms to ITU-TS, ANSI and the ATM Forum recommendations and implements the required AAL-5 SAR sublayer and ATM layer functions.

FEATURES

- Conforms to ITU-TS, T1S1 and the ATM Forum UNI3.1 recommendations
- Implements the required AAL-5 SAR sublayer and ATM layer functions
- AAL-5 adaptation layer supported in hardware
- Software support of non-AAL-5 traffic
- Hardware support of CRC-10 for non-AAL-5 traffic
- Supports up to 32K virtual channels (VCs)
- 16 traffic shapers for transmission scheduling (controlling the average/peak rate), enabling fine-grain rate setting per VC
- 32-bit general-purpose bus interface
- High-speed DMAC
- UTOPIA interface with physical layer
- CMOS technology
- Single +5 V supply
- 208-pin plastic QFP (fine pitch)

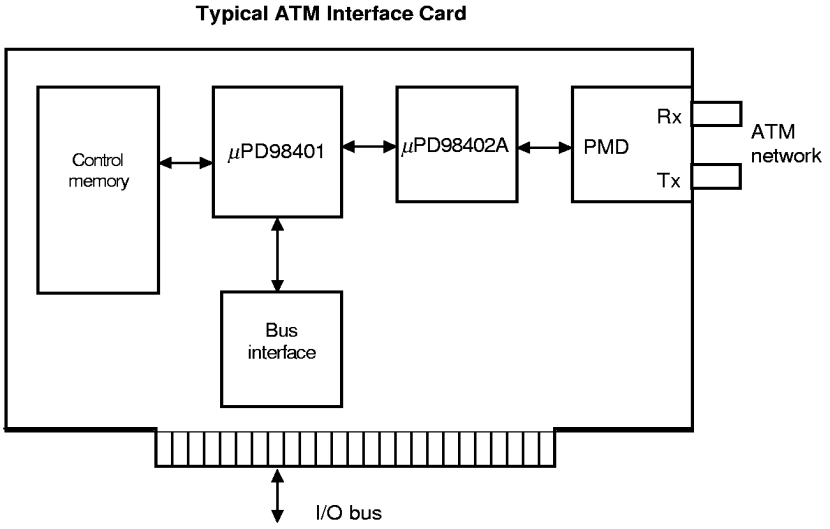
ORDERING INFORMATION

Part Number	Package
μPD98401GD-MML	208-pin plastic QFP (fine pitch) (28 x 28 mm)

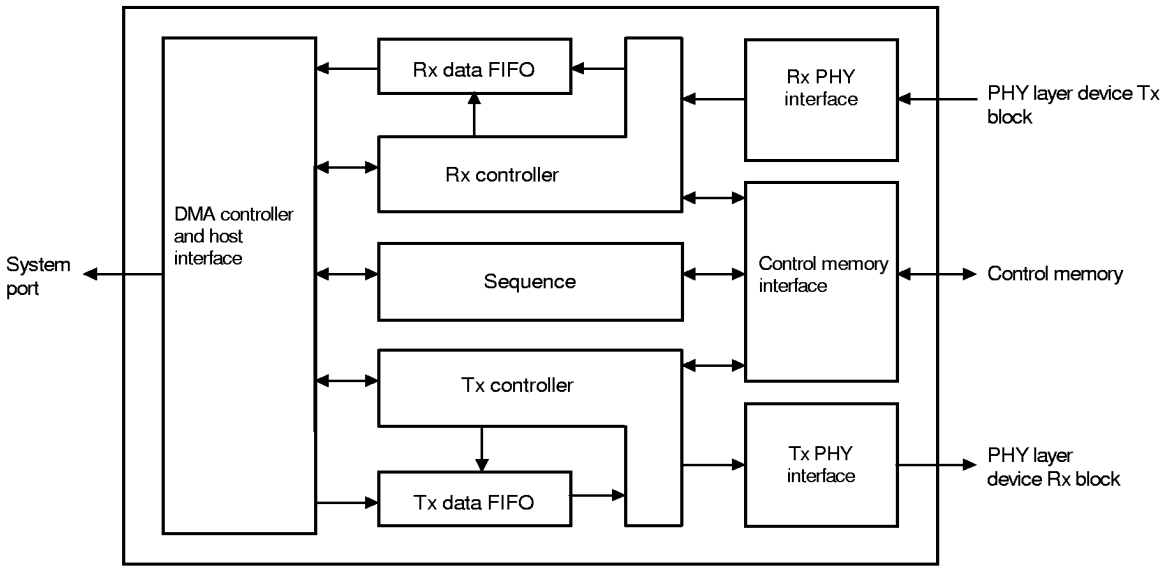
Note The electrical characteristics described in this document apply only to μPD98401 Ver. 4.4 (H-standard product).

The information in this document is subject to change without notice.

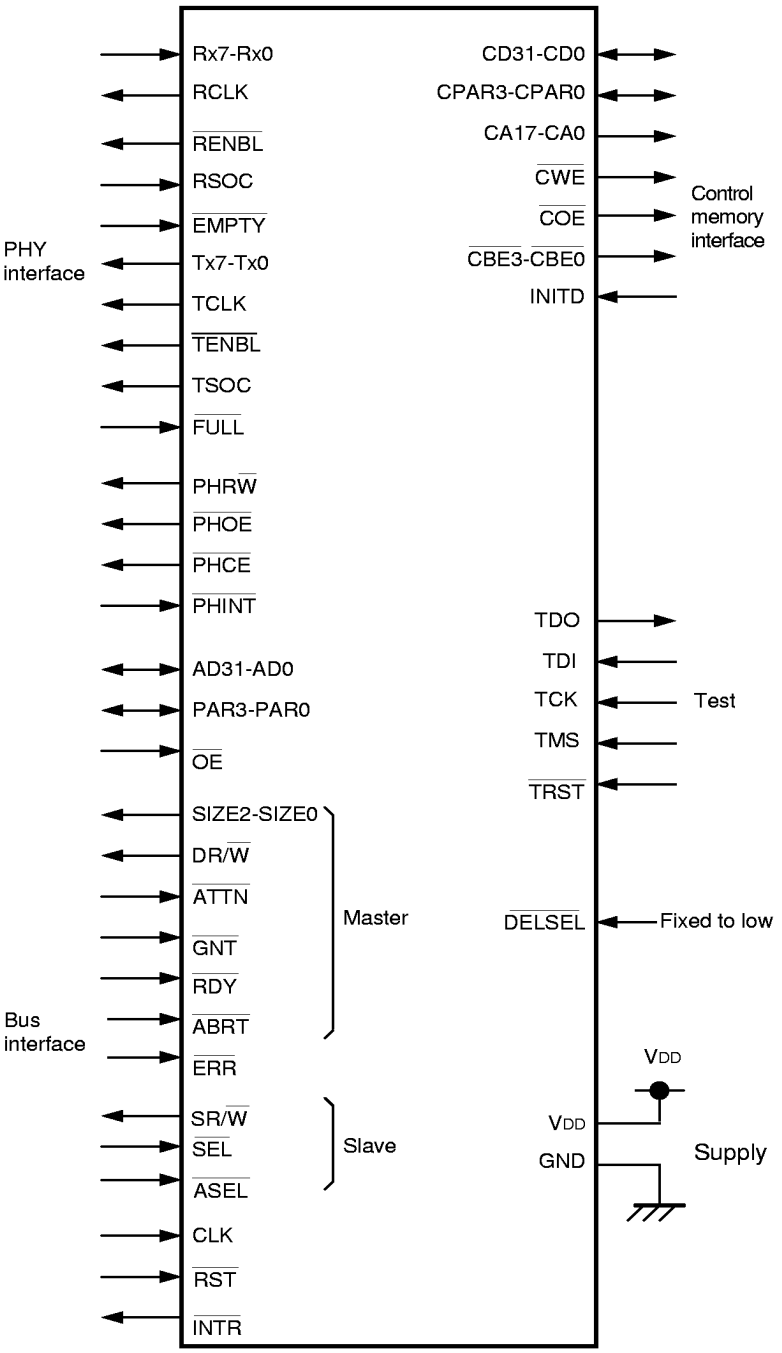
APPLICATION EXAMPLE



BLOCK DIAGRAM



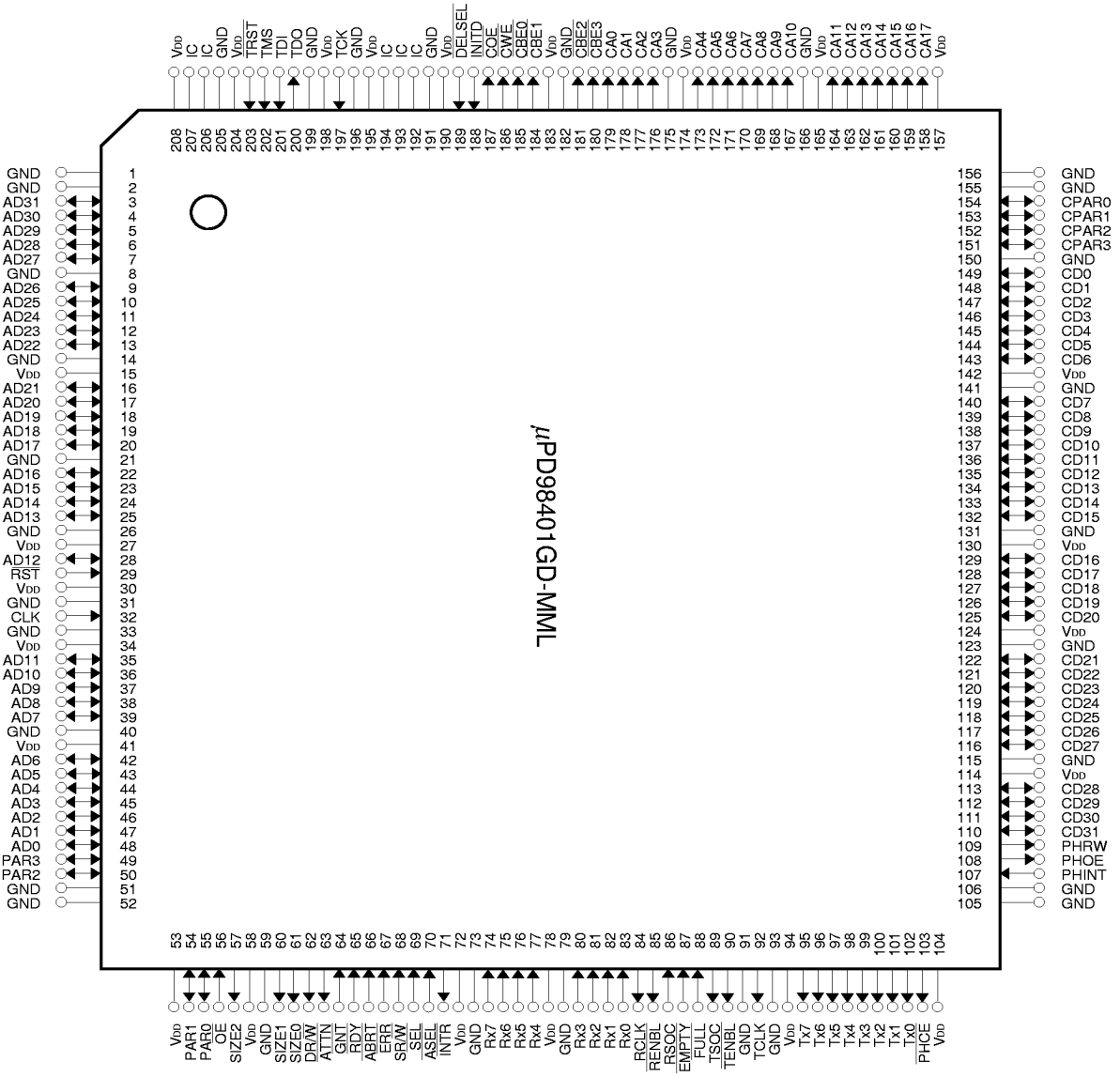
FUNCTIONAL PIN GROUPS



Remark	PHY interface	:	28	pins
	Bus interface	:	52	pins
	Control memory interface	:	61	pins
	Test	:	5	pins
	Others	:	1	pin
	Total	:	147	signal pins

[MEMO]

PIN CONFIGURATION (Top View)



IC: Internally connected. Leave open.

$\overline{\text{ABRT}}$	:Abort	$\overline{\text{PHCE}}$	:PHY Chip Enable
AD31-AD0	:Address/Data	$\overline{\text{PHINT}}$	:PHY Interrupt
$\overline{\text{ASEL}}$	:Slave Address Select	$\overline{\text{PHOE}}$	:PHY Output Enable
$\overline{\text{ATTN}}$	:Attention/Burst Frame	PHR$\overline{\text{W}}$	:PHY Read/Write
CA17-CA0	:Control Memory Address	RCLK	:Receive Clock
$\overline{\text{CBE3}}$-$\overline{\text{CBE0}}$	:Local Port Byte Enable	$\overline{\text{RDY}}$	:Target Ready
CD31-CD0	:Control Memory Data	$\overline{\text{RENBL}}$	:Receive Enable
CLK	:Clock	RSOC	:Receive Start Cell
$\overline{\text{COE}}$	:Control Memory Output Enable	$\overline{\text{RST}}$	:Reset
CPAR3-CPAR0	:Control Memory Parity	Rx7-Rx0	:Receive Data Bus
$\overline{\text{CWE}}$	:Control Memory Write Enable	$\overline{\text{SEL}}$	:Slave Select
$\overline{\text{DELSEL}}$	:Delay Select	SIZE2-SIZE0	:Burst Size
DR/$\overline{\text{W}}$	:DMA Read/Write	SR/$\overline{\text{W}}$	:Slave Read/Write
$\overline{\text{EMPTY}}$	:PHY Output Buffer Empty	TCK	:Test Pin
$\overline{\text{ERR}}$	:Error	TCLK	:Test Pin
$\overline{\text{FULL}}$	:PHY Buffer Full	TDI	:Test Pin
GND	:Ground	TDO	:Test Pin
$\overline{\text{GNT}}$	:Grant	$\overline{\text{TENBL}}$	:Transmit Enable
IC	:Internal Connect	TMS	:Test Pin
INITD	:Initialization Disable	$\overline{\text{TRST}}$	:Test Pin
$\overline{\text{INTR}}$	:Interrupt	TSOC	:Transmit Start of Cell
$\overline{\text{OE}}$	:Output Enable	Tx7-Tx0	:Transmit Data Bus
PAR3-PAR0	:Bus Parity	V_{DD}	:Power Supply

1. Pin Functions

The μPD98401 is packaged in a 208-pin package. It has 147 functional pins, 56 V_{DD} and GND pins, and 5 IC pins. Refer to **Chapter 4** of the μPD98401 User's Manual for details of the pin functions and notes on use.

PHY layer device interface signals

Signals for interfacing with the PHY layer device are classified into those used to transfer ATM cells between the μPD98401 and PHY layer device and those used to control the PHY layer device.

The μPD98401 supports the octet-level UTOPIA interface.

(1/2)

Symbol	Pin No.	I/O	I/O level	Function
Rx7-Rx4 Rx3-Rx0	74 - 77, 80 - 83	I	TTL	Receive Data Bus Rx7-Rx0 is an 8-bit input bus used to receive the network traffic in byte form from the PHY layer device. The eight bits are input to the μPD98401 in synchronization with the rising edge of RCLK.
RSOC	86	I	TTL	Receive Start of Cell The RSOC signal is input in synchronization with the first byte of cell data received from the PHY layer device. Keep this signal high while the first byte of the header is being input to Rx7-Rx0.
$\overline{\text{RENBL}}$	85	O	CMOS	Receive Enable The $\overline{\text{RENBL}}$ signal indicates to the PHY layer device that the μPD98401 is ready to accept data in the next clock cycle. This signal is set to high during and immediately after reset.
$\overline{\text{EMPTY}}$	87	I	TTL	PHY Output Buffer Empty The $\overline{\text{EMPTY}}$ signal indicates to the μPD98401 that the receive FIFO of the PHY layer device is empty and cannot provide receive data at this time.
RCLK	84	O	CMOS	Receive Clock The RCLK signal is a clock used to synchronize the reception of cell data from the PHY layer device. Once the system has been reset, the system clock, input to the CLK pin, is output as is.
Tx7-Tx 0	95 - 102	O	CMOS	Transmit Data Bus Tx7-Tx0 is an 8-bit output bus used to transmit the network traffic in byte form to the PHY layer device. The eight bits are output to the PHT layer device in synchronization with the rising edge of TCLK.

(2/2)

Symbol	Pin No.	I/O	I/O level	Function
TSOC	89	O	CMOS	Transmit Start of Cell The TSOC signal is output in synchronization with the first byte of cell data to be transmitted to the PHY layer device.
$\overline{\text{TENBL}}$	90	O	CMOS	Transmit Enable The $\overline{\text{TENBL}}$ signal indicates to the PHY layer device that Tx7 to Tx0 carries transmit data in the current clock cycle. This signal is held high during reset and set to low once reset has been completed.
$\overline{\text{FULL}}$	88	I	TTL	PHY Layer Buffer Full The $\overline{\text{FULL}}$ signal indicates to the μPD98401 that the input buffer of the PHY layer device is full and can not accept additional data.
TCLK	92	O	CMOS	Transmit Clock The TCLK signal is a clock used to synchronize the transmission of cell data to the PHY layer device. The system clock, input to the CLK pin, is output as is.
PHR$\overline{\text{W}}$	109	O	CMOS	PHY Read/Write The PHR$\overline{\text{W}}$ is asserted by the μPD98401 to indicate the direction of the PHY control transaction. This signal is set to low once the system has been reset. 1: Read 0: Write
$\overline{\text{PHOE}}$	108	O	CMOS	PHY Layer Output Enable The $\overline{\text{PHOE}}$ is asserted by the μPD98401 to enable data output from the PHY layer device.
$\overline{\text{PHCE}}$	103	O	CMOS	PHY Layer Chip Enable The $\overline{\text{PHCE}}$ is asserted by the μPD98401 when it accesses the PHY layer device. This signal is set to high once the system has been reset.
$\overline{\text{PHINT}}$	107	I	TTL	PHY Layer Interrupt The $\overline{\text{PHINT}}$ pin accepts an interrupt signal from the PHY layer device. If any interrupt occurs in the PHY layer device, it notifies the μPD98401 of the interrupt by driving $\overline{\text{PHINT}}$ low. This signal is set to high once the system has been reset.

Bus interface signals

The μPD98401 supports a general-purpose bus interface, optimized for the most commonly used I/O buses (e.g.: PCI, S bus, GIO and AP bus).

(1/3)

Symbol	Pin No.	I/O	I/O level	Function
AD31-AD27, AD26-AD22, AD21-AD17, AD16-AD13, AD12, AD11- AD7, AD6-AD0	3-7, 9 - 13, 16 - 20, 22 - 25, 28 35 - 39, 42 - 48	I/O 3-state	TTL in, CMOS out	Address/Data The AD31 to AD0 bus is a 32-bit, bi-directional, multiplexed address/data bus. During the first clock of a transaction, AD31 to AD0 contains a physical byte address. During subsequent clocks, AD31 to AD0 contains data. When the μPD98401 is not accessing the bus, it places the AD bus in the high impedance state.
PAR3 PAR2 PAR1 PAR0	49 50 54 55	I/O 3-state	TTL in, CMOS out	Bus Parity The PAR indicates the parity across AD31 to AD0. Parity checking is configured by setting the appropriate bits in the GMR. Parity checking may be enabled/disabled, even/odd, byte or word. When configured as byte parity, PAR3 represents AD31 to AD24 while PAR0 represents AD7 to AD0. When configured as word parity, PAR3 is a bi-directional signal: an output during address and write data phases and input during read data phases. When the μPD98401 is not accessing the bus it places PAR3 to PAR0 in the high impedance state. Connect a pull-up resistor when unused.
$\overline{OE}$	56	I	TTL	Output Enable When the $\overline{OE}$ signal is low, the μPD98401 controls AD31 to AD0 and PAR3 and PAR0 as 3-state bidirectional pins (normal operation). When the $\overline{OE}$ signal is high, these pins are placed in the high impedance state. This signal is optional. Fix it to low unless the above pins need be forcibly set to high impedance.
SIZE2 SIZE1 SIZE0	57 60 61	O	CMOS	Burst Size The SIZE2 to SIZE0 signals indicate the size of the current DMA transfer. These signals are provided to support interface to buses that require an explicit burst size (e.g., S bus).

SIZE2	SIZE1	SIZE0	Function
0	0	0	One-word transfer
0	0	1	Two-word burst
0	1	0	Four-word burst
0	1	1	Eight-word burst
1	0	0	Sixteen-word burst
Others			Reserved

(2/3)

Symbol	Pin No.	I/O	I/O level	Function
DR/$\overline{W}$	62	O	CMOS	DMA Read/Write The DR/$\overline{W}$ signal determines the direction of DMA access. 1: Read access 0: Write access This signal is set to 1 once the system has been reset.
$\overline{ATTN}$	63	O	CMOS	Attention The μPD98401 asserts the $\overline{ATTN}$ signal when attempting to start DMA operation. Once only one word remains to be transferred, the $\overline{ATTN}$ signal is deasserted at the rising edge of CLK.
$\overline{GNT}$	64	I	TTL	Grant Set the $\overline{GNT}$ signal to low once the bus arbiter has granted bus mastership in response to a DMA request from the μPD98401. By detecting the $\overline{GNT}$ signal being set to low, the μPD98401 assumes that bus mastership has been granted and starts DMA operation. The $\overline{GNT}$ signal must not be set to low until at least one system clock cycle has elapsed after the $\overline{ATTN}$ rising edge. The $\overline{GNT}$ signal must be set to high before the μPD98401 drives the $\overline{ATTN}$ signal to low to request the next DMA cycle.
$\overline{RDY}$	65	I	TTL	Target Device Ready $\overline{RDY}$ is used in DMA cycles to indicate to the μPD98401 that the transaction's target device is ready to input/output data. During the μPD98401 DMA read operation, the $\overline{RDY}$ signal should be asserted when valid data is present on AD31 to AD0. During the μPD98401 DMA write operation, the $\overline{RDY}$ signal should be asserted when the target device is ready to accept data. The timing at which the μPD98401 samples the $\overline{RDY}$ and $\overline{ABRT}$ signals can be changed to one clock earlier (early mode) by setting an internal register (GMR).
$\overline{ABRT}$	66	I	TTL	Abort $\overline{ABRT}$ is used to abort a data transfer cycle. When this signal is asserted during the data transfer cycle, the cycle is aborted and the μPD98401 will retry the burst starting from the aborted data. Note that the $\overline{RDY}$ signal has no effect if the $\overline{ABRT}$ signal is asserted. The timing at which the μPD98401 samples the $\overline{RDY}$ and $\overline{ABRT}$ signals can be changed to one clock earlier (early mode) by setting an internal register (GMR). Connect a pull-up resistor when the ABRT pin is not used.

(3/3)

Symbol	Pin No.	I/O	I/O level	Function
$\overline{ERR}$	67	I	TTL	System Bus Error The $\overline{ERR}$ signal is used by the bus control device to request the μPD98401 to halt operation if an error is detected on the system bus. Once this signal has been set to low, the μPD98401 immediately halts all bus operations, sets the system bus error bit (bit 25) in the GSR (if not masked), and generates an interrupt. Connect a pull-up resistor when this pin is not used.
SR/$\overline{W}$	68	I	TTL	Slave Read/Write The SR/$\overline{W}$ signal determines the direction of slave access. 1: Read access 0: Write access
$\overline{SEL}$	69	I	TTL	Slave Select Assert the $\overline{SEL}$ signal when selecting the μPD98401 as a slave. The $\overline{SEL}$ signal can be asserted either at the same time as the assertion of the $\overline{ASEL}$ signal, or subsequently. Once the $\overline{SEL}$ signal has been deasserted, it must be held inactive for at least two system clock cycles before it can be reasserted.
$\overline{ASEL}$	70	I	TTL	Slave Address Select The $\overline{ASEL}$ signal is used to select the μPD98401 directly addressed registers. When $\overline{ASEL}$ is asserted, the μPD98401 samples the AD lines at the first rising edge of CLK.
CLK	32	I	TTL	Clock CLK is the system clock. The clock range is 8 to 33 MHz.
$\overline{RST}$	29	I	TTL	Reset The $\overline{RST}$ signal provides a means of initializing the μPD98401 (i.e. on power up). When it is deasserted, the μPD98401 is ready to begin its normal operation. When asserted, $\overline{RST}$ resets the μPD98401 internal state machines and registers, and forces all 3-state signals to the high impedance state. Assertion and deassertion are asynchronous. If asserted during operation, current state will be lost. $\overline{RST}$ should be asserted for at least 10 clock cycles.
$\overline{INTR}$	71	O	N-ch open-drain output	Interrupt Output It is an open-drain pin and needs pull-up resistor connection. The $\overline{INTR}$ output is used to inform the CPU that an (unmasked) interrupt bit was set in the GSR.

Control memory interface

The control memory interface is used by the μPD98401 to enable access to the external control memory and PHY layer device. The interface consists of non-multiplexed 18-bit address and 32-bit data buses. The host can access control memory only via this interface.

Symbol	Pin No.	I/O	I/O level	Function
CD31-CD28 CD27-CD21 CD20-CD16 CD15-CD7 CD6-CD0	110-113 116-122 125-129 132-140 143-149	I/O 3-state	TTL in, CMOS out	Control Memory Data The CD31 to CD0 bus is a 32-bit, bi-directional, 3-state data bus used to transfer data to and from the control memory or the PHY layer device.
CPAR3- CPAR0	151-154	I/O	TTL in, CMOS out	Control Memory Parity The CPAR3 to CPAR0 signals indicate the parity on each octet of the CD31 to CD0 bus. The μPD98401 checks parity during read cycles (if enabled) and generates parity during write cycle. Connect pull-up resistors when these pins are not used.
CA17-CA11 CA1-CA4 CA3-CA0	158-164 167-173 176-179	O	CMOS	Control Memory Address The 18-bit CA17 to CA0 bus specifies the address of the control memory or PHY layer device for a read or write operation.
$\overline{\text{CWE}}$	186	O	CMOS	Control Memory Write Enable The $\overline{\text{CWE}}$ signal determines the direction of control memory access. 1: Read access 0: Write access
$\overline{\text{COE}}$	187	O	CMOS	Control Memory Output Enable The $\overline{\text{COE}}$ signal enables/disables the control memory data output lines.
$\overline{\text{CBE3}}$ $\overline{\text{CBE2}}$ $\overline{\text{CBE1}}$ $\overline{\text{CBE0}}$	180 181 184 185	O	CMOS	Local Port Byte Enable The $\overline{\text{CBE3}}$ to $\overline{\text{CBE0}}$ signals determine which byte or bytes out of the four on the control port is to be written in write cycle, and which of the bytes is read in read cycle.
INITD	188	I	TTL	Initialization Disable The INITD signal is used to disable automatic initialization of the control memory when testing the chip. INITD must be directly connected to GND in normal operation other than testing.

Test signals

Symbol	Pin No.	I/O	I/O level	Function
TDI	201	I	TTL	Test pin For normal operation, connect directly to ground.
TDO	200	O	CMOS	Test pin For normal operation, leave open.
TCK	197	I	TTL	Test pin For normal operation, connect directly to ground.
TMS	202	I	TTL	Test pin For normal operation, connect directly to ground.
$\overline{\text{TRST}}$	203	I	TTL	Test pin For normal operation, connect directly to ground.

Other signals

Symbol	Pin No.	I/O	I/O level	Function
$\overline{\text{DELSEL}}$	189	I	TTL	Delay Select This pin is used at the factory to change the internal signal timing during testing. This pin must be connected directly to ground, so that it is fixed to low, during normal operation.

Power and ground

Symbol	Pin No.	I/O	Function
V_{DD}	15, 27, 3, 34, 41, 53, 58, 72, 78, 94, 104, 114, 124, 130, 142, 157, 165, 174, 183, 190, 195, 198, 204, 208	-	Power Supply (24 pins) These 24 V_{DD} pins supply +5 ±5 % V to the chip.
GND	1, 2, 8, 14, 21, 26, 31, 33, 40, 51, 52, 59, 73, 79, 91, 93, 105, 106, 115, 123, 131, 141, 150, 155, 156, 166, 175, 182, 191, 196, 199, 205	-	Ground (32 pins) These 32 GND pins ground the chip.

2. ELECTRICAL CHARACTERISTICS

Note The electrical characteristics described below apply only to μPD98401 Ver. 4.4 (H-standard product).

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +6.5	V
Input voltage	V_I		–0.5 to V_{DD} + 0.5	V
Operating temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

DC Characteristics (T_A = 0 to +70 °C, V_{DD} = 5 V ±5 %)

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Low-level input voltage	V_{IL}		–0.5		+0.8	V	
High-level input voltage	V_{IH1}	Other than $\overline{RST}$ and CLK	+2.2		V_{DD} + 0.5	V	*
	V_{IH2}	$\overline{RST}$ and CLK pins	+3.3		V_{DD} + 0.5		*
High-level output voltage	V_{OH1}	I_{OH} = –2.0 mA Note 1	V_{DD} × 0.7			V	
	V_{OH2}	I_{OH} = –4.0 mA Note 2	V_{DD} × 0.7			V	
	V_{OH3}	I_{OH} = –6.0 mA Note 3	V_{DD} × 0.7			V	
Low-level output voltage	V_{OL1}	I_{OL} = 4.0 mA Note 1			+0.4	V	
	V_{OL2}	I_{OL} = 8.0 mA Note 2			+0.4	V	
	V_{OL3}	I_{OL} = 12.0 mA Note 3			+0.4	V	
Supply current	I_{DD}	Normal operation		370	570	mA	*
Input leakage current	I_{LI}	V_I = V_{DD} or GND			±10	μA	
Output leakage current	I_{OZ}	V_O = V_{DD} or GND			±10	μA	

Notes 1. V_{OH1} and V_{OL1} are applicable to the following pins.
RCLK, $\overline{RENBL}$, TSOC, $\overline{TENBL}$, TCLK, Tx7 - Tx0, $\overline{PHCE}$, $\overline{PHOE}$, PH$\overline{RW}$

2. V_{OH2} and V_{OL2} are applicable to the following pins.
CD31 - CD0, CPAR3 - CPAR0, CA17 - CA0, $\overline{CBE3}$ - $\overline{CBE0}$, $\overline{CWE}$, $\overline{COE}$

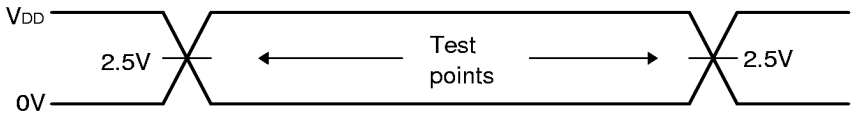
3. V_{OH3} and V_{OL3} are applicable to the following pins.
AD31 - AD0, PAR3 - PAR0, SIZE2 - SIZE0, DR/$\overline{W}$, $\overline{ATTN}$, $\overline{INTR}$

DC Characteristics (T_A = 0 to +70 °C, V_{DD} = 5 V ±5 %)

Capacitance

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output pin capacitance	C_O	f = 1 MHz		10	20	pF
Input pin capacitance	C_I	f = 1 MHz		10	20	pF
Input/output pin capacitance	C_{IO}	f = 1 MHz		10	20	pF

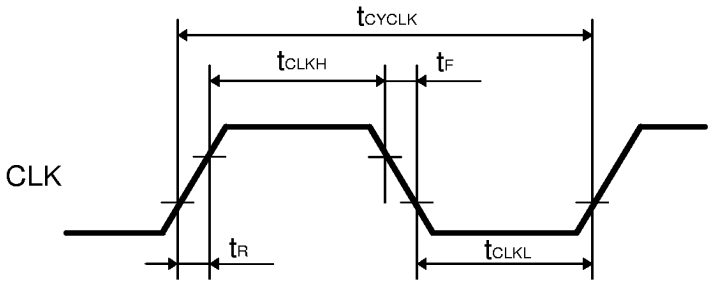
AC Testing Input/Output Waveform



AC Characteristics (T_A 0 to +70 °C, V_{DD} = 5 V ±5 %)

CLK Input

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit	
CLK cycle time	t_{CYCLK}		30		125	ns	
CLK high level width	t_{CLKH}		12			ns	
CLK low level width	t_{CLKL}		12			ns	
CLK rising time	t_R				3	ns	*
CLK falling time	t_F				3	ns	*



PHY Interface

Transmit Operation

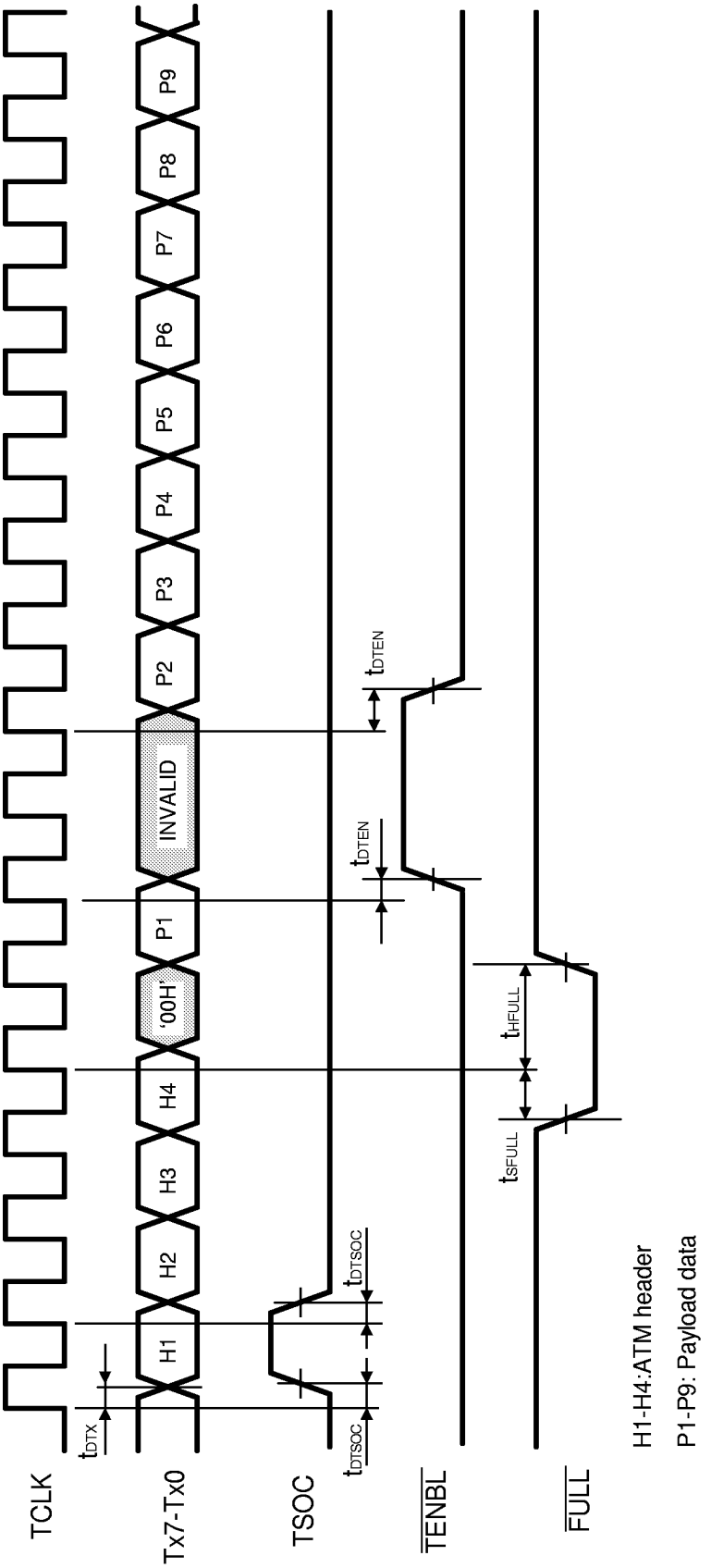
Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit	
CLK↑→TCLK↑ delay	t_{DTCLK}			6.5		ns	*
TCLK↑→Tx delay	t_{DTX}		3		18	ns	
TCLK↑→TSOC↑ delay	t_{DTSOC}		3		18	ns	
TCLK↑→$\overline{\text{TENBL}}$↑ delay	t_{DTEN}		3		18	ns	*
$\overline{\text{FULL}}$ setup time	t_{SFULL}		10			ns	*
$\overline{\text{FULL}}$ hold time	t_{HFULL}		1			ns	*

Receive Operation

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit	
CLK↑→RCLK↑ delay	t_{DRCLK}			7		ns	*
Rx setup time	t_{SRX}		10			ns	*
Rx hold time	t_{HRX}		1			ns	*
RSOC setup time	t_{SRSOC}		10			ns	*
RSOC hold time	t_{HRSOC}		1			ns	*
RCLK↑→$\overline{\text{RENBL}}$↑ delay	t_{DREN}		3		18	ns	
$\overline{\text{EMPTY}}$ setup time	t_{SEMPT}		10			ns	*
$\overline{\text{EMPTY}}$ hold time	t_{HEMPT}		1			ns	*

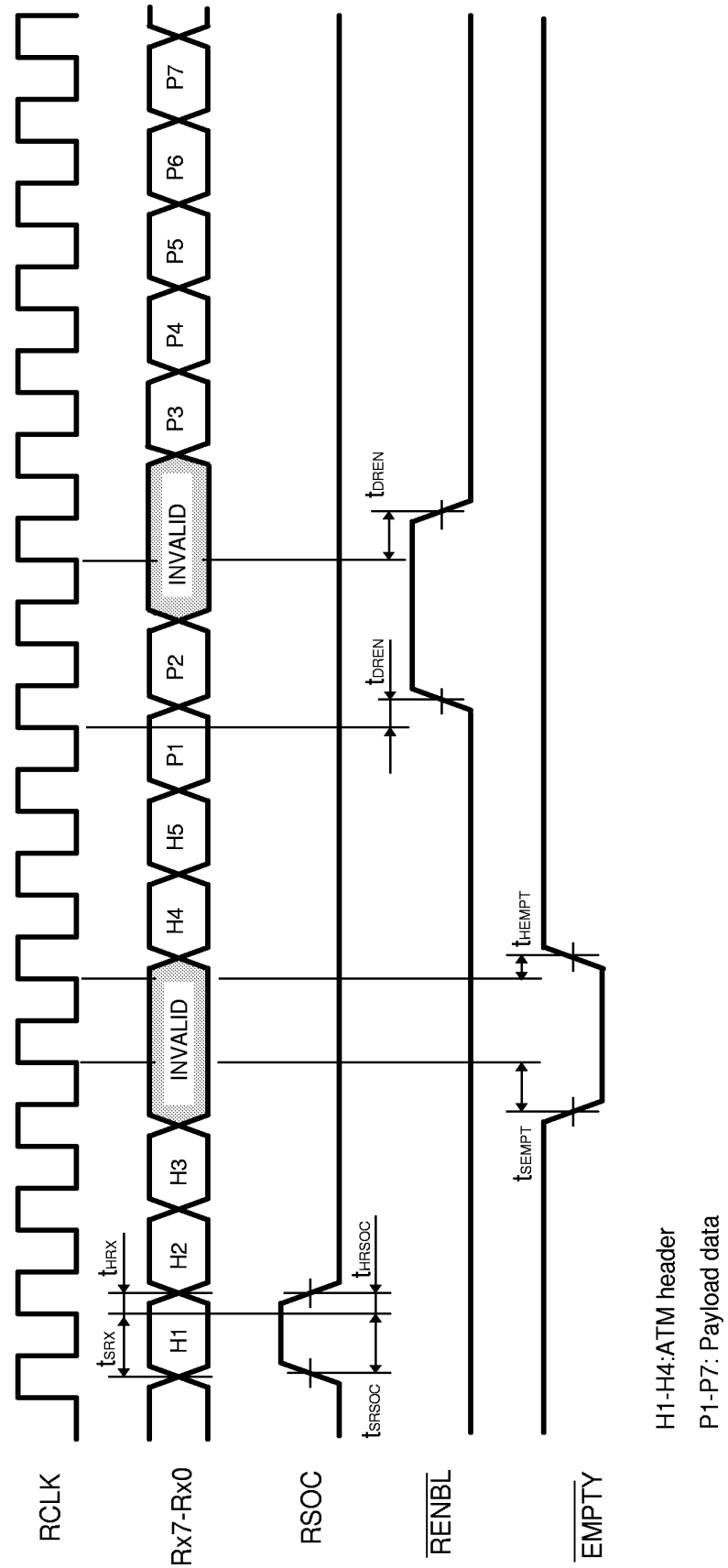
PHY Interface (1)

Transmission Timing



PHY Interface (2)

Reception Timing



H1-H4:ATM header

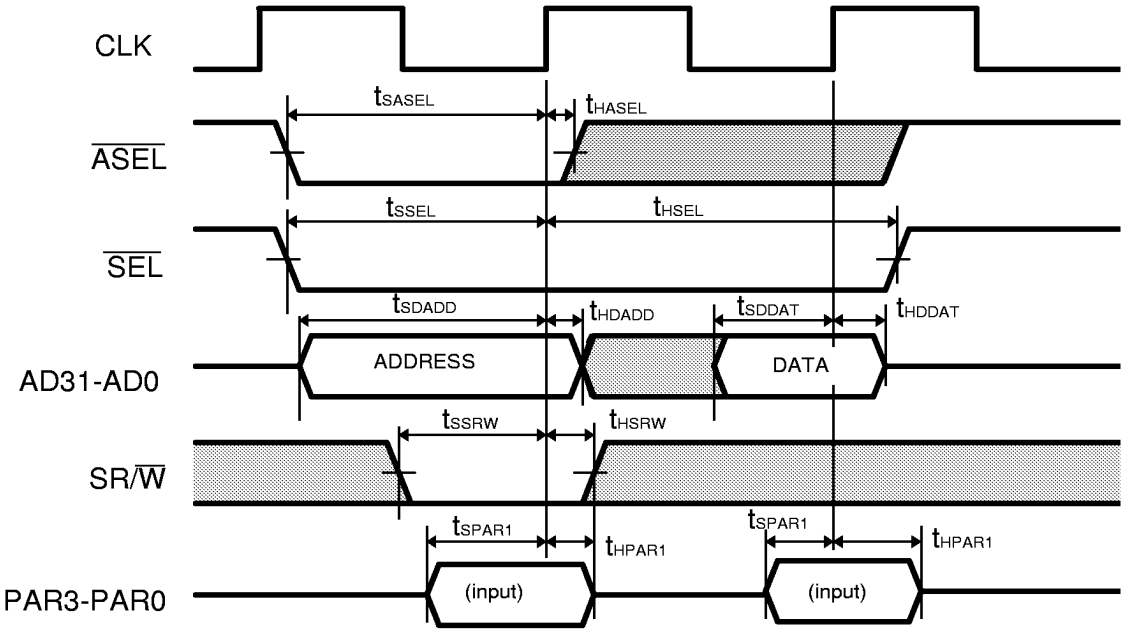
P1-P7: Payload data

Host Slave Access (1)

Write

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit	
$\overline{ASEL}$ setup time	t_{SASEL}		8			ns	
$\overline{ASEL}$ hold time	t_{HASEL}		3			ns	
$\overline{SEL}$ setup time	t_{SSEL}		8			ns	
$\overline{SEL}$ hold time	t_{HSEL}		$1t_{CYCLK}+3$			ns	
Address setup time	t_{SDADD}		8			ns	
Address hold time	t_{HDADD}		3			ns	*
Data setup time	t_{SDDAT}		8			ns	
Data hold time	t_{HDDAT}		3			ns	*
PAR setup time	t_{SPAR1}		8			ns	
PAR hold time	t_{HPAR1}		3			ns	
SR/$\overline{W}$ setup time	t_{SSRW}		8			ns	
SR/$\overline{W}$ hold time	t_{HSRW}		3			ns	

Write Timing



Host Slave Access (2)

Read

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit	
$\overline{ASEL}$ setup time	t_{SASEL}		8			ns	
$\overline{ASEL}$ hold time	t_{HASEL}		3			ns	
$\overline{SEL}$ setup time	t_{SSEL}		8			ns	
$\overline{SEL}$ hold time	t_{HSEL}		$1t_{CYCLK}+3$			ns	
Address setup time	t_{SDADD}		8			ns	
Address hold time	t_{HDADD}		3			ns	*
CLK↑→ data delay	t_{DDDAT}				20	ns	*
CLK↑→ data float time	t_{FDDAT}		3		18	ns	*
PAR setup time	t_{SPAR1}		8			ns	
PAR hold time	t_{HPAR1}		3			ns	
CLK↑→ PAR delay	t_{DPAR1}				20	ns	*
CLK↑→ PAR float time	t_{FPAR1}		3		18	ns	*
SR/$\overline{W}$ setup time	t_{SSRW}		8			ns	
SR/$\overline{W}$ hold time	t_{HSRW}		3			ns	

Read Timing