54AC/74AC723 • 54ACT/74ACT723

64 x 9 First-In, First-Out Memory

Description

The 'AC/'ACT723 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out (typical) data rate make it ideal for high-speed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with almost negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset ($\overline{MR}$) and Output Enable ($\overline{OE}$) for initializing the internal registers and allowing the data outputs to be 3-stated. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations.

The FIFO can be expanded to increase the depth by cascading or provide different word lengths by tying off unused data inputs.

- **64-Words by 9-Bit Dual Port RAM Organization**
- **85 MHz Shift-In, 60 MHz Shift-Out Data Rate with Flags, Typical**
- **Expandable in Word Depth and Width Dimensions**
- **'ACT723 has TTL-Compatible Inputs**
- **Asychronous or Synchronous Operation**
- **Asynchronous Master Reset**
- **Outputs Sink/Source 8 mA**
- **3-State Outputs**
- **Full ESD Protection**
- **Output and Input Pins Directly in Line for Easy Board Layout**
- **TRW 1030 Work-Alike* Operation**

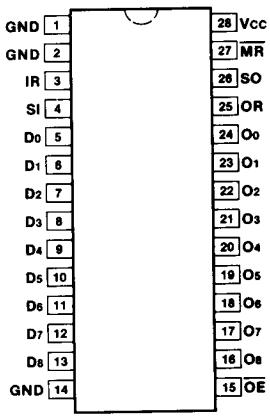
Applications

- **High-Speed Disk or Tape Controllers**
- **A/D Output Buffers**
- **High-Speed Graphics Pixel Buffer**
- **Video Time Base Correction**
- **Digital Filtering**

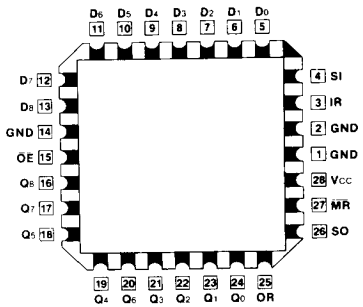
Ordering Code: See Section 6

*The TRW1030 has data setup and hold times with respect to the rising edge of SI. The 'AC/'ACT723 has data setup and hold times with respect to the falling edge of SI.

Connection Diagrams

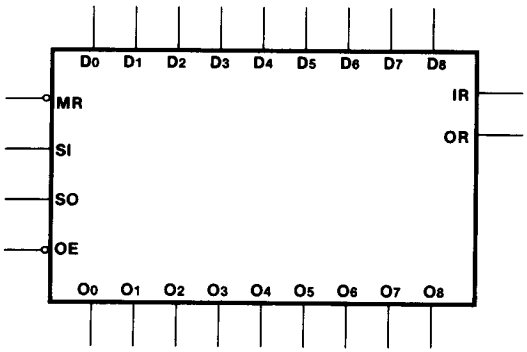


Pin Assignment for DIP and Flatpak



Pin Assignment for LCC and PCC

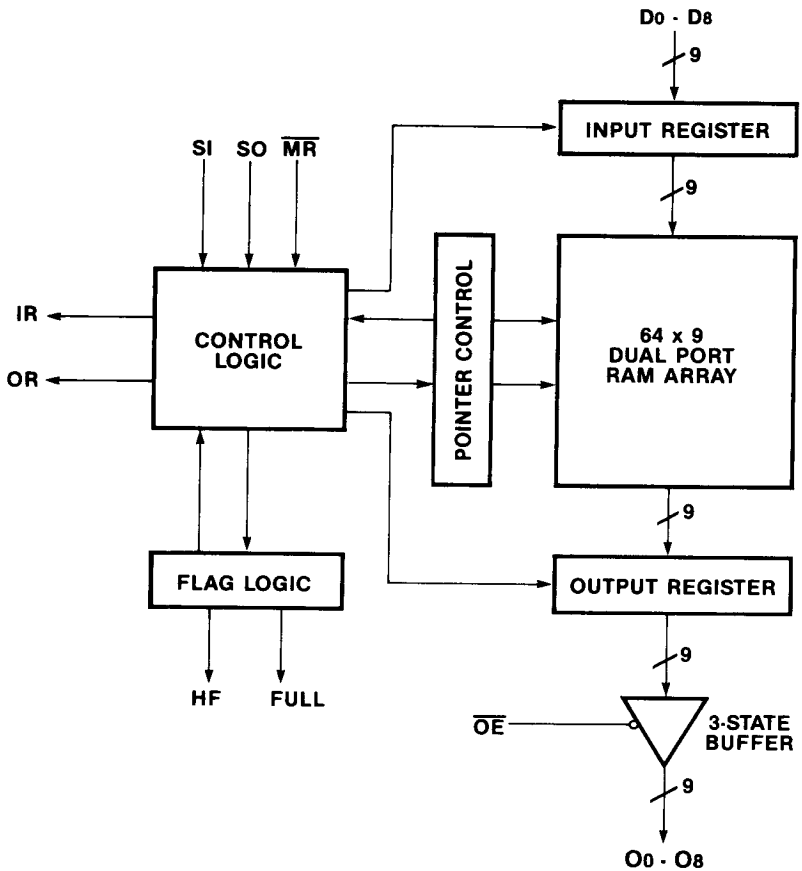
Logic Symbol



Pin Names

D_0 - D_8	Data Inputs
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable Input
SI	Shift-In
SO	Shift-Out
IR	Input Ready
OR	Output Ready
O_0 - O_8	Data Outputs

Block Diagram



Functional Description

Inputs

Data Inputs (D_0 - D_8)
Data inputs for 9-bit wide data are TTL-compatible ('ACT723). Word width can be reduced by tying unused inputs to ground and leaving the corresponding outputs open.

Reset ($\overline{MR}$)
Reset is accomplished by pulsing the $\overline{MR}$ input LOW. During normal operation $\overline{MR}$ is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, and OR goes LOW. During reset, both internal read and write pointers are set to the first location in the array.

Shift-In (SI)
Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into and internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation.

When the FIFO is empty and $\overline{OE}$ is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

Shift-Out (SO)
Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay t_D. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

Output Enable ($\overline{OE}$)
$\overline{OE}$ LOW enables the 3-state output buffers. When $\overline{OE}$ is HIGH, the outputs are in a 3-state mode.

Outputs

Data Outputs (O_0 - O_8)
Data outputs are enabled when $\overline{OE}$ is LOW and in the 3-state condition when $\overline{OE}$ is HIGH.

Input Ready (IR)
IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

Output Ready (OR)
OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or when there is no valid data and goes HIGH after the falling edge of the first shift-in.

Reset Truth Table

Inputs			Outputs		
$\overline{MR}$	SI	SO	IR	OR	O_0 - O_8
1	X	X	X	X	X
0	X	X	1	0	0

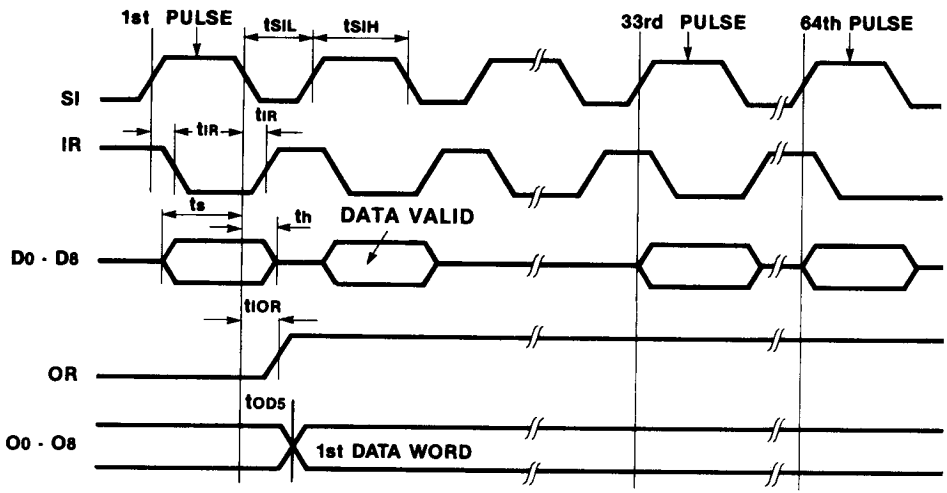
Modes of Operation

Mode 1: Shift-In Sequence for FIFO Empty to Full

Sequence of Operation

1. Input ready is initially HIGH; the FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data. Assume Shift-Out is LOW for this mode.
2. Shift-In is set HIGH, and data is loaded into the FIFO. Data has to be settled setup time t_s before the falling edge of SI and held hold time t_h after.
3. Input Ready (IR) goes LOW propagation delay t_{IR} after SI goes HIGH; input stage is busy.
4. Shift-In is set LOW; IR goes HIGH indicating the FIFO is ready for additional data. Data just shifted in arrives at output propagation delay t_{OD5} after SI falls. OR goes HIGH propagation delay t_{IOR} after SI goes LOW, indicating the FIFO has valid data on its outputs.
5. The process is repeated through the 64th data word. IR goes LOW on the falling edge of the 64th SI and remains LOW indicating a full FIFO. Any further shift-ins are disabled.

Figure 1: Modes of Operation
Mode 1



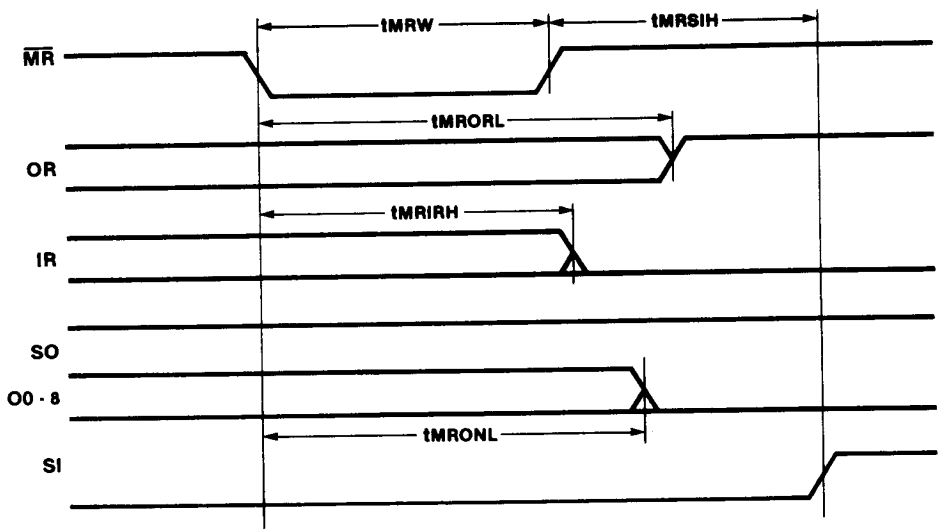
Note: SO and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH.

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready can be in any state before the reset sequence with Master Reset HIGH ($\overline{MR}$).
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recovery time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In must be delayed a minimum of recovery time t_{MRSIH}.

Figure 2: Modes of Operation
Mode 2

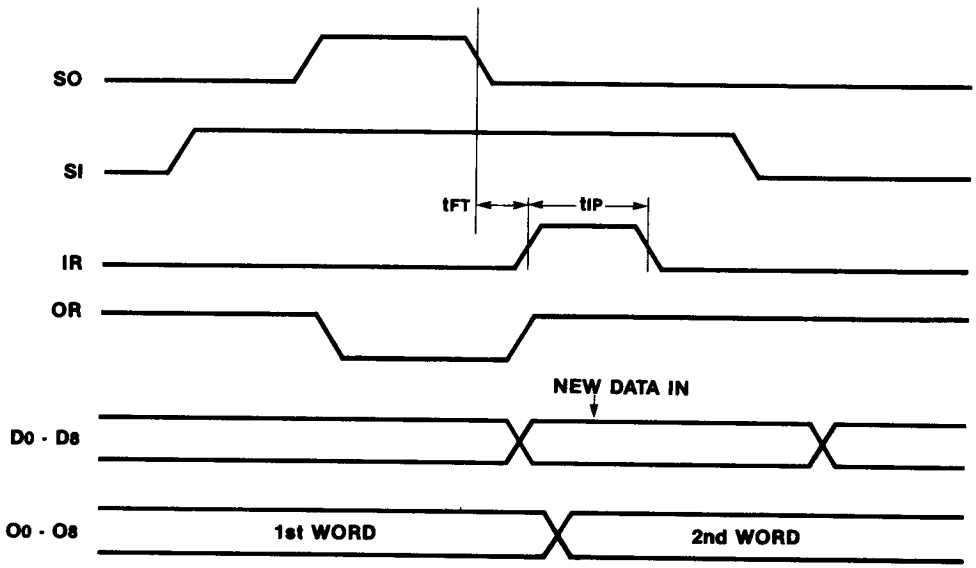


Mode 3: With FIFO Full, Shift-In is Held HIGH in Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. IR and SO are LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after OR propagation delay t_D.
3. Input Ready goes HIGH fall-through time t_{FT} after the falling edge of SO.
4. IR returns LOW pulse width t_{IP} after rising and shifting fresh data in.
5. Shift-In is brought LOW to complete the shift process and maintain normal operation.

Figure 3: Modes of Operation
Mode 3



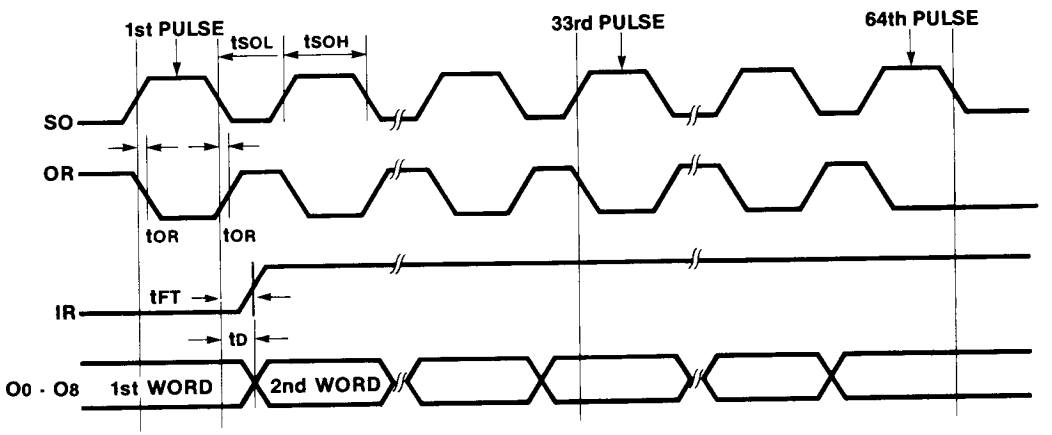
Note: $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW.

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW propagation delay t_{OR} after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output propagation delay t_D after SO falls; OR goes HIGH propagation delay t_{OR} after SO falls, IR rises fall-through time t_{FT} after SO falls.
4. Repeat process through the 64th SO pulse. OR stays LOW after 64th SO indicating an empty FIFO. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.

Figure 4: Modes of Operation
Mode 4



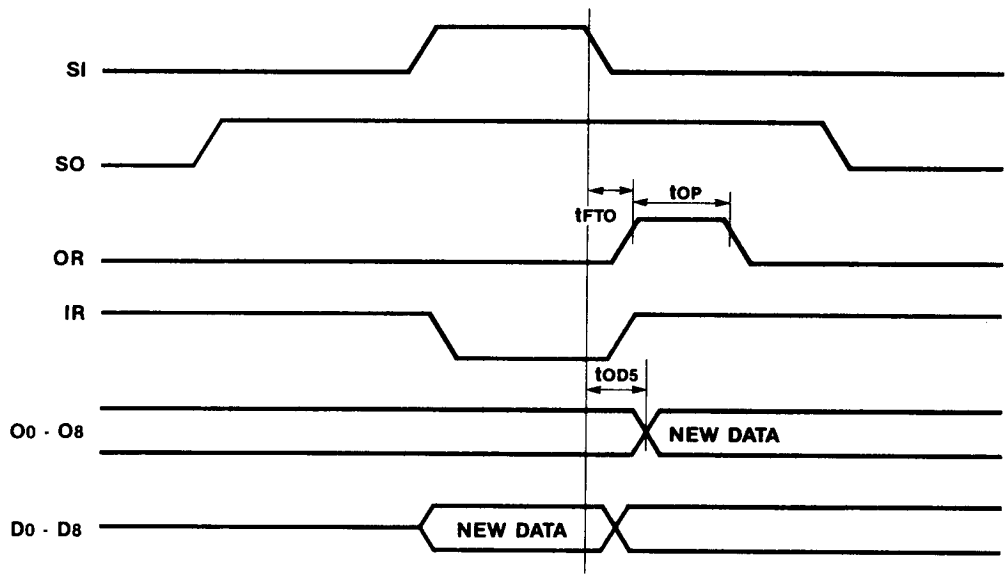
Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0 - D_8 are immaterial.

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH. IR is HIGH; OR is LOW.
2. Shift-In pulse HIGH loads data into the FIFO and IR falls.
3. OR rises fall through time t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output propagation delay t_{OD5} after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.

Figure 5: Modes of Operation
Mode 5



Note: $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$ — data output transition, valid data arrives at output stage t_{DOF} after OR is HIGH.

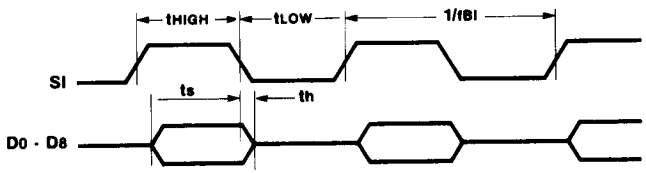
Mode 6: Shift-In Operation in High-Speed Burst Mode

Sequence of Operation

1. Shift-In goes HIGH, loading data into the FIFO. IR is ignored.
2. Shift-in goes LOW pulse width t_{HIGH} time later; loading is complete.
3. Shift-In rises again for the second load pulse width t_{LOW} after the falling edge.

The burst-in rate is determined by SI HIGH and LOW. Data is shifted-in ignoring the IR flag. Any SI after the FIFO is filled up will be ignored.

Figure 6: Modes of Operation
Mode 6



Note: $\overline{MR}$ is HIGH; $t_{HIGH} > t_{SIH}$; $t_{LOW} > t_{SIL}$; $t_{HIGH} + t_{LOW} > 1/f_{SI}$.

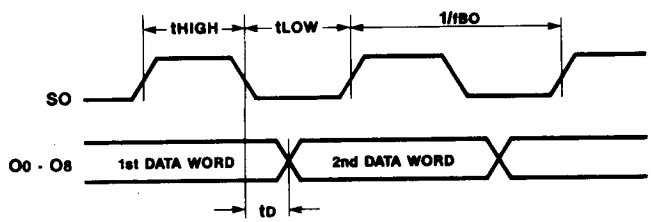
Mode 7: Shift-Out Operation in High-Speed Burst Mode

Sequence of Operations

1. Shift-Out is LOW; valid data is available on output with OR ignored.
2. Shift-Out rises; data out is latched.
3. Shift-Out falls pulse width time t_{HIGH} after rise Shift-Out is complete; new data is loaded onto output.

The burst-out rate is determined by SO HIGH and LOW. The OR flag is ignored.

Figure 7: Modes of Operation
Mode 7



Note: $\overline{OE}$ is LOW; $\overline{MR}$ is HIGH; $t_{HIGH} > t_{SOH}$; $t_{LOW} > t_{SOL}$; $t_{HIGH} + t_{LOW} > 1/f_{SO}$.

FIFO Expansion

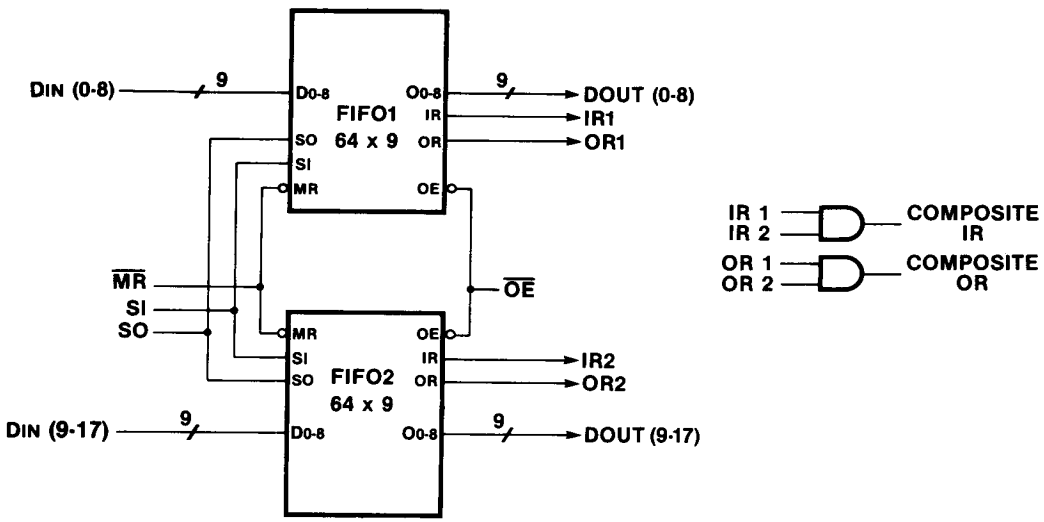
Word Width Expansion
Word width can be increased by connecting the corresponding input control signals of multiple devices. Flags can be monitored on any one device (Figure 8), or composite flag signals can be achieved by ANDing the corresponding flags.

Depth Expansion
Depth expansion can be achieved by connecting as shown in Figure 9. No external circuitry is required for handshaking, which is achieved by the internal FIFO signals IR and OR.

When n FIFOs are cascaded to attain a 64n word FIFO, the SI signal is connected to the first FIFO and the SO signal to the nth FIFO. The IR and OR signals are monitored from the first and last FIFOs respectively. The IR signal from each FIFO is connected to its preceding SO signal: IR(n)→SO(n-1); IR(n-1)→SO(n-2) . . . IR(2)→SO(1). The OR signal from each FIFO is connected to its succeeding SI signal: i.e., OR(1)→SI(2); OR(2)→SI(3) . . . OR(n-1)→SI(n). Handshaking signals are shown in Figure 10.

FIFO 1 operates in Mode 5 during SI until FIFO2 is filled. FIFO2 operates in Mode 3 during SO until FIFO1 is empty. Data from FIFO1 is written into FIFO2 after a word is read from FIFO2. To achieve this, the $\overline{OE}$ pin is grounded for FIFO1. In general, for n FIFOs, all $\overline{OE}$ pins but the nth FIFO's $\overline{OE}$ pin are enabled. 3-state control of the outputs can then be achieved by controlling the nth FIFO's $\overline{OE}$ pin.

Figure 8: Word Width Expansion — 64 x 18 FIFO



Note: Monitor flags from any one FIFO or AND the corresponding flags to obtain a composite signal.

Figure 9: Depth Expansion Mode — 128 x 9 FIFO

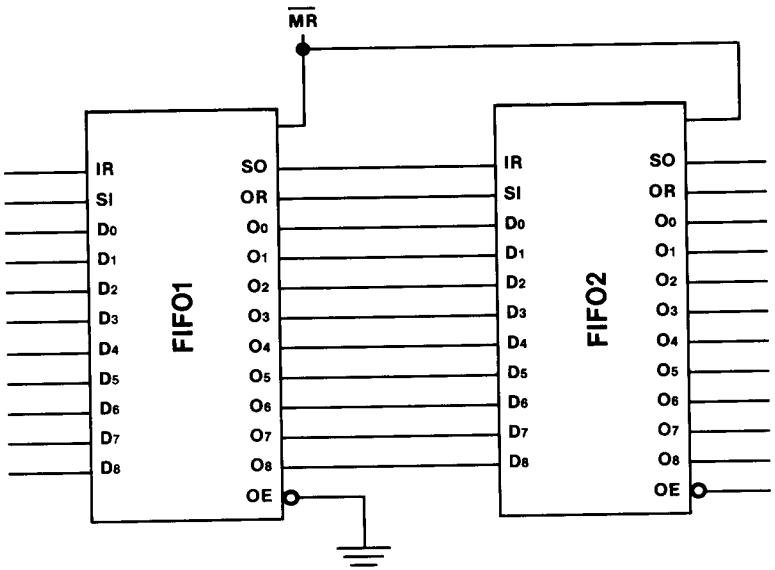
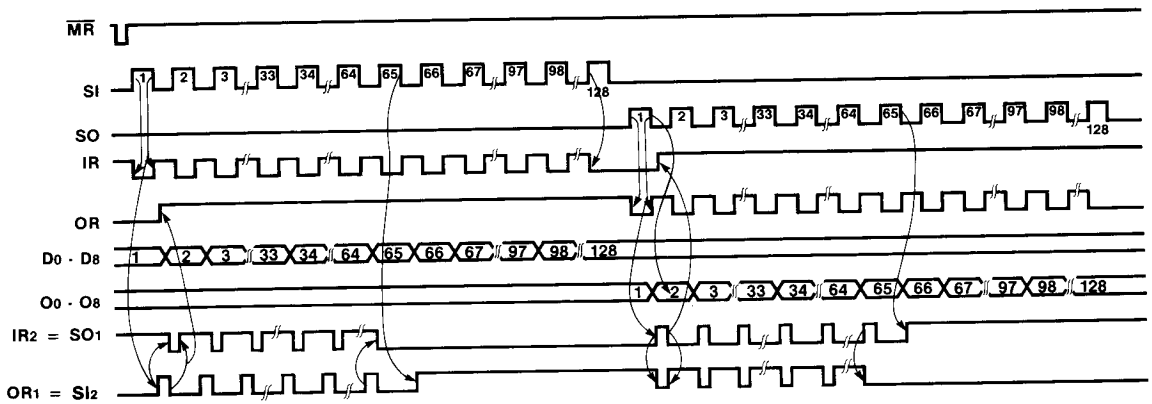


Figure 10: Handshaking for Depth Expansion Mode — 128 x 9 FIFO



Note: The numbers for SI and SO indicate the pulse numbers. The numbers for data in and data out indicate data words: 1 is the first data word, 2 is the second data word, etc.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I_{IN}	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
I_{CCQ}	Supply Current, Quiescent	50.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
I_{CCD}	Supply Current, 20 MHz Loaded	325		150	150	mA	V_{CC} = Max, f = 20 MHz Test Load: See Note 1
V_{OH}	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = −8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = −8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current			−32	−32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pF, 500 ohm to Ground

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay, t_{IR} SI to IR	3.3 5.0		8.5 5.5						ns	1
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	3.3 5.0		13.0 9.5						ns	1
t_{PHL}, t_{PLH}	Propagation Delay, t_{D} SO to Data Out	3.3 5.0		23.0 17.0						ns	4
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	3.3 5.0		9.5 7.0						ns	4
t_{PHL}, t_{PLH}	Propagation Delay, t_{ODS} SI to New Data Out	3.3 5.0		22.0 16.0						ns	1, 5
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	3.3 5.0		16.0 11.5						ns	5
t_{PLH}	Fall-Through Time, t_{FT} SO to IR, HIGH	3.3 5.0		18.5 13.5						ns	3
t_{PZL}	Output Enable $\overline{OE}$ to On	3.3 5.0		7.5 5.5						ns	3-8
t_{PLZ}	Output Disable $\overline{OE}$ to On	3.3 5.0		6.0 4.5						ns	3-8
t_{PZH}	Output Enable $\overline{OE}$ to On	3.3 5.0		9.0 6.5						ns	3-7
t_{PHZ}	Output Disable $\overline{OE}$ to On	3.3 5.0		9.0 6.5						ns	3-7
t_{rec}	Recovery Time, t_{MRIRH} $\overline{MR}$ to IR	3.3 5.0		9.5 7.0						ns	2
t_{rec}	Recovery Time, t_{MRORL} $\overline{MR}$ to OR	3.3 5.0		20.0 15.0						ns	2
t_{rec}	Recovery Time, t_{MRONL} $\overline{MR}$ to On, LOW	3.3 5.0		11.0 8.0						ns	2
t_w	IR Pulse Width, t_{IP}	3.3 5.0		38.0 28.0						ns	3
t_w	OR Pulse Width, t_{OP}	3.3 5.0		23.0 17.0						ns	5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{SI}	Maximum SI Clock Frequency	3.3 5.0		60 85						MHz	1
f_{SO}	Maximum SO Clock Frequency	3.3 5.0		50 60						MHz	4
f_{BO}	Maximum Clock Frequency, SO Burst Mode	3.3 5.0		55 65						MHz	7
f_{BI}	Maximum Burst In Clock	3.3 5.0		60 85						MHz	6

*Voltage Range 3.3 is 3.3 V. ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Typ	Guaranteed Minimum							
t_w	SI Pulse Width, t_{SIH} HIGH	3.3 5.0	4.0 1.5							ns	1, 6
t_w	SI Pulse Width, t_{SIL} LOW	3.3 5.0	4.0 1.5							ns	1, 6
t_s	Setup Time, HIGH or LOW, D_n to SI	3.3 5.0	2.0 1.0							ns	1
t_h	Hold Time, HIGH or LOW, D_n to SI	3.3 5.0	3.0 1.5							ns	1
t_w	$\overline{MR}$ Pulse Width, t_{MRW}	3.3 5.0	17.0 13.0							ns	2
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	3.3 5.0	7.0 4.0							ns	2
t_w	SO Pulse Width, t_{SOH} HIGH	3.3 5.0	4.5 2.0							ns	4, 7
t_w	SO Pulse Width, t_{SOL} LOW	3.3 5.0	12.5 9.0							ns	4, 7

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing bottominformation please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PLH}	Propagation Delay, t_{IR} SI to IR	5.0		6.5						ns	1
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	5.0		10.5						ns	1
t_{PHL}, t_{PLH}	Propagation Delay, t_D SO to Data Out	5.0		18.5						ns	4
t_{PHL}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	5.0		7.0						ns	4
t_{PHL}, t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	5.0		19.0						ns	1, 5
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	5.0		13.5						ns	5
t_{PLH}	Fall-Through Time, t_{FT} SO to IR, HIGH	5.0		15.0						ns	3
t_{PZL}	Output Enable $\overline{OE}$ to O_n	5.0		6.5						ns	3-8
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	5.0		5.0						ns	3-8
t_{PZH}	Output Enable $\overline{OE}$ to O_n	5.0		6.5						ns	3-7
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	5.0		6.5						ns	3-7
t_{rec}	Recovery Time, t_{MRIRH} $\overline{MR}$ to IR	5.0		8.5						ns	2
t_{rec}	Recovery Time, t_{MRORL} $\overline{MR}$ to OR	5.0		16.5						ns	2
t_{rec}	Recovery Time, t_{MRONL} $\overline{MR}$ to O_n, LOW	5.0		9.0						ns	2
t_w	IR Pulse Width, t_{IP}	5.0		28.0						ns	3
t_w	OR Pulse Width, t_{OP}	5.0		17.0						ns	5
f_{SI}	Maximum SI Clock Frequency	5.0		85						MHz	1
f_{SO}	Maximum SO Clock Frequency	5.0		60						MHz	4

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representatve.

AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{BO}	Maximum Clock Frequency, SO Burst Mode	5.0		65						MHz	7
f_{BI}	Maximum Burst In Clock	5.0		85						MHz	6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_w	SI Pulse Width, t_{SIH} HIGH	5.0	1.5				ns	1, 6
t_w	SI Pulse Width, t_{SIL} LOW	5.0	1.5				ns	1, 6
t_s	Setup Time, HIGH or LOW, D_n to SI	5.0	1.0				ns	1
t_h	Hold Time, HIGH or LOW, D_n to SI	5.0	1.5				ns	1
t_w	$\overline{MR}$ Pulse Width, t_{MRW}	5.0	13.0				ns	2
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	5.0	4.5				ns	2
t_w	SO Pulse Width, t_{SOH} HIGH	5.0	2.0				ns	4, 7
t_w	SO Pulse Width, t_{SOL} LOW	5.0	9.0				ns	4, 7

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V