STEL-1172B
Data Sheet

STEL-1172B (50 MHz)

32-Bit Resolution CMOS Numerically Controlled Oscillator

intel

FEATURES

- 32 BIT FREQUENCY RESOLUTION
- PARALLEL SINE AND COSINE OUTPUTS
- 50 MHz CLOCK FREQUENCY (0° TO 70°C)
- 8-BIT INTERNAL SINE AND COSINE AMPLITUDE RESOLUTION
- 10-BIT INTERNAL SINE AND COSINE PHASE RESOLUTION
- 12-BIT PHASE OUTPUT AVAILABLE
- MILITARY AND COMMERCIAL TEMPERATURE RANGES AVAILABLE
- MICROPROCESSOR BUS COMPATIBLE
- PIN COMPATIBLE WITH ST-1172A
- CASCADABLE FOR ULTRA HIGH RESOLUTION
- LOW POWER CMOS

APPLICATIONS

- FREQUENCY SYNTHESIZERS
- HI-SPEED FREQUENCY HOPPED SOURCES
- SINGLE SIDEBAND CONVERTERS
- BASEBAND RECEIVERS
- DIGITAL SIGNAL PROCESSORS

CIRCUIT DESCRIPTION

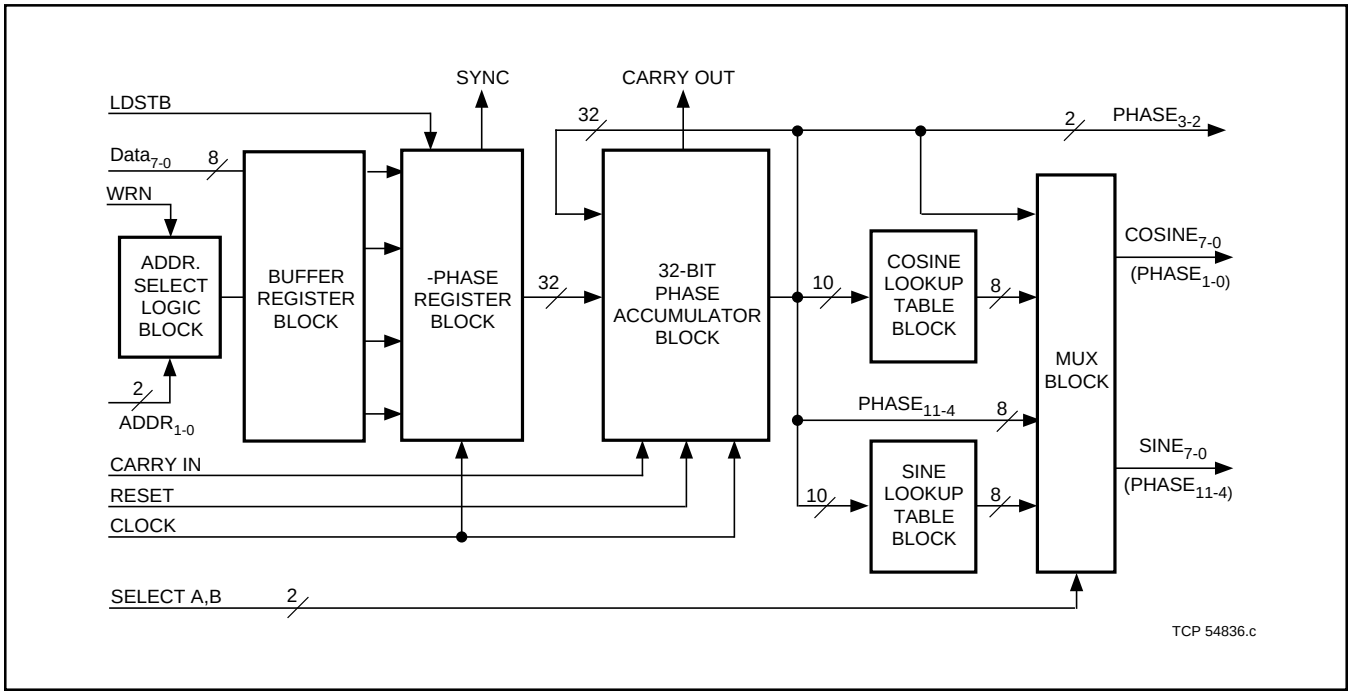
The STEL-1172B Numerically Controlled Oscillator (NCO) generates digital sine and cosine signals of very precise frequency to be used directly in digital signal processing applications or in conjunction with a D/A converter in analog frequency generation applications. The device, implemented with low power CMOS, can operate with clock frequencies as high as 50 MHz. (40 MHz over the military temperature range, –55° C to +125° C). The NCO is designed to interface with an eight bit microprocessor bus.

The NCO maintains a record of phase which is accurate to 32 bits of resolution. At each clock cycle, the number stored in the 32 bit Δ-phase register is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine and cosine functions. The number in the Δ-phase register represents the change of phase for each cycle of the clock. This number is directly related to the output frequency by the following:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{32}}$$

where: f_o is the frequency of the output signal
and: f_c is the clock frequency.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

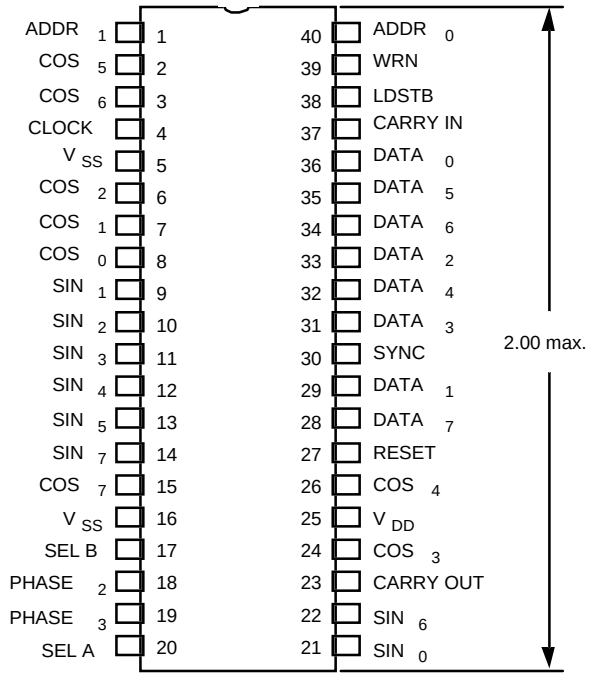
The sine and cosine signals are generated from the 10 most significant bits of the phase accumulator. The frequency of the NCO is determined by the number stored in the Δ−phase register which may be programmed by an eight-bit microprocessor.

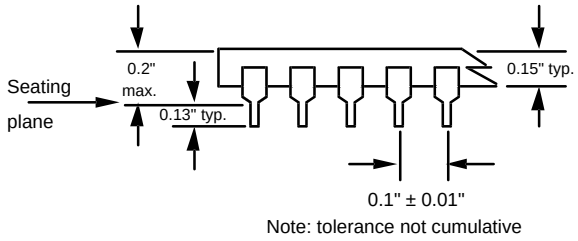
The STEL-1172B NCO generates digitized sampled sine and cosine signals where the sampling function is the clock. If the output frequency is very low with respect to the clock ($<f_c/1024$), then the NCO output will sequence through each of the 1024 states of the sine function stored in the lookup table. As the output frequency is increased with respect to the clock, the sine function appears more discontinuous as there are fewer samples in each cycle. At the Nyquist limit, when the output frequency is exactly half the clock, the output waveform reduces to a square wave. The practical upper limit of the NCO output frequency is about 40% of the clock frequency because spurious components created by sampling, which are at a frequency greater than half the clock frequency, become difficult to remove by filtering.

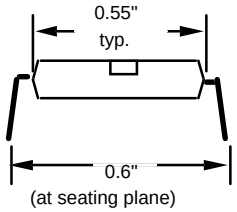
The phase noise of the NCO output signal may be determined by knowing the phase noise of the clock signal input and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

The NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCO represent 34 clock cycles. This effectively limits the minimum possible frequency switching period of the NCO. After new frequency data is entered the load command is given. After the 34 cycle pipeline delay the output will instantaneously switch frequency while maintaining phase coherence. After this the next new frequency may be entered. If a 50 MHz clock were utilized the NCO could be continuously switched between programmed frequencies with a minimum practical average switching time of about 1 μsec.

PIN CONFIGURATION







Package: 40 pin plastic DIP
Thermal coefficient, θjc = 15°/W
Note: pin spacing for Ceramic DIP is the same

FUNCTION BLOCK DESCRIPTION

ADDRESS SELECT LOGIC BLOCK

This block controls the writing of data into the device via the **$DATA_{7-0}$** inputs. The data is written into the device on the falling edge of the **WRN** input, and the register into which the data is written is selected by the **$ADDR_{1-0}$** inputs.

BUFFER REGISTER BLOCK

The Buffer Register is used to temporarily store the Δ-Phase data written into the device. This allows the data to be written asynchronously as four bytes per 32-bit Δ-Phase word. The data is transferred from this register into the Δ-Phase Register after a rising edge on the **LDSTB** input.

Δ-PHASE REGISTER BLOCK

This block controls the updating of the Δ-Phase word used in the Accumulator. The frequency data from the Mux Block is loaded into this block after a rising edge on the **LDSTB** input. The **SYNC** output, which indicates the instant of frequency change at the output at the end of the pipeline delay, is generated in this block.

PHASE ACCUMULATOR BLOCK

This block forms the core of the NCO function. It is a high-speed, pipelined, 32-bit parallel accumulator, generating a new sum in every clock cycle. A carry input (the **CARRY IN** input) allows the resolution of the accumulator to be expanded by means of an auxiliary NCO or phase accumulator. The overflow signal is discarded (and is available at the **CARRY OUT** pin), since the required output is the modulo (2^{32}) sum only. This represents the modulo (2π) phase angle.

SINE AND COSINE LOOKUP TABLE BLOCKS

These blocks are the sine and cosine memories. The 10 most significant bits from the Phase Accumulator are used to address this memory to generate the 8-bit **SIN_{7-0}** and **COS_{7-0}** outputs.

MUX BLOCK

The twelve most significant bits from the Phase Accumulator Block are available at the output via the MUX Blocks as alternatives to the **SIN_{7-0}** and **COS_{7-0}** outputs. The MUX Blocks are controlled by the **SELECT A** and **SELECT B** inputs.

INPUT SIGNALS

RESET

The **RESET** input is synchronous with the **CLOCK** input. When **RESET** goes to a logic high level all registers except the 32 bit input buffer and Δ-Phase register are cleared within 20 nsecs. of the next rising edge of the **CLOCK**. The output data and Phase Accumulator are cleared to zero. After the **RESET** returns to a logic zero the chip requires 37 rising clock edges to resume normal operation. For the first two of these cycles the output data will be 00_H and then 80_H, respectively. For the remaining 35 clock cycles the **SIN** and **COS** outputs remain at the value corresponding to zero phase, i.e. 129, or 81_H. Normal operation will then commence, starting at zero phase

CLOCK

All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 50 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 8 nanoseconds. At each rising edge of the **CLOCK** signal the contents of the phase accumulator are added to the number stored in the Δ-Phase register, and the result is placed in the Phase Accumulator.

WRN

The information on the 8-bit data bus is transferred to the buffer register selected by **$ADDR_1$** and **$ADDR_0$** on the falling edge of the **WRN** input.

LDSTB

On the rising edge of the clock following the rising edge of the **LDSTB** input the information in the four buffer registers is transferred to the Δ-Phase Register. The frequency at the NCO output will change 34 clock cycles after the **LDSTB** command due to pipelining delays.

$ADDR_1$ and $ADDR_0$

The **$ADDR_1$** and **$ADDR_0$** signals control the use of the **$DATA_{7-0}$** bus according to the table:

$ADDR_0$	$ADDR_1$	Δ-Phase Register Field
1	1	Bits 0 (LSB) through 7
0	1	Bits 8 through 15
1	0	Bits 16 through 23
0	0	Bits 24 through 31 (MSB)

The least significant bit of the input data bus always maps into the least significant bit of the Δ-Phase Register field.

$DATA_7$ through $DATA_0$

The eight bit $DATA_{7-0}$ bus is used to program the 32 bit Δ-Phase Register. $DATA_0$ is the least significant bit of the bus. To change all 32 bits of the Δ-Phase Register, the $DATA_{7-0}$ bus must be sequentially used four times in conjunction with the **WRN**, $ADDR_0$ and $ADDR_1$ signals.

SELECT A

When **SELECT A** is a logic 0, the sine function appears on the SIN_{7-0} bus. When **SELECT A** is a logic 1, the eight most significant bits of the phase accumulator appear on this bus. The twelve most significant bits of the 32 bit Phase Accumulator are available externally. The eight most significant bits appear on the **SIN** bus and are labeled $PHASE_{11}$ (MSB) through $PHASE_4$.

Output Pin	Pin Name	Function: SELECT A =0	Function: SELECT A =1
14	SIN_7	SIN_7 (MSB)	$PHASE_4$
22	SIN_6	SIN_6	$PHASE_5$
13	SIN_5	SIN_5	$PHASE_6$
12	SIN_4	SIN_4	$PHASE_7$
11	SIN_3	SIN_3	$PHASE_8$
10	SIN_2	SIN_2	$PHASE_9$
9	SIN_1	SIN_1	$PHASE_{10}$
21	SIN_0	SIN_0 (LSB)	$PHASE_{11}$ (MSB)

SELECT B

When **SELECT B** is a logic 1 the two most significant bits of the cosine function appear on output pins 3 and 15. When Select B is a logic 0 pin 15 provides the signal $PHASE_1$ and pin 3 provides the signal $PHASE_0$. $PHASE_1$ and $PHASE_0$ are the eleventh and twelfth most significant bits of the phase accumulator, with $PHASE_0$ being the least significant accessible bit.

CARRY IN

Normal operation of the NCO requires that the **CARRY IN** be set at a logic 0. When **CARRY IN** is a logic 1 the effective value of the Δ-phase register is increased by one. If two NCOs are cascaded together to obtain 64 bits of frequency resolution the **CARRY OUT** of the lower order NCO is connected to the **CARRY IN** of the higher order NCO.

OUTPUT SIGNALS

CARRY OUT

Each time the contents of the phase accumulator exceeds the maximum value that can be represented by a 32 bit number the **CARRY OUT** signal goes high for one clock cycle. When two NCOs are cascaded to obtain 64 bit frequency resolution the **CARRY OUT** of the lower order NCO must be connected to the **CARRY IN** of the higher order NCO.

SIN_{7-0} and COS_{7-0}

The sine and cosine functions which are presented on the SIN_{7-0} and COS_{7-0} buses are derived from the 10 most significant bits of the phase accumulator. The 8-bit sine and cosine functions are presented in offset binary format with a minimum value of 00_H and a maximum value of FF_H. SIN_7/COS_7 are the MSBs. When the phase accumulator is zero, the decimal value of the **SIN** output is 81_H. The nominal phase (in degrees) of the sine and cosine outputs may be determined by multiplying the decimal equivalent of the ten most significant bits of the phase accumulator by (360/1024) and adding (360/2048). The average amplitude over a full cycle is 127.5 decimal. See the description of **SELECT A/B** and **PHASE** for the alternate use of the SIN_{7-0} and COS_{7-0} buses.

$PHASE_{11-0}$

The twelve most significant bits of the 32 bit phase accumulator are available as outputs of the NCO. $PHASE_{11}$ is the most significant bit of the 32 bit phase accumulator. The eight most significant **PHASE** bits are multiplexed on the **SIN** bus (see description of **SELECT A** input). The next two significant bits ($PHASE_2$ and $PHASE_3$) are available continuously on pins 18 and 19 respectively. The two least significant bits ($PHASE_1$ and $PHASE_0$) are multiplexed on the **COS** bus (see description of **SELECT B** input).

SYNC

The normally high **SYNC** output goes low for one clock cycle 35 rising clock edges after a **RESET** and 34 rising clock edges after a **LDSTB** command. If two NCOs are cascaded for higher frequency resolution the **SYNC** output of the lower order NCO must be connected to the **LDSTB** input of the higher order NCO to insure a phase continuous frequency transition.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

***Warning:** Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}.*

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125 –65 to +150	°C (Plastic package) °C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD} + 0.3	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units	
V_{DD}	Supply Voltage	+5 ± 5% +5 ± 10%	Volts Volts	(Commercial) (Military)
T_a	Operating Temperature (Ambient)	0 to +70 –55 to +125	°C °C	(Commercial) (Military)

D.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS} = 0 V, T_a= 0° to 70° C, Commercial

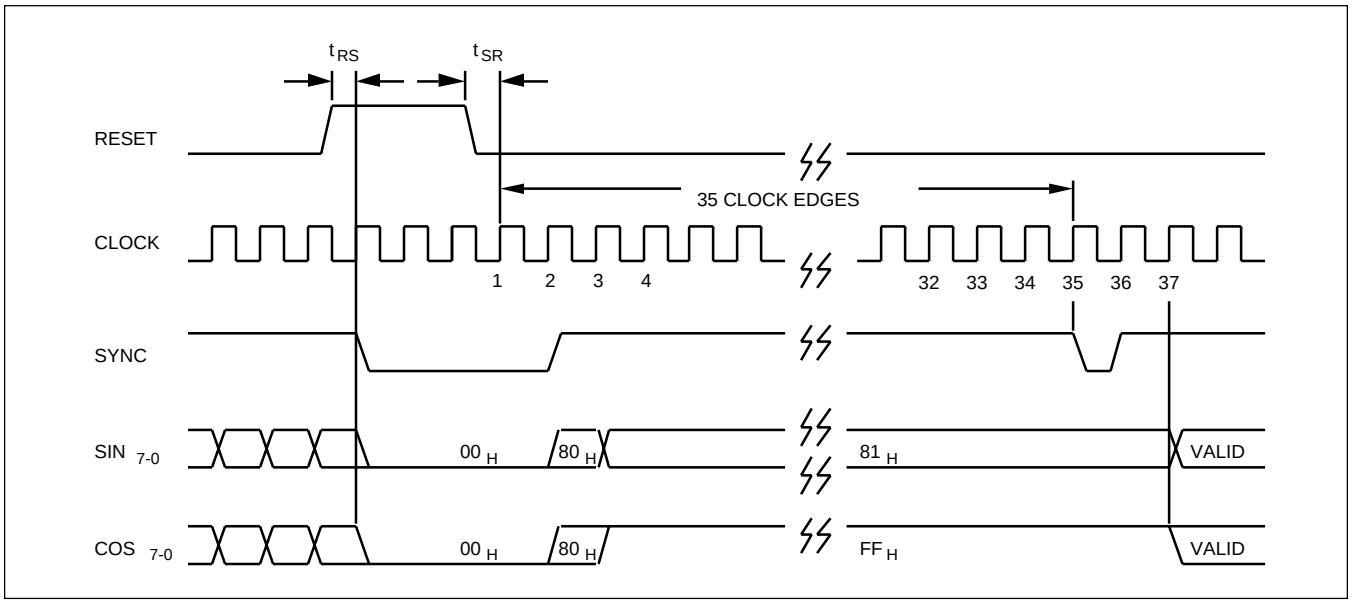
V_{DD}= 5.0 V ±10%, V_{SS} = 0 V, Ta = –55° to 125° C, Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			3.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current			10	µA	$V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current	–15	–45	–130	µA	$V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –4.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

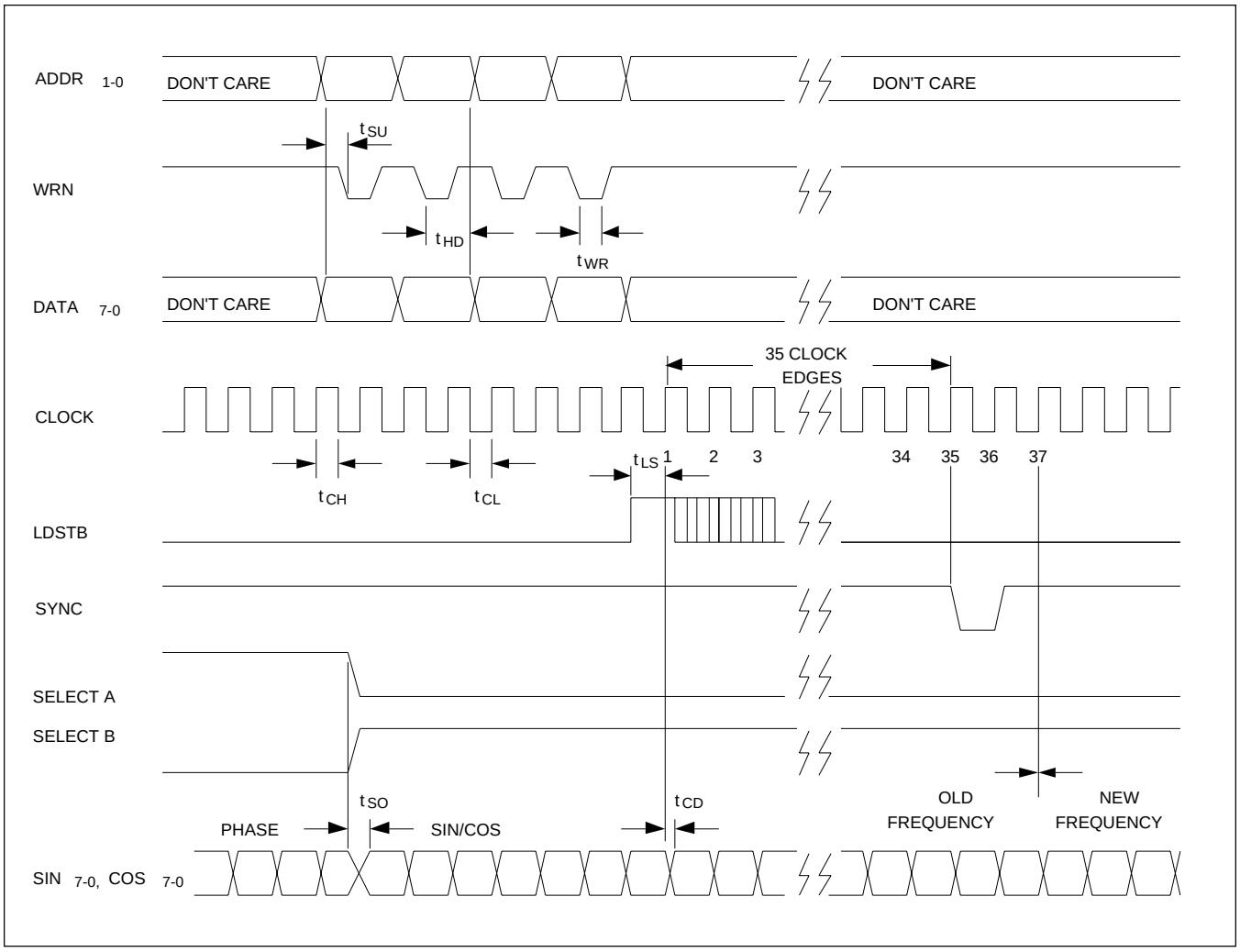
A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±5%, VSS = 0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, VSS = 0 V, Ta = –55° to 125° C, Military)

		(Commercial)		(Military)			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Conditions**
t_{RS}	**RESET** pulse width	30		35		nsec.	
t_{SR}	**RESET** to **CLOCK** Setup	10		10		nsec.	
t_{SU}	**DATA** or **ADDR** to **WRN** Setup, and **LDSTB** to **CLOCK** Setup	5		6		nsec.	
t_{HD}	**DATA** or **ADDR** to **WRN** Hold, and **LDSTB** to **CLOCK** Hold	5		6		nsec.	
t_{CH}	**CLOCK** high	8		10		nsec.	f_{CLK} = max.
t_{CL}	**CLOCK** low	8		10		nsec.	f_{CLK} = max.
t_W	**WRN** or **FRLD** pulse width	20		25		nsec.	
t_{CD}	**CLOCK** to output delay	5	10	3	13	nsec.	Load = 15 pF
t_{SD}	**SEL A/B** to **SIN/COS** delay	20			25	nsec.	Load = 15 pF

NCO RESET SEQUENCE

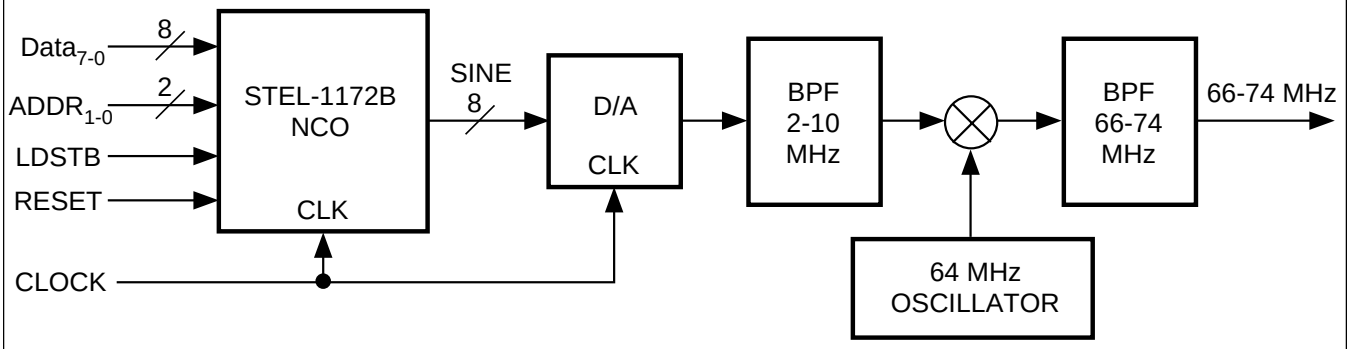


NCO FREQUENCY CHANGE



TYPICAL APPLICATION

HIGH-SPEED HOPPING 66-74 MHz SYNTHESIZER



If the STEL-1172B is combined with a high-speed 8-bit video DAC, signals with spectral purity of better than –55 dBc can be generated up to 10 MHz. In this way a signal can be generated in the 66 to 74 MHz band after filtering and upconversion. Because of the phase continuous frequency switching characteristics of the STEL-1172B this architecture is suitable for Frequency Hopping Spread Spectrum applications.

SPECTRAL PURITY

In many applications the NCO is used with a digital to analog converter (DAC) to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC.

The sine and cosine signals generated by the STEL-1172B have eight bits of amplitude resolution and ten bits of phase resolution which results in spurious levels which are theoretically about -60 dBc. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of the NCO approaches $f_c/2$ the "image" spur at $f_c - f_o$ also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this "image" spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

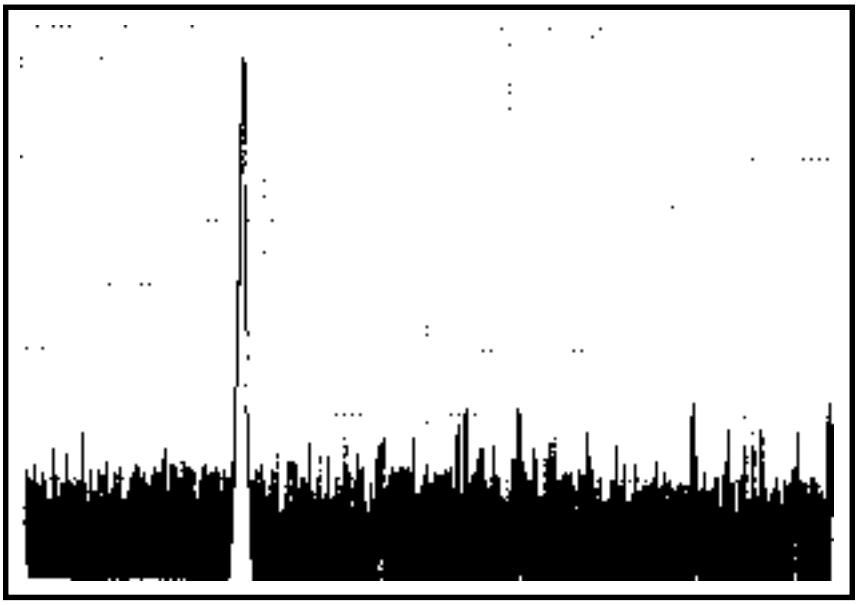
The higher the resolution of the NCO outputs the greater the spectral purity. Each additional bit used in quantizing the phase and amplitude of the sine function (assuming equal resolution for each) provides 6 dB improvement in spectral purity. For this reason, 12 bits of phase information are brought to the STEL-1172B outputs. It is possible to use these signals with an external sine ROM to generate sine waves which have spurious levels as low as -72 dBc.

In some applications the NCO is used with two DACs to generate analog sine and cosine signals to drive a single sideband mixer. If the sine and cosine functions were ideal a typical single sideband mixer would provide 20 to 30 dB of LO and image suppression. This performance can be significantly degraded if an NCO is used to generate these signals near the maximum NCO frequency. It is recommended that care be taken when designing the STEL-1172B into such systems when the output frequency is a significant fraction of the clock frequency.

A spectral plot of the NCO output after conversion with a DAC (AD9703) is shown below. In this case the clock frequency is 50 MHz and the output frequency is programmed to 5.6789 MHz. The maximum spur level observed over the entire useful output frequency range in this case is –55 dBc. Under other conditions the spurious levels may be greater than this due to DAC limitations or clock feedthrough problems relating to grounding on the PC board. At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason the settling time of the DAC should be short in comparison to the clock period . As a general rule the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Output frequency:	5.6789 MHz
Clock frequency:	50.0 MHz
Frequency Span:	0 to 20 MHz
Reference Level:	0 dBm
Resolution Bandwidth:	1 kHz
Video Bandwidth:	3 kHz
Scale:	Log, 10 dB/div



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