

- **Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus**
- **40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators**
- **17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation**
- **Compare Select Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator**
- **Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units**
- **Data Bus With a Bus Holder Feature**
- **192K × 16-Bit Maximum Addressable Memory Space (64K Words Program, 64K Words Data, and 64K Words I/O)**
- **On-Chip ROM with Some Configurable to Program/Data Memory**
- **Dual-Access On-Chip RAM**
- **Single-Instruction Repeat and Block Repeat Operations for Program Code**
- **Block Memory Move Instructions for Better Program and Data Management**
- **Instructions With a 32-Bit Long Word Operand**
- **Instructions With Two- or Three-Operand Reads**
- **Arithmetic Instructions With Parallel Store and Parallel Load**
- **Conditional Store Instructions**
- **Fast Return From Interrupt**
- **On-Chip Peripherals**
 - Software-Programmable Wait-State Generator and Programmable Bank Switching
 - On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source
 - Full-Duplexed Serial Port to Support 8- or 16-Bit Transfers ('C541, 'LC541, 'VC541, 'LC544, 'VC544, 'LC545, 'VC545, 'LC546, and 'VC546 Only)
 - Time-Division Multiplexed (TDM) Serial Port ('C542, 'LC542, 'VC542, 'LC543 and 'VC543 Only)
 - Buffered Serial Port (BSP) ('C542, 'LC542, 'VC542, 'LC543, 'VC543, 'LC545, 'VC545, 'LC546, and 'VC546 Only)
 - 8-Bit Parallel Host Port Interface (HPI) ('C542, 'LC542, 'VC542, 'LC545, and 'VC545 Only)
 - One 16-Bit Timer
 - External-Input/Output (XIO) Off Control to Disable the External Data Bus, Address Bus and Control Signals
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes**
- **CLKOUT Off Control to Disable the CLKOUT**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic**
- **25-ns Single-Cycle Fixed-Point Instruction Execution Time [40 million instructions per second (MIPS)] for 5-V Power Supply ('C541 and 'C542 Only)**
- **20-ns and 25-ns Single-Cycle Fixed-Point Instruction Execution Time (50 MIPS and 40 MIPS) for 3-V Power Supply ('LC54x and 'VC54x)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

SPRS039 – FEBRUARY 1996

description

The TMS320C54x, TMS320LC54x and TMS320VC54x fixed-point, digital signal processor (DSP) families are fabricated with a combination of an advanced modified Harvard architecture which has one program memory bus and three data memory buses. These processors also provide a central arithmetic logic unit (CALU) which has a high-degree of parallelism and application-specific hardware logic, on-chip memory, additional on-chip peripherals. These DSP families also provide a highly specialized instruction set which is the basis of the operational flexibility and speed of these DSPs.

Separate program and data spaces allow simultaneous access to program instructions and data, providing the high degree of parallelism. Two reads and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that all can be performed in a single machine cycle. In addition, the 'C54x, 'LC54x and 'VC54x versions include the control mechanisms to manage interrupts, repeated operations, and function calling.

Table 1 provides an overview of the 'C54x/'LC54x/'VC54x generation of DSPs. The table shows the capacity of on-chip RAM and ROM memories, the peripherals, the execution time of one machine cycle, and the type of package with its total pin count. Use the information in Table 1 to select the best processor for each application.

Table 1. Characteristics of the 'C54x/'LC54x/'VC54x Processors

DSP TYPE	NOMINAL VOLTAGE (V)	ON-CHIP MEMORY		PERIPHERALS			CYCLE TIME (ns)	PACKAGE TYPE
		RAM†	ROM	SERIAL PORT	TIMER	HPI		
TMS320C541	5.0	5K	28K‡	2	1	No	25	100 pin (TQFP)
TMS320LC541	3.3	5K	28K‡	2	1	No	20/25	100 pin (TQFP)
TMS320VC541	3.0	5K	28K‡	2	1	No	20/25	100 pin (TQFP)
TMS320C542	5.0	10K	2K	2§	1	Yes	25	144 pin (TQFP)
TMS320LC542	3.3	10K	2K	2§	1	Yes	20/25	128 pin (TQFP)/144 pin (TQFP)
TMS320VC542	3.0	10K	2K	2§	1	Yes	20/25	128 pin (TQFP)/144 pin (TQFP)
TMS320LC543	3.3	10K	2K	2§	1	No	20/25	100 pin (TQFP)
TMS320VC543	3.0	10K	2K	2§	1	No	20/25	100 pin (TQFP)
TMS320LC544	3.3	4K	24K‡	2	1	No	20/25	80 pin (TQFP)
TMS320VC544	3.0	4K	24K‡	2	1	No	20/25	80 pin (TQFP)
TMS320LC545	3.3	6K	48K¶	2#	1	Yes	20/25	128 pin (TQFP)
TMS320VC545	3.0	6K	48K¶	2#	1	Yes	20/25	128 pin (TQFP)
TMS320LC546	3.3	6K	48K¶	2#	1	No	20/25	100 pin (TQFP)
TMS320VC546	3.0	6K	48K¶	2#	1	No	20/25	100 pin (TQFP)

Legend:

TQFP = Thin Quad Flat Pack

† The dual-access RAM can be configured as data memory or program and data memory.

‡ For 'C541/'LC541/'VC541/'LC544/'VC544, 8K words of ROM can be configured as program memory or program/data memory.

§ TDM and buffered serial ports

¶ For 'LC545/'VC545/'LC546/'VC546, 16K words of ROM can be configured as program memory or program/data memory.

Standard and buffered serial ports

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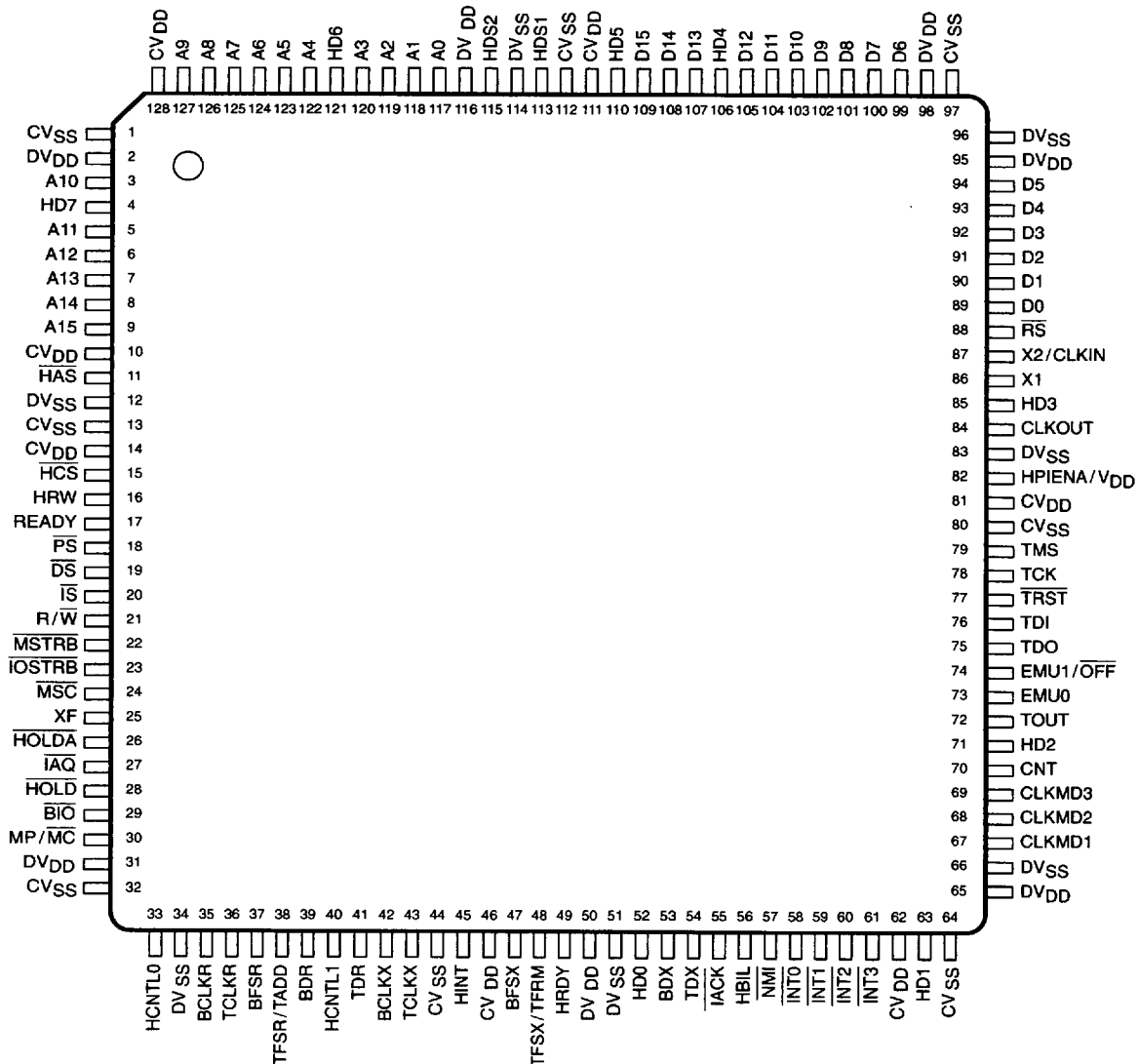
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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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TMS320LC542, TMS320VC542 PBK PACKAGE† (TOP VIEW)



† DVSS and DVDD are power supplies for I/O pins while CVSS and CVDD are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC542PBK/VC542PBK (128-pin) packages.

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC542PBK/'VC542PBK (128-Pin TQFP Package)

PIN NAME	NO	FUNCTION†	DESCRIPTION
CVSS	1	Supply	Ground
DVDD	2	Supply	+VDD
A10	3	O/Z	Parallel port address bus
HD7	4	I/O/Z	Parallel bi-directional data bus (HPI)
A11 – A15	5 – 9	O/Z	Parallel port address bus
CVDD	10	Supply	+VDD
HAS	11	I	Address data strobe (HPI)
DVSS	12	Supply	Ground
CVSS	13	Supply	Ground
CVDD	14	Supply	+VDD
HCS	15	I	Chip select input (HPI)
HRW	16	I	Read/write (HPI)
READY	17	I	External access ready to complete
PS	18	O/Z	Program space select
DS	19	O/Z	Data space select
IS	20	O/Z	I/O select
R/W	21	O/Z	Read/write
MSTRB	22	O/Z	External memory access strobe
IOSTRB	23	O/Z	External I/O access strobe
MSC	24	O/Z	Microstate complete
XF	25	O/Z	External flag
HOLDA	26	O/Z	Hold acknowledge
IAQ	27	O/Z	Instruction acquisition
HOLD	28	I	Request access of local memory
BIO	29	I	Bit I/O pin
MP/MC	30	I	Microprocessor/microcomputer
DVDD	31	Supply	+VDD
CVSS	32	Supply	Ground
HCNTL0	33	I	Control inputs (HPI)
DVSS	34	Supply	Ground
BCLKR	35	I	Receive clock input (BSP)
TCLKR	36	I	Receive clock input (TDM)
BFSR	37	I	Frame synchronization pulse for receive (BSP)
TFSR/TADD	38	I/O	Receive frame synchronization (TDM)
BDR	39	I	Serial data receive input (BSP)
HCNTL1	40	I	Control inputs (HPI)
TDR	41	I	Serial data receive input (TDM)
BCLKX	42	I/O/Z	Serial port 0 transmit clock (BSP)
TCLKX	43	I/O/Z	Serial port 0 transmit clock (TDM)

† I = Input, O = Output, Z = High impedance

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC542PBK/VC542PBK (128-Pin TQFP Package) (Continued)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
CVSS	44	Supply	Ground
HINT	45	O/Z	Interrupt output (HPI)
CVDD	46	Supply	+VDD
BFSX	47	I/O/Z	Frame synchronization pulse for transmit (BSP)
TFSX/TFRM	48	I/O/Z	Transmit frame synchronization (TDM)
HRDY	49	O/Z	Ready output (HPI)
DVDD	50	Supply	+VDD
DVSS	51	Supply	Ground
HD0	52	I/O/Z	Parallel bi-directional data bus (HPI)
BDX	53	O/Z	Serial data transmit output (BSP)
TDX	54	O/Z	Serial data transmit output (TDM)
ACK	55	O/Z	Interrupt acknowledge
HBIL	56	I	Byte identification input (HPI)
NMI	57	I	Nonmaskable interrupt
INT0–INT3	58–61	I	Interrupt 0 through Interrupt 3
CVDD	62	Supply	+VDD
HD1	63	I/O/Z	Parallel bi-directional data bus (HPI)
CVSS	64	Supply	Ground
DVDD	65	Supply	+VDD
DVSS	66	Supply	Ground
CLKMD1	67	I	Clock mode pin 1
CLKMD2	68	I	Clock mode pin 2
CLKMD3	69	I	Clock mode pin 3
CNT	70	I	I/O level select
HD2	71	I/O/Z	Parallel bi-directional data bus (HPI)
TOUT	72	O/Z	Timer output
EMU0	73	I/O/Z	Emulator interrupt 0
EMU1/OFF	74	I/O/Z	Emulator interrupt 1/shutoff
TDO	75	O/Z	Test data output (IEEE standard 1149.1)
TDI	76	I	Test data input (IEEE standard 1149.1)
TRST	77	I	Test reset (IEEE standard 1149.1)
TCK	78	I	Test clock (IEEE standard 1149.1)
TMS	79	I	Test mode select (IEEE standard 1149.1)
CVSS	80	Supply	Ground
CVDD	81	Supply	+VDD
HPIENA/VDD	82	I	HPI module select input
DVSS	83	Supply	Ground
CLKOUT	84	O/Z	Machine clock output

† I = Input, O = Output, Z = High impedance

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC542PBK/'VC542PBK (128-Pin TQFP Package) (Continued)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
HD3	85	I/O/Z	Parallel bi-directional data bus (HPI)
X1	86	O	Oscillator output
X2/CLKIN	87	I	Oscillator/external clock input
\overline{RS}	88	I	Device reset
D0–D5	89–94	I/O/Z	Parallel data port
DVDD	95	Supply	+VDD
DVSS	96	Supply	Ground
CVSS	97	Supply	Ground
DVDD	98	Supply	+VDD
D6–D12	99–105	I/O/Z	Parallel data port
HD4	106	I/O/Z	Parallel bi-directional data bus (HPI)
D13–D15	107–109	I/O/Z	Parallel data port
HD5	110	I/O/Z	Parallel bi-directional data bus (HPI)
CVDD	111	Supply	+VDD
CVSS	112	Supply	Ground
HDS1	113	I	Data strobe input (HPI)
DVSS	114	Supply	Ground
HDS2	115	I	Data strobe input (HPI)
DVDD	116	Supply	+VDD
A0–A3	117–120	O/Z	Parallel port address bus
HD6	121	I/O/Z	Parallel bi-directional data bus (HPI)
A4–A9	122–127	O/Z	Parallel port address bus
CVDD	128	Supply	+VDD

† I = Input, O = Output, Z = High impedance

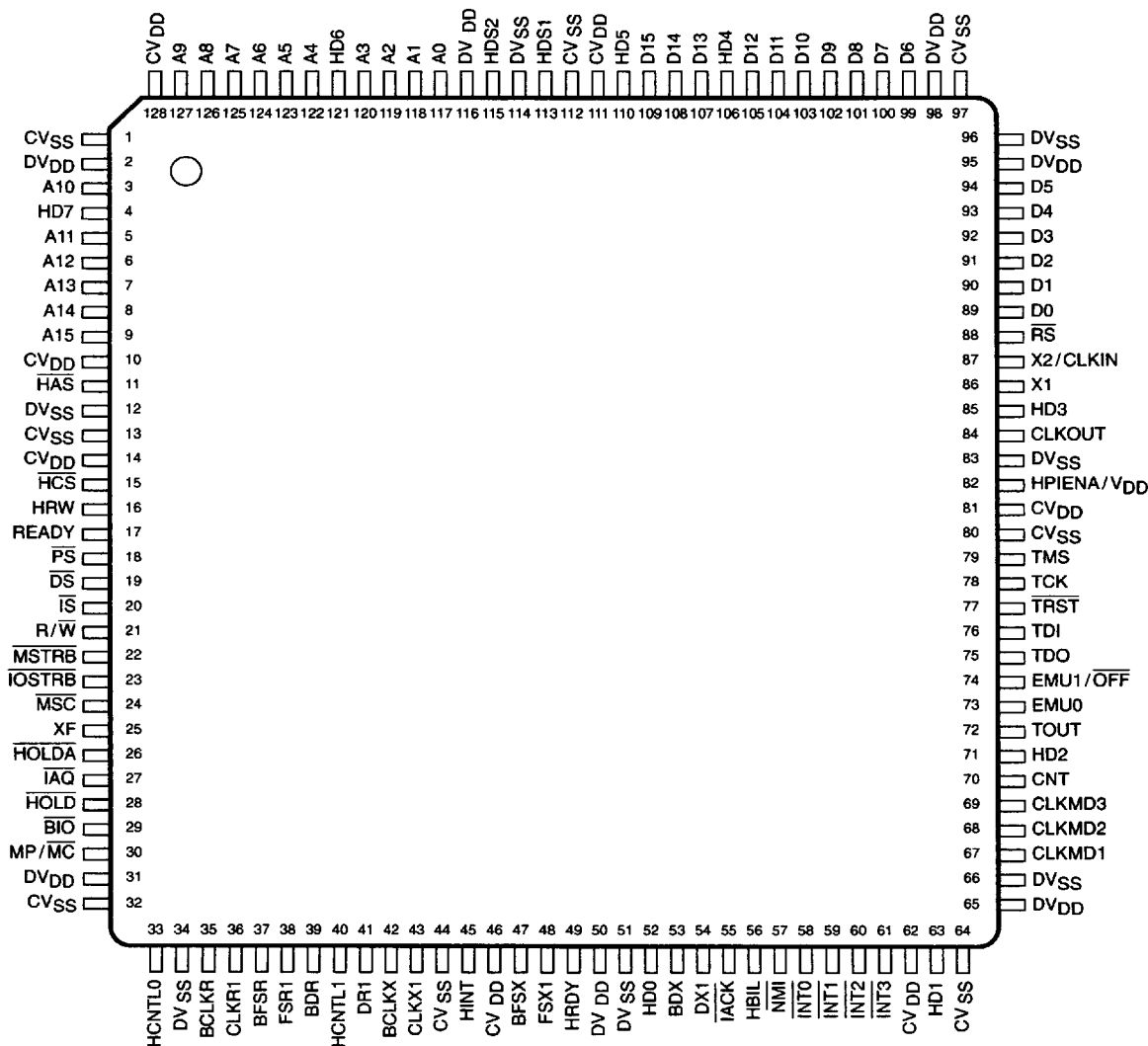
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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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TMS320LC545, TMS320VC545 PBK PACKAGE† (TOP VIEW)



† DVSS and DVDD are power supplies for I/O pins while CVSS and CVDD are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC545PBK/VC545PBK (128-pin) packages.

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC545PBK/'VC545PBK (128-Pin TQFP Package)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
CVSS	1	Supply	Ground
DVDD	2	Supply	+VDD
A10	3	O/Z	Parallel port address bus
HD7	4	I/O/Z	Parallel bi-directional data bus (HPI)
A11–A15	5–9	O/Z	Parallel port address bus
CVDD	10	Supply	+VDD
HAS	11	I	Address data strobe (HPI)
DVSS	12	Supply	Ground
CVSS	13	Supply	Ground
CVDD	14	Supply	+VDD
HCS	15	I	Chip select input (HPI)
HRW	16	I	Read/write (HPI)
READY	17	I	External access ready to complete
PS	18	O/Z	Program space select
DS	19	O/Z	Data space select
IS	20	O/Z	I/O select
R/W	21	O/Z	Read/write
MSTRB	22	O/Z	External memory access strobe
IOSTRB	23	O/Z	External I/O access strobe
MSC	24	O/Z	Microstate complete
XF	25	O/Z	External flag
HOLDA	26	O/Z	Hold acknowledge
IAQ	27	O/Z	Instruction acquisition
HOLD	28	I	Request access of local memory
BIO	29	I	Bit I/O pin
MP/MC	30	I	Microprocessor/microcomputer
DVDD	31	Supply	+VDD
CVSS	32	Supply	Ground
HCNTL0	33	I	Control inputs (HPI)
DVSS	34	Supply	Ground
BCLKR	35	I	Receive clock input (BSP)
CLKR1	36	I	Receive clock input
BFSR	37	I	Frame synchronization pulse for receive (BSP)
FSR1	38	I/O	Receive frame synchronization
BDR	39	I	Serial data receive input (BSP)
HCNTL1	40	I	Control inputs (HPI)
DR1	41	I	Serial data receive input
BCLKX	42	I/O/Z	Serial port transmit clock (BSP)
CLKX1	43	I/O/Z	Serial port transmit clock

† I = Input, O = Output, Z = High impedance



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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC545PBK/VC545PBK (128-Pin TQFP Package) (Continued)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
CVSS	44	Supply	Ground
HINT	45	O/Z	Interrupt output (HPI)
CVDD	46	Supply	+VDD
BFSX	47	I/O/Z	Frame synchronization pulse for transmit (BSP)
FSX1	48	I/O/Z	Transmit frame synchronization
HRDY	49	O/Z	Ready output (HPI)
DVDD	50	Supply	+VDD
DVSS	51	Supply	Ground
HD0	52	I/O/Z	Parallel bi-directional data bus (HPI)
BDX	53	O/Z	Serial data transmit output (BSP)
DX1	54	O/Z	Serial data transmit output
ACK	55	O/Z	Interrupt acknowledge
HBIL	56	I	Byte identification input (HPI)
NMI	57	I	Nonmaskable interrupt
INT0–INT3	58–61	I	Interrupt 0 through Interrupt 3
CVDD	62	Supply	+VDD
HD1	63	I/O/Z	Parallel bi-directional data bus (HPI)
CVSS	64	Supply	Ground
DVDD	65	Supply	+VDD
DVSS	66	Supply	Ground
CLKMD1	67	I	Clock mode pin 1
CLKMD2	68	I	Clock mode pin 2
CLKMD3	69	I	Clock mode pin 3
CNT	70	I	I/O level select
HD2	71	I/O/Z	Parallel bi-directional data bus (HPI)
TOUT	72	O/Z	Timer output
EMU0	73	I/O/Z	Emulator interrupt 0
EMU1/OFF	74	I/O/Z	Emulator interrupt 1/shutoff
TDO	75	O/Z	Test data output (IEEE standard 1149.1)
TDI	76	I	Test data input (IEEE standard 1149.1)
TRST	77	I	Test reset (IEEE standard 1149.1)
TCK	78	I	Test clock (IEEE standard 1149.1)
TMS	79	I	Test mode select (IEEE standard 1149.1)
CVSS	80	Supply	Ground
CVDD	81	Supply	+VDD
HPIENA/VDD	82	I	HPI module select input
DVSS	83	Supply	Ground
CLKOUT	84	O/Z	Machine clock output

† I = Input, O = Output, Z = High impedance

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC545PBK/'VC545PBK (128-Pin TQFP Package) (Continued)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
HD3	85	I/O/Z	Parallel bi-directional data bus (HPI)
X1	86	O	Oscillator output
X2/CLKIN	87	I	Oscillator/external clock input
\overline{RS}	88	I	Device reset
D0–D5	89–94	I/O/Z	Parallel data port
DVDD	95	Supply	+VDD
DVSS	96	Supply	Ground
CVSS	97	Supply	Ground
DVDD	98	Supply	+VDD
D6–D12	99–105	I/O/Z	Parallel data port
HD4	106	I/O/Z	Parallel bi-directional data bus (HPI)
D13–D15	107–109	I/O/Z	Parallel data port
HD5	110	I/O/Z	Parallel bi-directional data bus (HPI)
CVDD	111	Supply	+VDD
CVSS	112	Supply	Ground
HDS1	113	I	Data strobe input (HPI)
DVSS	114	Supply	Ground
HDS2	115	I	Data strobe input (HPI)
DVDD	116	Supply	+VDD
A0–A3	117–120	O/Z	Parallel port address bus
HD6	121	I/O/Z	Parallel bi-directional data bus (HPI)
A4–A9	122–127	O/Z	Parallel port address bus
CVDD	128	Supply	+VDD

† I = Input, O = Output, Z = High impedance

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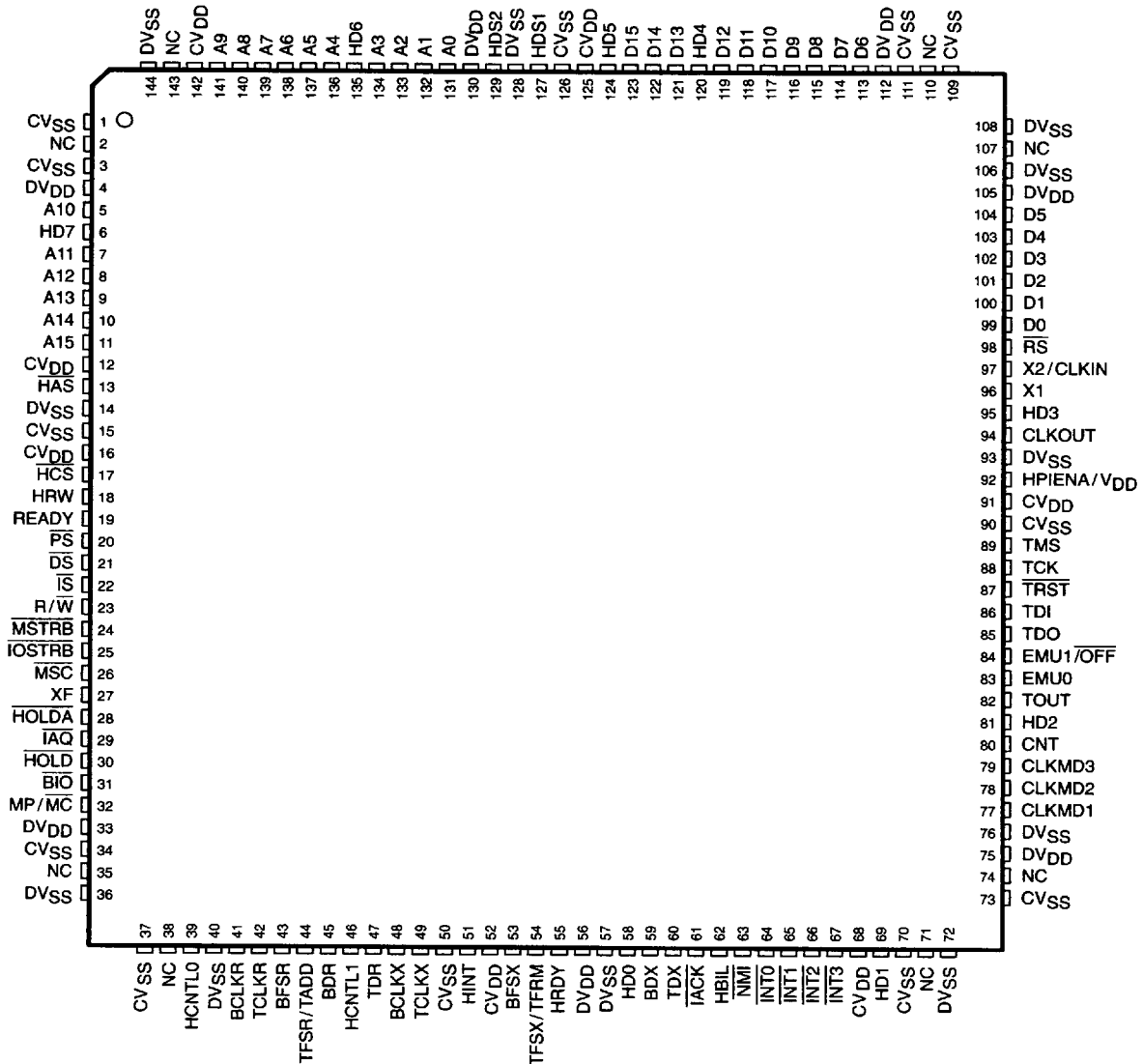
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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

SPRS039 – FEBRUARY 1996

TMS320C542/TMS320LC542/TMS320VC542 PGE PACKAGE†‡ (TOP VIEW)



† NC = No connection

‡ DVSS and DVDD are power supplies for I/O pins while CVSS and CVDD are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320C542PGE/LC542PGE/VC542PGE (144-pin) packages.

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320C542PGE/LC542PGE/VC542PGE (144-Pin TQFP Package)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
CVSS	1	Supply	Ground
NC	2	N/A	No connection
CVSS	3	Supply	Ground
DVDD	4	Supply	+VDD
A10	5	O/Z	Parallel port address bus
HD7	6	I/O/Z	Parallel bi-directional data bus (HPI)
A11–A15	7–11	O/Z	Parallel port address bus
CVDD	12	Supply	+VDD
HAS	13	I	Address data strobe (HPI)
DVSS	14	Supply	Ground
CVSS	15	Supply	Ground
CVDD	16	Supply	+VDD
HCS	17	I	Chip select input (HPI)
HRW	18	I	Read/write (HPI)
READY	19	I	External access ready to complete
PS	20	O/Z	Program space select
DS	21	O/Z	Data space select
IS	22	O/Z	I/O select
R/W	23	O/Z	Read/write
MSTRB	24	O/Z	External memory access strobe
IOSTRB	25	O/Z	External I/O access strobe
MSC	26	O/Z	Microstate complete
XF	27	O/Z	External flag
HOLDA	28	O/Z	Hold acknowledge
IAQ	29	O/Z	Instruction acquisition
HOLD	30	I	Request access of local memory
BIO	31	I	Bit I/O pin
MP/MC	32	I	Microprocessor/microcomputer
DVDD	33	Supply	+VDD
CVSS	34	Supply	Ground
NC	35	N/A	No connection
DVSS	36	Supply	Ground
CVSS	37	Supply	Ground
NC	38	N/A	No connection
HCNTL0	39	I	Control inputs (HPI)
DVSS	40	Supply	Ground
BCLKR	41	I	Receive clock input (BSP)
TCLKR	42	I	Receive clock input (TDM)
BFSR	43	I	Frame synchronization pulse for receive (BSP)
TFSR/TADD	44	I/O	Receive frame synchronization (TDM)

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION



Pin Functions for the TMS320C542PGE/LC542PGE/VC542PGE
(144-Pin TQFP Package) (Continued)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
BDR	45	I	Serial data receive input (BSP)
HCNTL1	46	I	Control inputs (HPI)
TDR	47	I	Serial data receive input (TDM)
BCLKX	48	I/O/Z	Serial port transmit clock (BSP)
TCLKX	49	I/O/Z	Serial port transmit clock (TDM)
CVSS	50	Supply	Ground
HINT	51	O/Z	Interrupt output (HPI)
CVDD	52	Supply	+VDD
BFSX	53	I/O/Z	Frame synchronization pulse for transmit (BSP)
TFSX/TFRM	54	I/O/Z	Transmit frame synchronization (TDM)
HRDY	55	O/Z	Ready output (HPI)
DVDD	56	Supply	+VDD
DVSS	57	Supply	Ground
HD0	58	I/O/Z	Parallel bi-directional data bus (HPI)
BDX	59	O/Z	Serial data transmit output (BSP)
TDX	60	O/Z	Serial data transmit output (TDM)
IACK	61	O/Z	Interrupt acknowledge
HBIL	62	I	Byte identification input (HPI)
NMI	63	I	Nonmaskable interrupt
INT0–INT3	64–67	I	Interrupt 0 through Interrupt 3
CVDD	68	Supply	+VDD
HD1	69	I/O/Z	Parallel bi-directional data bus (HPI)
CVSS	70	Supply	Ground
NC	71	N/A	No connection
DVSS	72	Supply	Ground
CVSS	73	Supply	Ground
NC	74	NA	No connection
DVDD	75	Supply	+VDD
DVSS	76	Supply	Ground
CLKMD1	77	I	Clock mode pin 1
CLKMD2	78	I	Clock mode pin 2
CLKMD3	79	I	Clock mode pin 3
CNT	80	I	I/O level select
HD2	81	I/O/Z	Parallel bi-directional data bus (HPI)
TOUT	82	O/Z	Timer output
EMU0	83	I/O/Z	Emulator interrupt 0
EMU1/OFF	84	I/O/Z	Emulator interrupt 1/shut off
TDO	85	O/Z	Test data output (IEEE standard 1149.1)

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION



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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320C542PGE/LC542PGE/VC542PGE (144-Pin TQFP Package) (Continued)

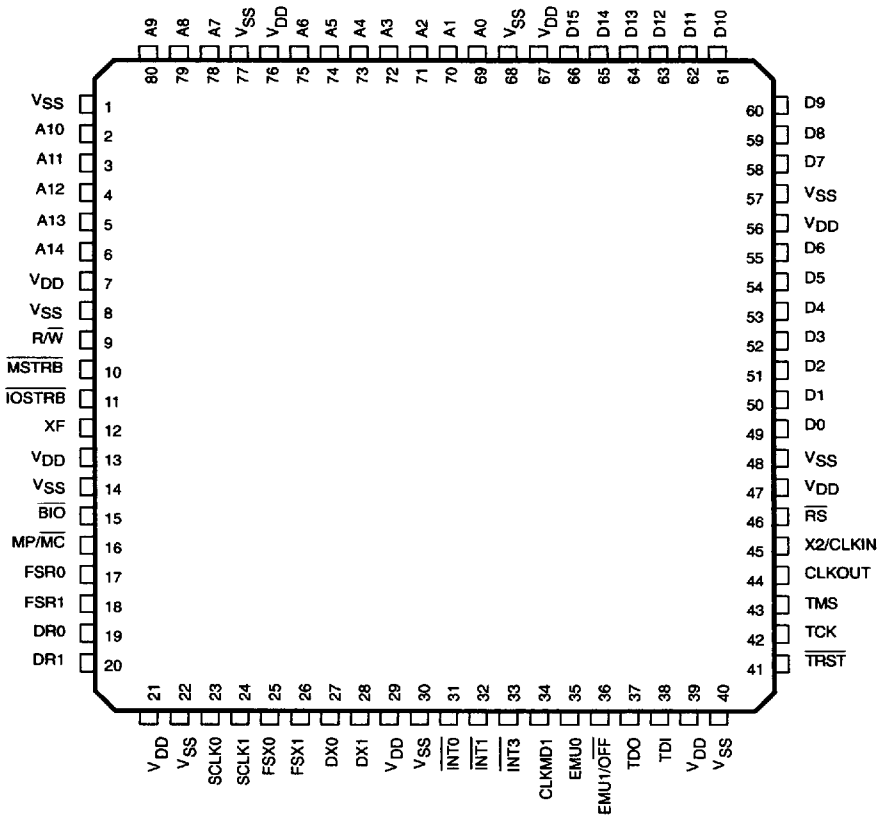
NAME	PIN NO	FUNCTION†	DESCRIPTION
TDI	86	I	Test data input (IEEE standard 1149.1)
TRST	87	I	Test reset (IEEE standard 1149.1)
TCK	88	I	Test clock (IEEE standard 1149.1)
TMS	89	I	Test mode select (IEEE standard 1149.1)
CVSS	90	Supply	Ground
CVDD	91	Supply	+VDD
HPIEN/VDD	92	I	HPI module select input
DVSS	93	Supply	Ground
CLKOUT	94	O/Z	Machine clock output
HD3	95	I/O/Z	Parallel bi-directional data bus (HPI)
X1	96	O	Oscillator output
X2/CLKIN	97	I	Oscillator/external clock input
RS	98	I	Device reset
D0–D5	99–104	I/O/Z	Parallel data port
DVDD	105	Supply	+VDD
DVSS	106	Supply	Ground
NC	107	N/A	No connection
DVSS	108	Supply	Ground
CVSS	109	Supply	Ground
NC	110	N/A	No connection
CVSS	111	Supply	Ground
DVDD	112	Supply	+VDD
D6–D12	113–119	I/O/Z	Parallel data port
HD4	120	I/O/Z	Parallel bi-directional data bus (HPI)
D13–D15	121–123	I/O/Z	Parallel data port
HD5	124	I/O/Z	Parallel bi-directional data bus (HPI)
CVDD	125	Supply	+VDD
CVSS	126	Supply	Ground
HDS1	127	I	Data strobe input (HPI)
DVSS	128	Supply	Ground
HDS2	129	I	Data strobe input (HPI)
DVDD	130	Supply	+VDD
A0–A3	131–134	O/Z	Parallel port address bus
HD6	135	I/O/Z	Parallel bi-directional data bus (HPI)
A4–A9	136–141	O/Z	Parallel port address bus
CVDD	142	Supply	+VDD
NC	143		
DVSS	144	Supply	+VDD

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION



TMS320LC544, TMS320VC544
PN PACKAGE
(TOP VIEW)



The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC544PN/TMS320VC544PN (80-pin) packages.

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC544PN/TMS320VC544PN (80-Pin TQFP Package)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
VSS	1	Supply	Ground
A10–A14	2–6	O/Z	Parallel port address bus
VDD	7	Supply	+VDD
VSS	8	Supply	Ground
R/W	9	O/Z	Read/Write
MSTRB	10	O/Z	External memory access strobe
IOSTRB	11	O/Z	External I/O access strobe
XF	12	O/Z	External flag
VDD	13	Supply	+VDD
VSS	14	Supply	Ground
BIO	15	I	Bit I/O pin
MP/MC	16	I	Microprocessor/microcomputer
FSR0	17	I	Serial port 0 receive frame synchronization
FSR1	18	I	Serial port 1 receive frame synchronization
DR0	19	I	Serial port 0 data receive
DR1	20	I	Serial port 1 data receive
VDD	21	Supply	+VDD
VSS	22	Supply	Ground
SCLK0	23	I/O/Z	Serial port 0 clock
SCLK1	24	I/O/Z	Serial port 1 clock
FSX0	25	I/O/Z	Serial port 0 transmit frame synchronization
FSX1	26	I/O/Z	Serial port 1 transmit frame synchronization
DX0	27	O/Z	Serial port 0 transmit output
DX1	28	O/Z	Serial port 1 transmit output

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION



Pin Functions for the TMS320LC544PN/TMS320VC544PN
(80-Pin TQFP Package) (Continued)

NAME	PIN NO	FUNCTION†	DESCRIPTION
V _{DD}	29	Supply	+V _{DD}
V _{SS}	30	Supply	Ground
INT0, INT1, INT3	31–33	I	Interrupt 0, 1, 3
CLKMD1	34	I	Clock mode pin 1
EMU0	35	I/O/Z	Emulator interrupt 0
EMU1/OFF	36	I/O/Z	Emulator interrupt 1/shut off
TDO	37	O/Z	Test data output (IEEE standard 1149.1)
TDI	38	I	Test data input (IEEE standard 1149.1)
V _{DD}	39	Supply	+V _{DD}
V _{SS}	40	Supply	Ground
TRST	41	I	Test reset (IEEE standard 1149.1)
TCK	42	I	Test clock (IEEE standard 1149.1)
TMS	43	I	Test mode select (IEEE standard 1149.1)
CLKOUT	44	O/Z	Machine clock output
X2/CLKIN	45	I	External clock input
RS	46	I	Device reset
V _{DD}	47	Supply	+V _{DD}
V _{SS}	48	Supply	Ground
D0–D6	49–55	I/O/Z	Parallel data port
V _{DD}	56	Supply	+V _{DD}
V _{SS}	57	Supply	Ground
D7–D15	58–66	I/O/Z	Parallel data port
V _{DD}	67	Supply	+V _{DD}
V _{SS}	68	Supply	Ground
A0–A6	69–75	O/Z	Parallel port address bus
V _{DD}	76	Supply	+V _{DD}
V _{SS}	77	Supply	Ground
A7–A9	78–80	O/Z	Parallel port address bus

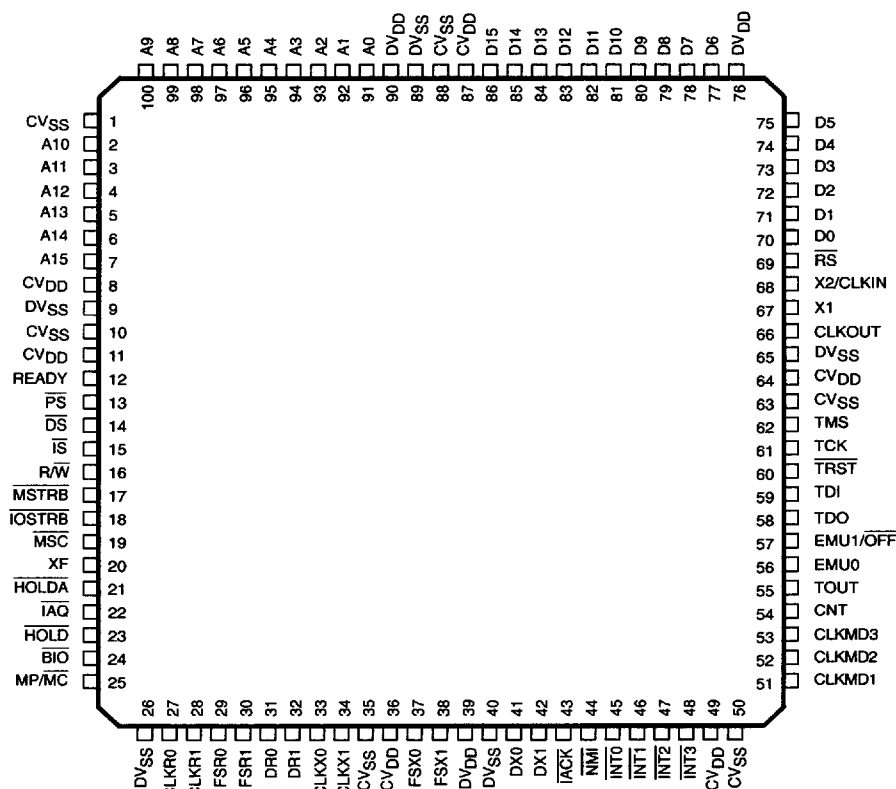
† I = Input, O = Output, Z = High impedance

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

SPRS039 – FEBRUARY 1996

TMS320C541, TMS320LC541, TMS320VC541 PZ PACKAGE† (TOP VIEW)



† DVSS and DVDD are power supplies for I/O pins while CVSS and CVDD are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320C541PZ/TMS320LC541PZ/TMS320VC541PZ (100-pin) packages.

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Pin Functions for the TMS320C541PZ/TMS320LC541PZ/TMS320VC541PZ
(100-Pin TQFP Package)

NAME	PIN NO	FUNCTION†	DESCRIPTION
CVSS	1	Supply	Ground
A10–A15	2–7	O/Z	Parallel port address bus
CVDD	8	Supply	+VDD
DVSS	9	Supply	Ground
CVSS	10	Supply	Ground
CVDD	11	Supply	+VDD
READY	12	I	External access ready to complete
PS	13	O/Z	Program space select
DS	14	O/Z	Data space select
IS	15	O/Z	I/O space select
R/W	16	O/Z	Read/write
MSTRB	17	O/Z	External memory access strobe
IOSTRB	18	O/Z	External I/O access strobe
MSC	19	O/Z	Microstate complete
XF	20	O/Z	External flag
HOLDA	21	O/Z	Hold acknowledge
IAQ	22	O/Z	Instruction acquisition
HOLD	23	I	Request access of local memory
BIO	24	I	Bit I/O pin
MP/MC	25	I	Microprocessor/microcomputer
DVSS	26	Supply	Ground
CLKR0	27	I	Serial port 0 receive clock
CLKR1	28	I	Serial port 1 receive clock
FSR0	29	I	Serial port 0 receive frame synchronization
FSR1	30	I	Serial port 1 receive frame synchronization
DR0	31	I	Serial port 0 data receive
DR1	32	I	Serial port 1 data receive
CLKX0	33	I/O/Z	Serial port 0 transmit clock
CLKX1	34	I/O/Z	Serial port 1 transmit clock
CVSS	35	Supply	Ground
CVDD	36	Supply	+VDD
FSX0	37	I/O/Z	Serial port 0 transmit frame synchronization
FSX1	38	I/O/Z	Serial port 1 transmit frame synchronization
DVDD	39	Supply	+VDD
DVSS	40	Supply	Ground
DX0	41	O/Z	Serial port 0 transmit output
DX1	42	O/Z	Serial port 1 transmit output

† I = Input, O = Output, Z = High impedance

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320C541PZ/TMS320LC541PZ/TMS320VC541PZ (100-Pin TQFP Package) (Continued)

NAME	PIN NO	FUNCTION†	DESCRIPTION
IACK	43	O/Z	Interrupt acknowledge
NMI	44	I	Non-maskable interrupt
INT0–INT3	45–48	I	Interrupt 0 through Interrupt 3
CVDD	49	Supply	+VDD
CVSS	50	Supply	Ground
CLKMD1	51	I	Clock mode pin 1
CLKMD2	52	I	Clock mode pin 2
CLKMD3	53	I	Clock mode pin 3
CNT	54	I	I/O level select
TOUT	55	O/Z	Timer output
EMU0	56	I/O/Z	Emulator interrupt 0
EMU1/OFF	57	I/O/Z	Emulator interrupt 1/shut off
TDO	58	O/Z	Test data output (IEEE standard 1149.1)
TDI	59	I	Test data input (IEEE standard 1149.1)
TRST	60	I	Test reset (IEEE standard 1149.1)
TCK	61	I	Test clock (IEEE standard 1149.1)
TMS	62	I	Test mode select (IEEE standard 1149.1)
CVSS	63	Supply	Ground
CVDD	64	Supply	+VDD
DVSS	65	Supply	Ground
CLKOUT	66	O/Z	Machine clock output
X1	67	O	Oscillator output
X2/CLKIN	68	I	Oscillator/external clock input
RS	69	I	Device reset
D0–D5	70–75	I/O/Z	Parallel data port
DVDD	76	Supply	+VDD
D6–D15	77–86	I/O/Z	Parallel data port
CVDD	87	Supply	+VDD
CVSS	88	Supply	Ground
DVSS	89	Supply	Ground
DVDD	90	Supply	+VDD
A0–A9	91–100	O/Z	Parallel port address bus

† I = Input, O = Output, Z = High impedance

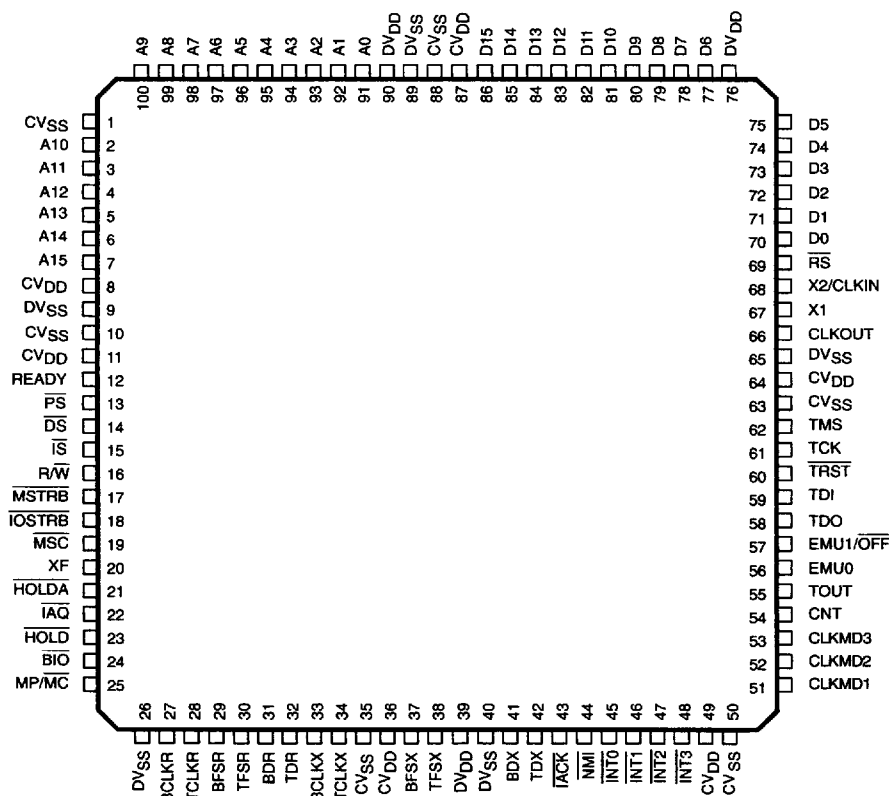
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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

SPRS039 – FEBRUARY 1996

TMS320LC543, TMS320VC543 PZ PACKAGE† (TOP VIEW)



† DVSS and DVDD are power supplies for I/O pins while CVSS and CVDD are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC543PZ/TMS320VC543PZ (100-pin) packages.

For the 'LC543 and 'VC543, the letter B in front of CLKR, FSR, DR, CLKX, FSX, and DX means buffered serial port (BSP). The letter T in front of CLKR, FSR, DR, CLKX, FSX, and DX means time-division multiplexed (TDM).

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC543PZ/TMS320VC543PZ (100-Pin TQFP Package)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
CVSS	1	Supply	Ground
A10–A15	2–7	O/Z	Parallel port address bus
CVDD	8	Supply	+VDD
DVSS	9	Supply	Ground
CVSS	10	Supply	Ground
CVDD	11	Supply	+VDD
READY	12	I	External access ready to complete
PS	13	O/Z	Program space select
DS	14	O/Z	Data space select
IS	15	O/Z	I/O space select
R/W	16	O/Z	Read/write
MSTRB	17	O/Z	External memory access strobe
IOSTRB	18	O/Z	External I/O access strobe
MSC	19	O/Z	Microstate complete
XF	20	O/Z	External flag
HOLDA	21	O/Z	Hold acknowledge
IAQ	22	O/Z	Instruction acquisition
HOLD	23	I	Request access of local memory
BIO	24	I	Bit I/O pin
MP/MC	25	I	Microprocessor/microcomputer
DVSS	26	Supply	Ground
BCLKR	27	I	Buffered serial port receive clock
TCLKR	28	I	TDM serial port receive clock
BFSR	29	I	Buffered serial port receive frame synchronization
TFSR	30	I	TDM serial port receive frame synchronization
BDR	31	I	Buffered serial port data receive
TDR	32	I	TDM serial port data receive
BCLKX	33	I/O/Z	Buffered serial port transmit clock
TCLKX	34	I/O/Z	TDM serial port transmit clock
CVSS	35	Supply	Ground
CVDD	36	Supply	+VDD
BFSX	37	I/O/Z	Buffered serial port transmit frame synchronization
TFSX	38	I/O/Z	TDM serial port transmit frame synchronization
DVDD	39	Supply	+VDD
DVSS	40	Supply	Ground
BDX	41	O/Z	Buffered serial port transmit output
TDX	42	O/Z	TDM serial port transmit output

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION



Pin Functions for the TMS320LC543PZ/TMS320VC543PZ (100-Pin TQFP Package) (Continued)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
IACK	43	O/Z	Interrupt acknowledge
NMI	44	I	Non-maskable interrupt
INT0–INT3	45–48	I	Interrupt 0 through Interrupt 3
CVDD	49	Supply	+VDD
CVSS	50	Supply	Ground
CLKMD1	51	I	Clock mode pin 1
CLKMD2	52	I	Clock mode pin 2
CLKMD3	53	I	Clock mode pin 3
CNT	54	I	I/O level select
TOUT	55	O/Z	Timer output
EMU0	56	I/O/Z	Emulator interrupt 0
EMU1/OFF	57	I/O/Z	Emulator interrupt 1/shut off
TDO	58	O/Z	Test data output (IEEE standard 1149.1)
TDI	59	I	Test data input (IEEE standard 1149.1)
TRST	60	I	Test reset (IEEE standard 1149.1)
TCK	61	I	Test clock (IEEE standard 1149.1)
TMS	62	I	Test mode select (IEEE standard 1149.1)
CVSS	63	Supply	Ground
CVDD	64	Supply	+VDD
DVSS	65	Supply	Ground
CLKOUT	66	O/Z	Machine clock output
X1	67	O	Oscillator output
X2/CLKIN	68	I	Oscillator/external clock input
RS	69	I	Device reset
D0–D5	70–75	I/O/Z	Parallel data port
DVDD	76	Supply	+VDD
D6–D15	77–86	I/O/Z	Parallel data port
CVDD	87	Supply	+VDD
CVSS	88	Supply	Ground
DVSS	89	Supply	Ground
DVDD	90	Supply	+VDD
A0–A9	91–100	O/Z	Parallel port address bus

† I = Input, O = Output, Z = High impedance

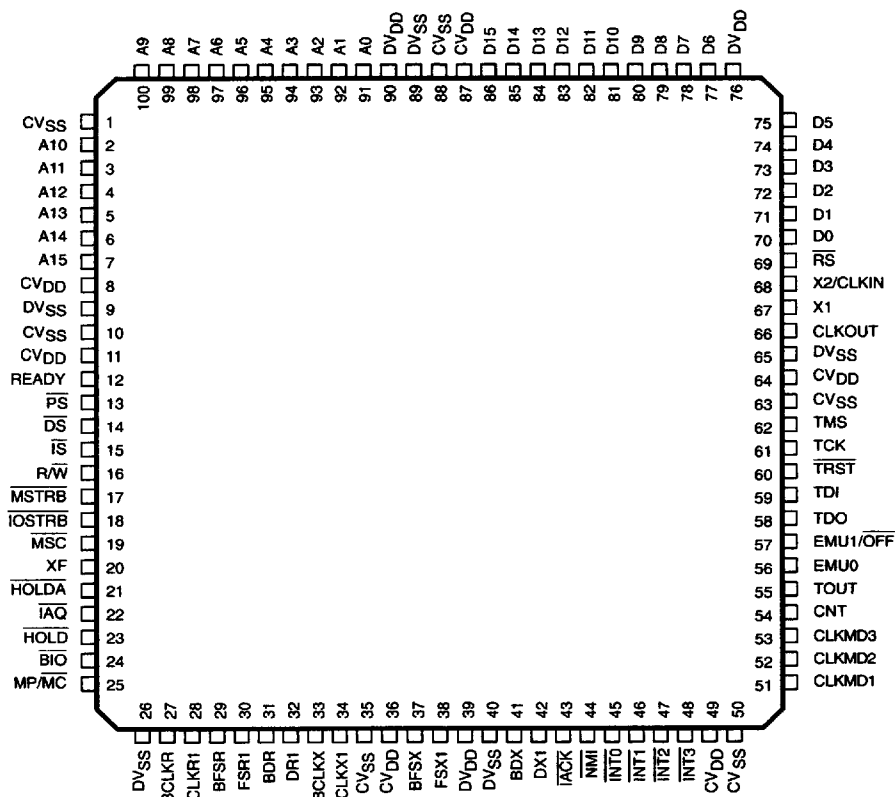
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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

SPRS039 – FEBRUARY 1996

**TMS320LC546, TMS320VC546
PZ PACKAGE†
(TOP VIEW)**



† DVSS and DVDD are power supplies for I/O pins while CVSS and CVDD are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC546PZ/TMS320VC546PZ (100-pin) packages.

For the 'LC546 and 'VC546, the letter B in front of CLKR, FSR, DR, FSX, and DX means BSP.

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC546PZ/TMS320VC546PZ (100-Pin TQFP Package)

PIN		FUNCTION†	DESCRIPTION
NAME	NO		
CVSS	1	Supply	Ground
A10–A15	2–7	O/Z	Parallel port address bus
CVDD	8	Supply	+VDD
DVSS	9	Supply	Ground
CVSS	10	Supply	Ground
CVDD	11	Supply	+VDD
READY	12	I	External access ready to complete
PS	13	O/Z	Program space select
DS	14	O/Z	Data space select
IS	15	O/Z	I/O space select
R/W	16	O/Z	Read/write
MSTRB	17	O/Z	External memory access strobe
IOSTRB	18	O/Z	External I/O access strobe
MSC	19	O/Z	Microstate complete
XF	20	O/Z	External flag
HOLDA	21	O/Z	Hold acknowledge
IAQ	22	O/Z	Instruction acquisition
HOLD	23	I	Request access of local memory
BIO	24	I	Bit I/O pin
MP/MC	25	I	Microprocessor/microcomputer
DVSS	26	Supply	Ground
BCLKR	27	I	Buffered serial port receive clock
CLKR1	28	I	Serial port 1 receive clock
BFSR	29	I	Buffered serial port receive frame synchronization
FSR1	30	I	Serial port 1 receive frame synchronization
BDR	31	I	Buffered serial port data receive
DR1	32	I	Serial port 1 data receive
BCLKX	33	I/O/Z	Buffered serial port transmit clock
CLKX1	34	I/O/Z	Serial port 1 transmit clock
CVSS	35	Supply	Ground
CVDD	36	Supply	+VDD
BFSX	37	I/O/Z	Buffered serial port transmit frame synchronization
FSX1	38	I/O/Z	Serial port 1 transmit frame synchronization
DVDD	39	Supply	+VDD
DVSS	40	Supply	Ground
BDX	41	O/Z	Buffered serial port transmit output
DX1	42	O/Z	Serial port 1 transmit output

† I = Input, O = Output, Z = High impedance

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Pin Functions for the TMS320LC546PZ/TMS320VC546PZ (100-Pin TQFP Package) (Continued)

NAME	PIN NO	FUNCTION†	DESCRIPTION
IACK	43	O/Z	Interrupt acknowledge
NMI	44	I	Non-maskable interrupt
INT0–INT3	45–48	I	Interrupt 0 through Interrupt 3
CVDD	49	Supply	+VDD
CVSS	50	Supply	Ground
CLKMD1	51	I	Clock mode pin 1
CLKMD2	52	I	Clock mode pin 2
CLKMD3	53	I	Clock mode pin 3
CNT	54	I	I/O level select
TOUT	55	O/Z	Timer output
EMU0	56	I/O/Z	Emulator interrupt 0
EMU1/OFF	57	I/O/Z	Emulator interrupt 1/shut off
TDO	58	O/Z	Test data output (IEEE standard 1149.1)
TDI	59	I	Test data input (IEEE standard 1149.1)
TRST	60	I	Test reset (IEEE standard 1149.1)
TCK	61	I	Test clock (IEEE standard 1149.1)
TMS	62	I	Test mode select (IEEE standard 1149.1)
CVSS	63	Supply	Ground
CVDD	64	Supply	+VDD
DVSS	65	Supply	Ground
CLKOUT	66	O/Z	Machine clock output
X1	67	O	Oscillator output
X2/CLKIN	68	I	Oscillator/external clock input
RS	69	I	Device reset
D0–D5	70–75	I/O/Z	Parallel data port
DVDD	76	Supply	+VDD
D6–D15	77–86	I/O/Z	Parallel data port
CVDD	87	Supply	+VDD
CVSS	88	Supply	Ground
DVSS	89	Supply	Ground
DVDD	90	Supply	+VDD
A0–A9	91–100	O/Z	Parallel port address bus

† I = Input, O = Output, Z = High impedance

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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The following tables list each signal, function, and operating mode(s) grouped by function.

Signal Descriptions

PIN		DESCRIPTION
NAME	TYPE†	
DATA SIGNALS		
A15 (MSB) A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)	O/Z	Parallel address bus A15 (MSB) through A0 (LSB). A15–A0 are multiplexed to address external data/program memory or I/O. A15–A0 are placed in the high-impedance state in the hold mode. A15–A0 also go into the high-impedance state when $\overline{\text{OFF}}$ is low.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). D15–D0 are multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. D15–D0 are placed in high-impedance state when not output or when $\overline{\text{RS}}$ or $\overline{\text{HOLD}}$ is asserted. D15–D0 also go into the high-impedance state when $\overline{\text{OFF}}$ is low. The data bus has a feature called bus holder that eliminates passive components and power dissipation associated with it. The bus holder keeps the data bus at the previous logic level when the bus goes into a high-impedance state.
INITIALIZATION, INTERRUPT AND RESET OPERATIONS		
$\overline{\text{IACK}}$	O/Z	Interrupt acknowledge signal. $\overline{\text{IACK}}$ indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–0. $\overline{\text{IACK}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{INT3}}$	I	External user interrupt inputs. $\overline{\text{INT0}}$ – $\overline{\text{INT3}}$ are prioritized and maskable by the interrupt mask register and interrupt mode bit. $\overline{\text{INT0}}$ – $\overline{\text{INT3}}$ can be polled and reset by the interrupt flag register.
$\overline{\text{NMI}}$	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is an external interrupt that cannot be masked via the INTM or the IMR. When $\overline{\text{NMI}}$ is activated, the processor traps to the appropriate vector location.
$\overline{\text{RS}}$	I	Reset input. $\overline{\text{RS}}$ causes the DSP to terminate execution and forces the program counter to 0FF80h. When $\overline{\text{RS}}$ is brought to a high level, execution begins at location 0FF80h of program memory. $\overline{\text{RS}}$ affects various registers and status bits.

† I = Input, O = Output, Z = High impedance

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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Signal Descriptions (Continued)

PIN		DESCRIPTION
NAME	TYPE†	
INITIALIZATION, INTERRUPT AND RESET OPERATIONS (CONTINUED)		
MP/ \overline{MC}	I	Microprocessor/microcomputer mode-select pin. If active low at reset (microcomputer mode), MP / \overline{MC} causes the internal program ROM to be mapped into the upper 28K ('C541, 'LC541 and 'VC541) words of program memory space. In the microprocessor mode, off-chip memory and its corresponding addresses instead of internal program ROM are accessed by the DSP.
CNT	I	I/O level select. For 5-V operation, all input and output voltage levels are TTL-compatible when CNT is pulled down to a low level. For 3-V operation with CMOS-compatible I/O interface levels, CNT is pulled to a high level.
MULTIPROCESSING SIGNALS		
\overline{BIO}	I	Branch control input. A branch can be conditionally executed when \overline{BIO} is active. If low, the processor executes the conditional instruction. The \overline{BIO} condition is sampled during the decode phase of the pipeline for XC instruction, and all other instructions sample \overline{BIO} during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or as a general-purpose output pin. XF goes into the high-impedance state when \overline{OFF} is low, and is set high at reset.
MEMORY CONTROL SIGNALS		
\overline{DS} \overline{PS} \overline{IS}	O/Z	Data, program, and I/O space select signals. \overline{DS} , \overline{PS} , and \overline{IS} are always high unless driven low for communicating to a particular external space. Active period corresponds to valid address information. Placed into a high-impedance state in hold mode. \overline{DS} , \overline{PS} , and \overline{IS} also go into the high-impedance state when \overline{OFF} is low.
\overline{MSTRB}	O/Z	Memory strobe signal. \overline{MSTRB} is always high unless low-level asserted to indicate an external bus access to data or program memory. Placed in high-impedance state in hold mode. \overline{MSTRB} also goes into the high-impedance state when \overline{OFF} is low.
READY	I	Data ready input. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/ \overline{W}	O/Z	Read/write signal. R/ \overline{W} indicates transfer direction during communication to an external device and is normally in read mode (high), unless asserted low when the DSP performs a write operation. Placed in the high-impedance state in hold mode, R/ \overline{W} also goes into the high-impedance state when \overline{OFF} is low.
\overline{IOSTRB}	O/Z	I/O strobe signal. \overline{IOSTRB} is always high unless low level asserted to indicate an external bus access to an I/O device. Placed in high-impedance state in hold mode. \overline{IOSTRB} also goes into the high-impedance state when \overline{OFF} is low.
\overline{HOLD}	I	Hold input. \overline{HOLD} is asserted to request control of the address, data, and control lines. When acknowledged by the 'C54x, these lines go into high-impedance state.
\overline{HOLDA}	O/Z	Hold acknowledge signal. \overline{HOLDA} indicates to the external circuitry that the processor is in a hold state and that the address, data, and control lines are in a high-impedance state allowing them to be available to the external circuitry. \overline{HOLDA} also goes into the high-impedance state when \overline{OFF} is low.
\overline{MSC}	O/Z	Microstate complete signal. \overline{MSC} goes low when the last wait state of two or more internal software wait states programmed are executed. If connected to the READY line, it forces one external wait state after the last internal wait state has been completed. \overline{MSC} also goes into the high-impedance state when \overline{OFF} is low.
\overline{IAQ}	O/Z	Instruction acquisition signal. \overline{IAQ} is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when \overline{OFF} is low.

† I = Input, O = Output, Z = High impedance

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Signal Descriptions (Continued)

PIN		DESCRIPTION
NAME	TYPE†	
OSCILLATOR/TIMER SIGNALS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. CLKOUT also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode external/internal input signals. They allow you to select and configure different clock modes such as crystal, external clock, various PLL factors.
X2/CLKIN	I	Input pin to internal oscillator from the crystal. If the internal (crystal) oscillator is not being used, a clock can become input to the device using this pin. The internal machine cycle time is determined by the clock operating mode pins (CLKMD1, CLKMD2 and CLKMD3).
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when $\overline{\text{OFF}}$ is low.
TOUT	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT cycle wide. TOUT also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
BUFFERED SERIAL PORT (BSP) SIGNALS		
BCLKR	I	Receive clock input. BCLKR serves as the serial shift clock for the buffered serial port receiver.
BDR	I	Serial data receive input.
BFSR	I	Frame synchronization pulse for receive input. The BFSR pulse initiates the receive data process over BDR.
BCLKX	I/O/Z	Transmit clock. BCLKX serves as the serial shift clock for the buffered serial port transmitter. If $\overline{\text{RS}}$ is asserted when BCLKX is configured as output, then BCLKX is turned into input mode by reset operation. BCLKX goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
BDX	O/Z	Serial data transmit output. BDX is placed in the high-impedance state when not transmitting, when $\overline{\text{RS}}$ is asserted or when $\overline{\text{OFF}}$ is low.
BFSX	I/O/Z	Frame synchronization pulse for transmit input/output. The BFSX pulse initiates the transmit data process over BDX. If $\overline{\text{RS}}$ is asserted when BFSX is configured as output, then BFSX is turned into input mode by reset operation. BFSX goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
SERIAL PORT 0 AND SERIAL PORT 1 SIGNALS		
CLKR0 CLKR1	I	Receive clocks. External clock signal for clocking data from the data receive (DR) pin into the serial port receive shift registers (RSR). Must be present during serial port transfers. If the serial port is not being used, CLKR0 and CLKR1 can be sampled as an input via IN0 bit of the SPC register.
CLKX0 CLKX1	I/O/Z	Transmit clock. Clock signal for clocking data from the serial port transmit shift register (XSR) to the data transmit (DX) pin. CLKX can be an input if MCM in the serial port control register is cleared to 0. It also can be driven by the device at 1/4 CLKOUT frequency when MCM is set to 1. If the serial port is not used, CLKX can be sampled as an input via IN1 of the SPC register. CLKX0 and CLKX1 go into the high-impedance state when $\overline{\text{OFF}}$ is low.
DR0 DR1	I	Serial-data-receive input. Serial data is received in the RSR by DR.
DX0 DX1	O/Z	Serial port transmit output. Serial data is transmitted from the XSR via DX. DX0 and DX1 are placed in the high-impedance state when not transmitting and when $\overline{\text{OFF}}$ is low.
FSR0 FSR1	I	Frame synchronization pulse for receive input. The falling edge of the FSR pulse initiates the data-receive process, beginning the clocking of the RSR.
FSX0 FSX1	I/O/Z	Frame synchronization pulse for transmit input/output. The falling edge of the FSX pulse initiates the data transmit process, beginning the clocking of the XSR. Following reset, the default operating condition of FSX is an input. FSX0 and FSX1 can be selected by software to be an output when TXM in the serial control register is set to 1. This pin goes into the high-impedance state when $\overline{\text{OFF}}$ is low.

† I = Input, O = Output, Z = High impedance

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Signal Descriptions (Continued)

PIN		DESCRIPTION
NAME	TYPE†	
TDM SERIAL PORT SIGNAL		
TCLKR	I	Receive clock input
TDR	I	Serial data receive input
TFSR/TADD	I/O	Receive frame synchronization or address
TCLKX	I/O/Z	Transmit clock
TDX	O/Z	Serial data transmit output
TFSX/TFRM	I/O/Z	Transmit frame synchronization
MISCELLANEOUS PIN		
NC		No connection
HOST PORT INTERFACE SIGNALS		
HD0–HD7	I/O/Z	Parallel bi-directional data bus. HD0–HD7 are placed in high-impedance state when not outputting data. The signals go into the high-impedance state when $\overline{\text{OFF}}$ is low.
HCNTL0 HCNTL1	I	Control inputs
HBIL	I	Byte identification input
HCS	I	Chip select input
HDS1 HDS2	I	Data strobe inputs
HAS	I	Address strobe input
HRW	I	Read/write input
HRDY	O/Z	Ready output. This signal goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
HINT	O/Z	Interrupt output. When the DSP is in reset, this signal is driven high. The signal goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
HPIENA/V _{DD}	I	HPI module select input. This signal must be tied to V _{DD} to have HPI selected. If this input is left open or connected to ground, HPI module will not be selected, internal pullup for HPI input pins are enabled and HPI data bus has keepers set.
SUPPLY PINS		
CV _{SS}	Supply	Ground. CV _{SS} is the dedicated power supply for the core CPU.
CV _{DD}	Supply	+V _{DD} . CV _{DD} is the dedicated power supply for the core CPU.
DV _{SS}	Supply	Ground. DV _{SS} is the dedicated power supply for I/O pins.
DV _{DD}	Supply	+V _{DD} . DV _{DD} is the dedicated power supply for I/O pins.
TEST PINS		
TCK	I	IEEE standard 1149.1 test clock. This is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TD	I	IEEE standard 1149.1 test data input, pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. TDO also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.

† I = Input, O = Output, Z = High impedance



Signal Descriptions (Continued)

PIN		DESCRIPTION
NAME	TYPE†	
TEST PINS (CONTINUED)		
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{\text{TRST}}$	I	IEEE standard 1149.1 test reset. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pullup device.
EMU0	I/O/Z	Emulator 0 pin. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output via IEEE standard 1149.1 scan system.
EMU1/ $\overline{\text{OFF}}$	I/O/Z	Emulator 1 pin/disable all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/ $\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output via IEEE standard 1149.1 scan system. When $\overline{\text{TRST}}$ is driven low, EMU1/ $\overline{\text{OFF}}$ is configured as $\overline{\text{OFF}}$. The EMU1/ $\overline{\text{OFF}}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Thus, for $\overline{\text{OFF}}$ condition, the following conditions apply: $\overline{\text{TRST}}$ = low, EMU0 = high EMU1/ $\overline{\text{OFF}}$ = low

† I = Input, O = Output, Z = High impedance

architecture

The 'C54x/'LC54x/'VC54x DSPs use an advanced, modified Harvard architecture that maximizes processing power by maintaining three separate bus structures for data memory and one for program memory. Separate program and data spaces allow simultaneous access to program instructions and data, providing a high degree of parallelism. For example, two reads and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that all can be performed in a single machine cycle. In addition, the 'C54x/'LC54x/'VC54x include the control mechanisms to manage interrupts, repeated operations, and function calling.

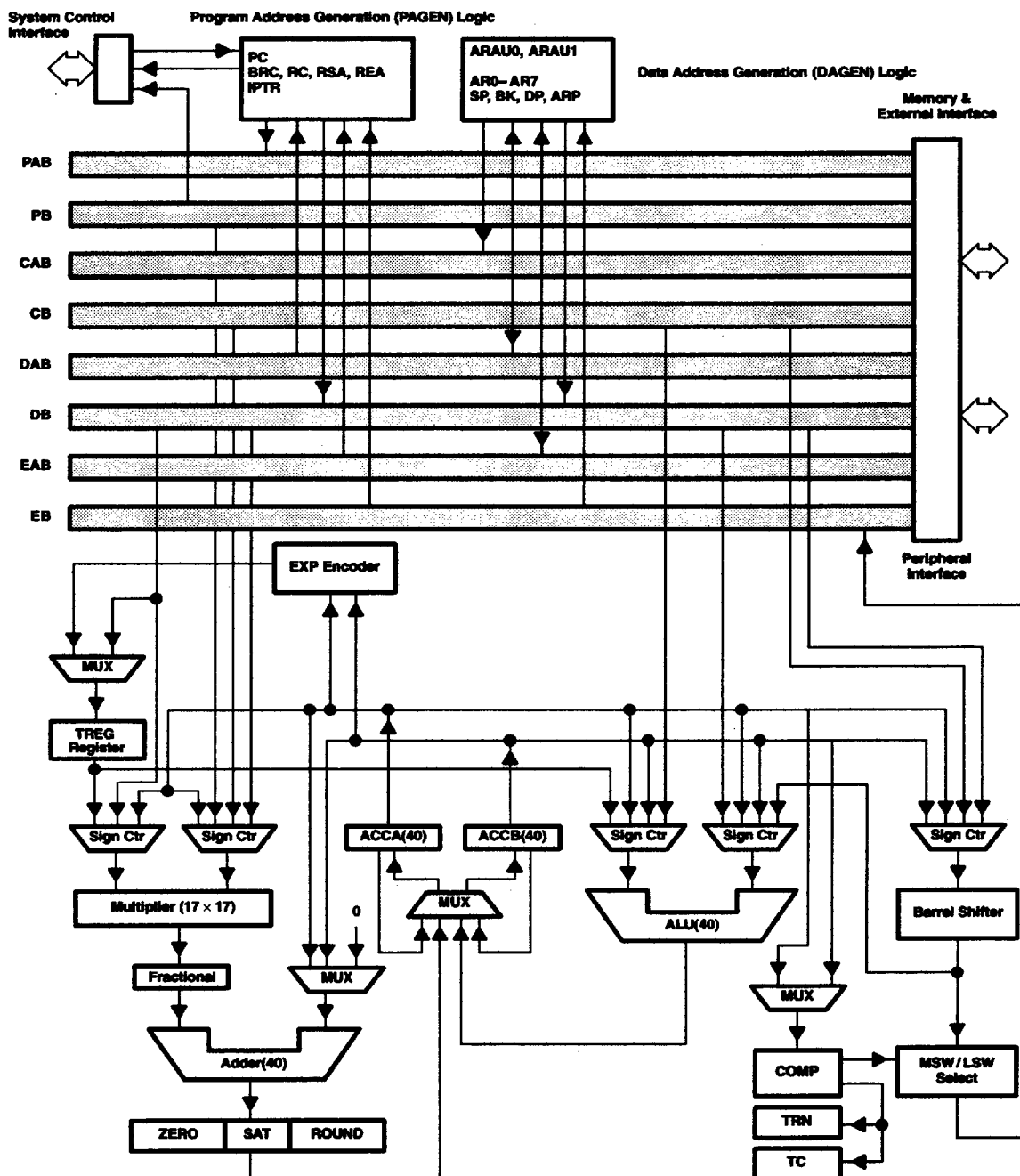
The functional block diagram includes the principal blocks and bus structure in the 'C54x/'LC54x/'VC54x devices.



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functional block diagram of the 'C54x/'LC54x/'VC54x internal hardware



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bus structure

The 'C54x/'LC54x/'VC54x device architecture is built around eight major 16-bit buses:

- One program bus (P bus), which carries the instruction code and immediate operands from program memory
- Three data buses (CB, DB, and EB), which interconnect to various elements, such as the CPU, data-address generation logic, program-address generation logic, on-chip peripherals, and data memory
 - The CB and DB carry the operands read from data memory.
 - The EB carries the data to be written to memory.
- Four address buses (PAB, CAB, DAB, and EAB), which carry the addresses needed for instruction execution

The 'C54x/'LC54x/'VC54x devices have the capability to generate up to two data memory addresses per cycle, which are stored into two auxiliary register arithmetic units (ARAU0 and ARAU1).

The program bus (PB) can carry data operands stored in program space (for instance, a coefficient table) to the multiplier for multiply/accumulate operations or to a destination in data space for the data move instruction. This capability allows implementation of single-cycle three-operand instructions such as FIRS.

The 'C54x/'LC54x/'VC54x devices also have an on-chip bi-directional bus for accessing on-chip peripherals; this bus is connected to DB and EB through the bus exchanger in the CPU interface. Accesses using this bus can require more than two cycles for reads and writes depending on the peripheral's structure.

The 'C54x/'LC54x/'VC54x devices can have bus keepers connected to the data bus. Bus keepers ensure that the data bus does not float. When bus keepers are enabled, the data bus maintains its previous level. Setting bit 1 of the bank switching control register (BSCR) enables bus keepers and clearing bit 1 disables the bus keepers. Resets automatically disable the bus keepers.

Table 2 summarizes the buses used by various types of accesses.

Table 2. Bus Usage for Accesses

ACCESS TYPE	ADDRESS BUS				DATA BUS			
	PAB	CAB	DAB	EAB	PB	CB	DB	EB
Program read	√				√			
Program write	√							√
Data single read			√				√	
Data dual read		√	√			√	√	
Data long (32-bit) read		√(hw)	√(lw)			√(hw)	√(lw)	
Data single write				√				√
Data read/data write			√	√			√	√
Dual read/coefficient read	√	√	√		√	√	√	
Peripheral read			√				√	
Peripheral write				√				√

Legend:

hw = high 16-bit word

lw = low 16-bit word



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central processing unit (CPU)

The CPU of the 'C54x/'LC54x/'VC54x devices contains:

- A 40-bit arithmetic logic unit (ALU)
- Two 40-bit accumulators
- A barrel shifter
- A 17×17 -bit multiplier
- A compare select and store unit (CSSU)

arithmetic logic unit (ALU)

The 'C54x/'LC54x/'VC54x perform 2s-complement arithmetic using: a 40-bit arithmetic logic unit (ALU) and two 40-bit accumulators (ACCA and ACCB). The ALU also can perform Boolean operations.

The ALU can function as two 16-bit ALUs and perform two 16-bit operations simultaneously when the C16 bit in status register 1 (ST1) is set.

accumulators

The accumulators, ACCA and ACCB, store the output from the ALU or the multiplier/adder block; the accumulators can also provide a second input to the ALU or the multiplier/adder. The accumulators are divided into three parts:

- Guard bits (bits 32–39)
- A high-order word (bits 16–31)
- A low-order word (bits 0–15)

Instructions are provided for storing the guard bits, the high- and the low-order accumulator words in data memory, and for manipulating 32-bit accumulator words in or out of data memory. Also, any of the accumulators can be used as temporary storage for the other.

barrel shifter

The 'C54x/'LC54x/'VC54x's barrel shifter has a 40-bit input connected to the accumulator, or data memory (C, D bus) and a 40-bit output connected to the ALU, or data memory (E bus). The barrel shifter produces a left shift of 0 to 31 bits and a right shift of 0 to 16 bits on the input data. The shift requirements are defined in the shift count field (ASM) of ST1 or defined in the temporary register (TREG), which is designated as a shift count register. This shifter and the exponent detector normalize the values in an accumulator in a single cycle. The LSBs of the output are filled with 0s and the MSBs can be either zero-filled or sign-extended, depending on the state of the sign-extended mode bit (SXM) of ST1. Additional shift capabilities enable the processor to perform numerical scaling, bit extraction, extended arithmetic, and overflow prevention operations.

multiplier/adder

The multiplier/adder performs 17×17 -bit 2s-complement multiplication with a 40-bit accumulation in a single instruction cycle. The multiplier/adder block consists of several elements: a multiplier, adder, signed/unsigned input control, fractional control, a zero detector, a rounder (2s-complement), overflow/saturation logic, and TREG. The multiplier has two inputs: one input is selected from either TREG, data memory operand, or an accumulator; the other is selected from either program memory, data memory, an accumulator, or an immediate value. The fast on-chip multiplier allows the 'C54x to efficiently perform operations such as convolution, correlation, and filtering.

In addition, the multiplier and ALU together execute multiply/accumulate (MAC) computations and ALU operations in parallel in a single instruction cycle. This function is used in determining the Euclid distance, and implementing symmetrical and LMS filters, which are required for complex DSP algorithms.

compare, select and store unit (CSSU)

The compare, select, and store unit (CSSU) performs maximum comparisons between the accumulator's high and low word, allows test/control (TC) flag bit of status control register 0 (ST0) and transition (TRN) register to keep their transition histories, and selects larger word in accumulator to be stored into data memory. The CSSU also accelerates Viterbi-type butterfly computation with optimized on-chip hardware.

program control

Program control is provided by several hardware and software mechanisms:

- The program controller decodes instructions, manages the pipeline, stores the status of operations, and decodes conditional operations. Some of the hardware elements included in the program controller are the program counter, the status and control register, the stack, and the address-generation logic.
- Some of the software mechanisms used for program control include branches, calls, conditional instructions, a repeat instruction, reset, and interrupts.

power-down modes

There are three power-down modes, activated by the IDLE1, IDLE2, and IDLE3 instructions. In these modes, the 'C54x/'LC54x/'VC54x enters a dormant state and dissipates considerably less power than in normal operation. The IDLE1 instruction is used to shut down the CPU. The IDLE2 instruction is used to shut down the CPU and on-chip peripherals. The IDLE3 instruction is used to completely shut down the 'C54x/'LC54x/'VC54x processor. This instruction stops the PLL circuitry as well as the CPU and peripherals.

memory

The total memory address range of the 'C54x/'LC54x/'VC54x devices is 192K 16-bit words. The memory space is divided into three specific memory segments: 64K word program, 64K-word data, and 64K-word I/O. The program memory space contains the instructions to be executed as well as tables used in execution. The data memory space stores data used by the instructions. The I/O memory space interfaces to external memory-mapped peripherals and can also serve as extra data storage space.

The parallel nature of the architecture of these DSPs allows them to perform four concurrent memory operations in any given machine cycle: fetching an instruction, reading two operands, and writing an operand. The four parallel buses are the program-read bus (PB), the write-data bus (EB) and two read-data buses (CB and DB). Each bus accesses different memory spaces for different aspects of the DSPs operation. Additionally, this architecture allows dual-operand reads, 32-bit-long word accesses, and a single read with a parallel store.

The 'C54x/'LC54x/'VC54x DSPs include on-chip memory to aid in system performance and integration.

on-chip ROM

The 'C541, 'LC541 and 'VC541 all feature a 28K-word \times 16-bit on-chip maskable ROM. 8K words of the 'C541, 'LC541 and 'VC541 ROM can be mapped into program and data memory space if the data ROM (DROM) bit in the processor mode status (PMST) register is set. This allows an instruction to use data stored in the ROM as an operand.

The 'LC544 and 'VC544 both feature a 24K-word \times 16-bit on-chip maskable ROM. 8K words of the 'LC544 and 'VC544 ROM can be mapped into program and data memory space if the DROM bit in the PMST register is set.

The 'LC545/'VC545/'LC546/'VC546 all feature a 48K-word \times 16-bit on-chip maskable ROM. 16K words of the ROM on these devices can be mapped into program and data memory space if the DROM bit in the PMST register is set.

The 'C542/'LC542/'VC542/'LC543/'VC543 all feature 2K-word \times 16-bit on-chip ROM.

Customers can arrange to have the ROM of the 'C54x/'LC54x/'VC54x programmed with contents unique to any particular application.



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on-chip ROM (continued)

A boot loader is available in the standard 'C54x/'LC54x/'VC54x on-chip ROM. This boot loader can be used to transfer user code from an external source to anywhere in the program memory at power up automatically. If MP/MC of the device is sampled low during a hardware reset, execution begins at location FF80h of the on-chip ROM. This location contains a branch instruction to the start of the boot loader program. The standard 'C54x/'LC54x/'VC54x devices provide different ways to download the code to accommodate various system requirements:

- Parallel from 8-bit of 16-bit wide EPROM
- Parallel from I/O space 8-bit of 16-bit mode
- Serial boot from serial ports 8-bit of 16-bit mode
- Host port interface boot ('C542, 'LC542, 'VC542, 'LC545, 'VC545 devices only)
- Warm boot

on-chip dual-access RAM

The 'C541, 'LC541 and 'VC541 devices have a 5K-word \times 16-bit on-chip dual-access RAM (DARAM) (5 blocks of 1K-word each).

The 'C542, 'LC542, 'VC542, 'LC543 and 'VC543 have a 10K-word \times 16-bit on-chip DARAM (5 blocks of 2K-word each).

The 'LC544 and 'VC544 have a 4K-word \times 16-bit on-chip DARAM (2 blocks of 2K-word each).

The 'LC545, 'VC545, 'LC546 and 'VC546 have a 6K-word \times 16-bit on-chip DARAM (3 blocks of 2K-word each).

Each of these RAM blocks can be accessed twice per machine cycle. This memory is intended primarily to store data values; however, it can be used to store program as well. At reset, the DARAM is mapped into data memory space. DARAM can be mapped into program/data memory space by setting the OVLY bit in the PMST register.

on-chip memory security

The 'C54x/'LC54x/'VC54x devices have a maskable option to protect the contents of on-chip memories. When the related bit is set, no externally originating instruction can access the on-chip memory spaces.

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on-chip memory security (continued)

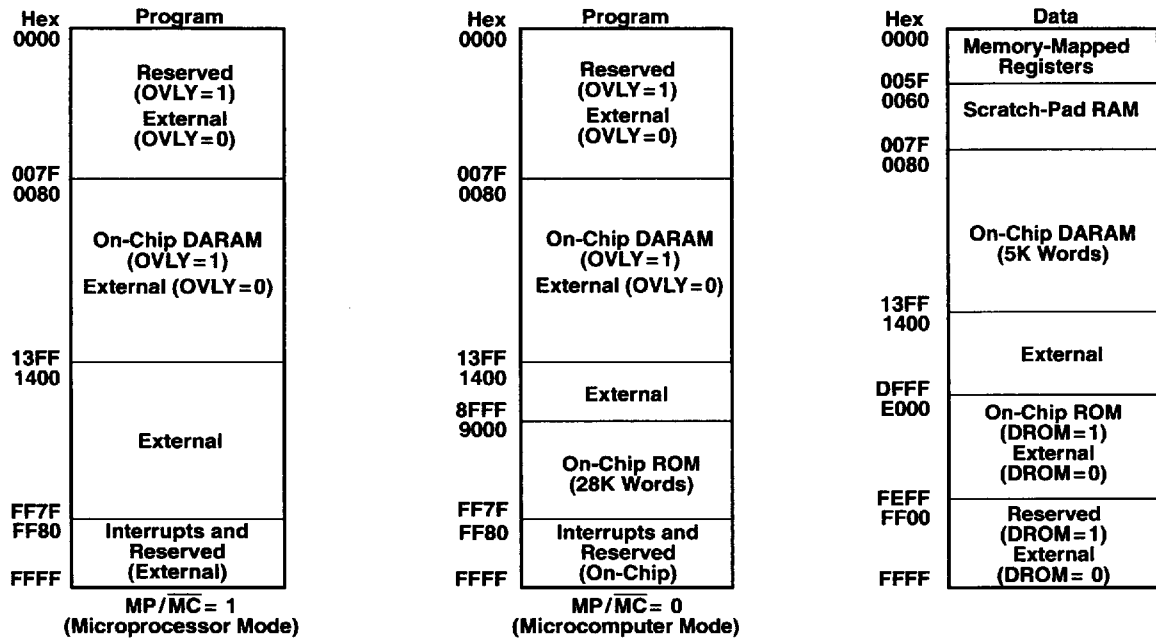


Figure 1. Memory Map ('C541, 'LC541, 'VC541)

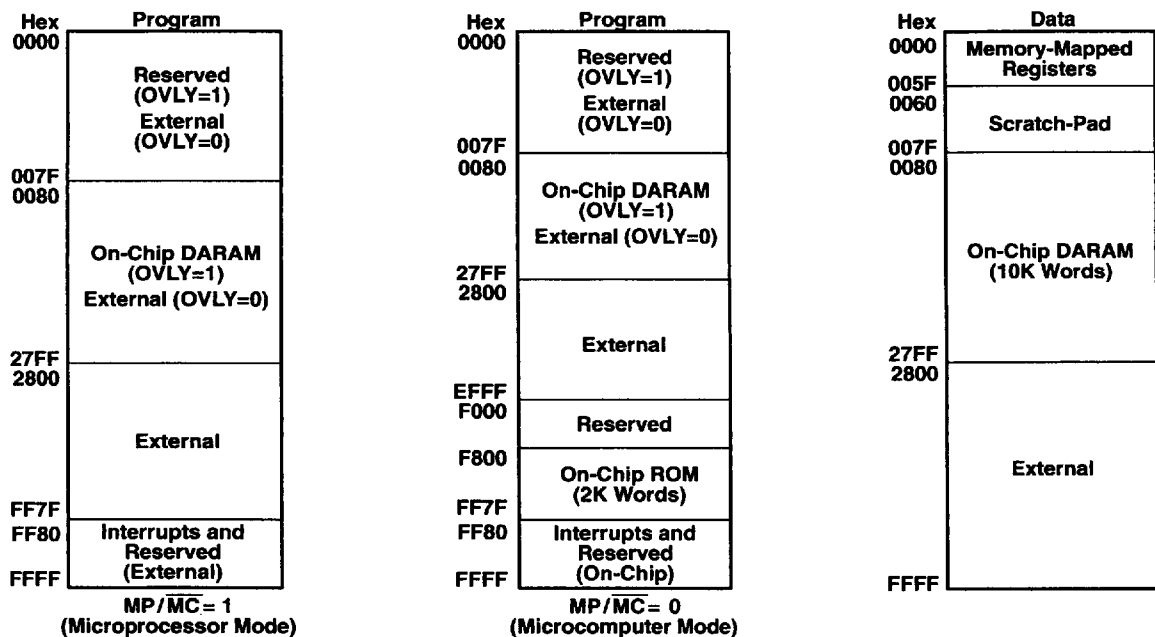


Figure 2. Memory Map ('C542, 'LC542, 'VC542, 'LC543 and 'VC543)



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on-chip memory security (continued)

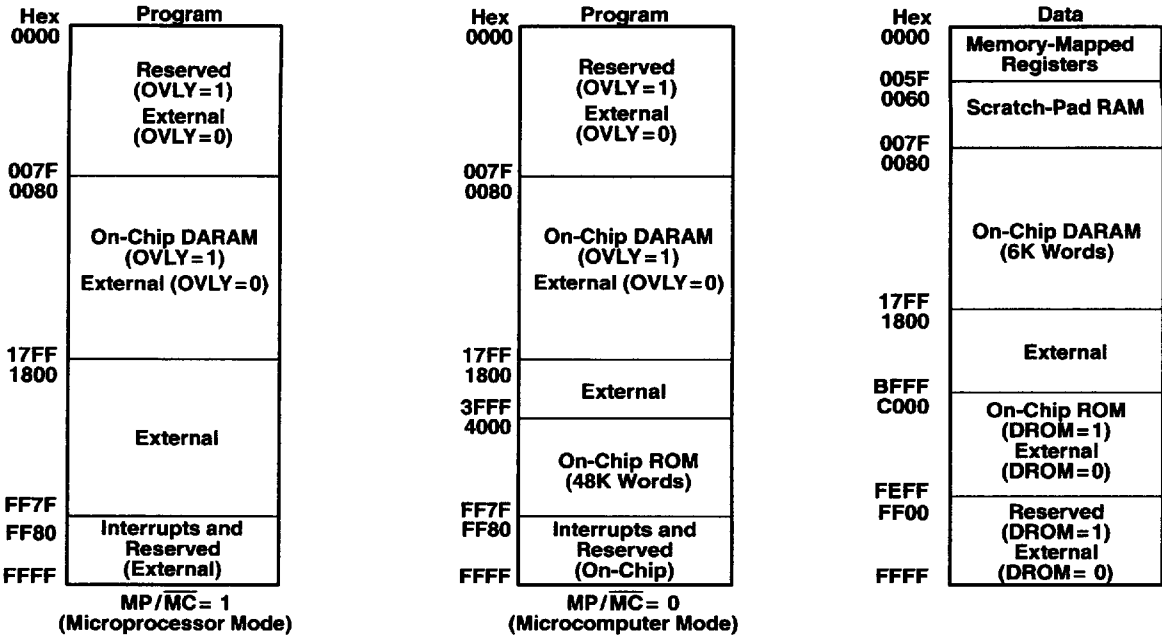


Figure 3. Memory Map ('LC545, 'VC545, 'LC546, and 'VC546)

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'LC544/'VC544 memory maps

Internal Address	External Physical Address A[0:14]	Prog Space
0000h	0000h(OVLY=0) or NO(OVLY=1)	External (OVLY=0) (see Note B) or Reserved (OVLY=1)
007Fh 0080h	007Fh(OVLY=0) or NO(OVLY=1) 0080h(OVLY=0) or NO(OVLY=1)	External (OVLY=0) (see Note B) or On-Chip RAM (OVLY=1) (4K words)
0FFFh 1000h	0FFFh(OVLY=0) or NO(OVLY=1) 1000h	External (see Note B)
1FFFh 2000h	1FFFh 2000h	External (24K words) Can be in same physical memory as data values since PS and DS signals are not present on '544 (see Note C)
7FFFh 8000h	7FFFh 0000h	External (8K words) Can be in same physical memory as data values since PS and DS signals are not present on '544 (see Note C)
9FFFh A000h	1FFFh NO (see Note A)	On-Chip ROM (24K words)
FF7Fh FF80h	NO NO	Interrupt Vector Table On-chip ROM
FFFFh	NO	

NOTES: A. This space is on-chip only. NO means no external access.

B. The space placed between 0000h and 1FFFh (when OVLY is off) or between 1000h and 1FFFh (when OVLY is on) addresses requires special attention. An access at this space is the same as an access at the image address in the 8000h–9FFFh (internal address) space. For example, access at 1000h is an access at internal 9000h (or in other words external 1000h).

C. It is the user's responsibility to make sure that data and program do not overlay in the same external physical addresses.

Figure 4. Memory Map – Program Space With MP/MC=0 ('LC544 and 'VC544)



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'LC544/'VC544 memory maps (continued)

Internal Address	External Physical Address A[0:14]	Prog Space
0000h	0000h(OVLY=0) or NO(OVLY=1)	External (OVLY=0) or Reserved (OVLY=1) (see Note A)
007Fh 0080h	007Fh(OVLY=0) or NO(OVLY=1) 0080h(OVLY=0) or NO(OVLY=1)	External (OVLY=0) (see Note A) or On-Chip RAM (OVLY=1) (4K words)
0FFFh 1000h	0FFFh(OVLY=0) or NO(OVLY=1) 1000h	External (28K words) (see Note A)
7FFFh 8000h	7FFFh 0000h	External (32K words) Can be in same physical memory as data values since \overline{PS} and \overline{DS} signals are not present on '544 (see Note B)
FF7Fh FF80h	7F7Fh 7F80h	Interrupt Vector Table External
FFFFh	7FFFh	

- NOTES: A. The space placed between 0000h and 7FFFh (when OVLY is off) or between 1000h and 7FFFh (when OVLY is on) addresses requires special attention. An access at this space is the same as an access at the image address in the 8000h–FFFFh (internal address) space.
- B. For example, access at 1000h the same as an access at internal 9000h (or, in other words, external 1000h).

Figure 5. Memory Map – Program Space With $\overline{MP}/\overline{MC}=1$ ('LC544 and 'VC544)

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'LC544/VC544 memory maps (continued)

Internal Address	External Physical Address A[0:14]	Data Space
0000h	NO (see Note D)	Memory-Mapped Registers
005Fh	NO	
0060h	NO	Scratch-Pad
007Fh	NO	
0080h	NO	
0FFFh	NO	On-Chip DARAM (4K words)
1000h	1000h	
		External (28K words) Can be in same physical memory as program values since PS and DS signals are not present on '544 (see Note B)
7FFFh	7FFFh	
8000h	0000h	External (4K words) Can be in same physical memory as program values since PS and DS signals are not present on '544 (see Note B)
8FFFh	0FFFh	External (see Note C)
9000h	1000h	
DFFFh	5FFFh	External (DROM=0) (see Note D)
E000h	6000h(DROM=0) or NO(DROM=1)	or On-Chip DROM (DROM=1)
FEFFh	7F00h(DROM=0) or NO(DROM=1)	External (DROM=0) (see Note D)
FF00h		or Reserved (DROM=1)
FFFFh		

- NOTES: A. This space is on-chip only. NO means no external access.
 B. It is the user's responsibility to make sure that data and program do not overlay in the same external physical addresses.
 C. The 20K words of space placed between 9000h and DFFFh internal addresses requires special attention. An access at this space is the same as an access at the image address in the 1000h–5FFFh space. For example, access at B000h (internal address) is an access at external 3000h.
 D. When DROM=0, the 8K words of space placed between E000h and FFFFh internal addresses requires special attention. An access at this space is the same as an access at the image address in the 6000h–7FFFh space.

Figure 6. Memory Map – Data Space ('LC544 and 'VC544)

The external memory space on the 'LC544 and 'VC544 device addresses up to 32K of 16-bit words through its external 15 line address bus A[0:14]. Since A15 line still is present in internal address buses, the internal address reach is 64K for both data and program spaces. Two types of addresses are defined in Figure 4, Figure 5, and Figure 6.

- internal address which appears on internal buses (PAB, CAB, DAB, EAB).
- external physical address which appears on the external A[0:14] bus.



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program memory

The external program memory space on the 'C54x/'LC54x/'VC54x devices addresses up to 64K 16-bit words. Software can configure their memory cells to reside inside or outside of the program address map. When the cells are mapped into program space, the device automatically accesses them when their addresses are within bounds. When the program-address generation (PAGEN) logic generates an address outside its bounds, the device automatically generates an external access. The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

program memory address map

The reset, interrupt, and trap vectors are addressed in program space. These vectors are soft — meaning that the processor, when taking the trap, loads the program counter (PC) with the trap address and executes the code at the vector location. Four words are reserved at each vector location to accommodate a delayed branch instruction, and either two 1-word instructions or one 2-word instruction, which allows branching to the appropriate interrupt service routine without the overhead.

At device reset, the reset, interrupt, and trap vectors are mapped to address FF80h in program space. However, these vectors can be remapped to the beginning of any 128-word page in program space after device reset. This is done by loading the interrupt vector pointer (IPTR) bits in the PMST register with the appropriate 128-word page boundary address. After loading IPTR, any user interrupt or trap vector is mapped to the new 128-word page. For example:

```
STM    #05800h, PMST    ; Remapped vectors to start at 5800h.
```

This example moves the interrupt vectors to off-chip program space at address 05800h. Any subsequent interrupt (except for a device reset) fetches its interrupt vector from that new location. For example, if, after loading the IPTR, an $\overline{\text{INT2}}$ occurs, the interrupt service routine vector is fetched from location 5848h in program space as opposed to location FFC8h. This feature facilitates moving the desired vectors out of the boot ROM and then removing the ROM from the memory map. Once the system code is booted into the system from the boot-loader code resident in ROM, the application reloads the IPTR with a value pointing to the new vectors. In the previous example, the STM instruction is used to modify the PMST. Note that the STM instruction modifies not only the IPTR but other status/control bits in the PMST register.

NOTE: The hardware reset ($\overline{\text{RS}}$) vector can not be remapped, because the hardware reset loads the IPTR with 1s. Therefore, the reset vector is always fetched at location FF80h in program space. In addition, for the 'C54x/'LC54x/'VC54x, 128 words are reserved in the on-chip ROM for device-testing purposes. Application code written to be implemented in on-chip ROM must reserve these 128 words at addresses FF00h–FF7Fh in program space.

data memory

The data memory space on the 'C54x/'LC54x/'VC54x device addresses contains up to 64K of 16-bit words. The 'C54x/'LC54x/'VC54x devices automatically access the on-chip RAM when addressing within its bounds. When an address is generated outside the RAM bounds, the device automatically generates an external access.

The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Higher performance because of better flow within the pipeline of the CALU
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.



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on-chip peripherals

All the 'C54x/'LC54x/'VC54x devices have the same CPU structure; however, they have different on-chip peripherals connected to their CPUs. The on-chip peripheral options provided are:

- Software-programmable wait-state generator
- Programmable bank switching
- Parallel I/O ports
- Serial ports
- A hardware timer
- A clock generator

software-programmable wait-state generator

Software-programmable wait-state generators can be used to extend external bus cycles up to seven machine cycles to interface with slower off-chip memory and I/O devices. The software wait-state generators are incorporated without any external hardware. For off-chip memory access, a number of wait states can be specified for every 32K-word block of program and data memory space, and for one 64K-word block of I/O space within the software wait-state (SWWSR) register.

programmable bank switching

Programmable bank switching can be used to insert one cycle automatically when crossing memory-bank boundaries inside program memory or data memory space. One cycle also can be inserted when crossing from program-memory space to data-memory space. This extra cycle allows memory devices to release the bus before other devices start driving the bus; thus avoiding bus contention. The size of memory bank for the bank switching is defined by the bank switching control register (BSCR).

parallel I/O ports

Each 'C54x/'LC54x/'VC54x device has a total of 64K-I/O ports. These ports can be addressed by the PORTR instruction or the PORTW instruction. The \overline{IS} signal indicates a read/write operation through an I/O port. The 'C54x/'LC54x/'VC54x devices can interface easily with external devices through the I/O ports while requiring minimal off-chip address decoding circuits.

host-port interface ('C542, 'LC542, 'VC542, 'LC545, and 'VC545 only)

The host-port interface is an 8-bit parallel port used to interface a host processor to the DSP device. Information is exchanged between the DSP device and the host processor through on-chip memory that is accessible by both the host and the DSP device. The DSP devices have access to the HPI control (HPIC) register and the host can address the HPI memory through the HPI address register (HPIA). HPI memory is a 2K 16-bit DARAM block which can also be used as general-purpose on-chip data or program DARAM.

Data transfers of 16-bit words occur as two consecutive bytes with a dedicated pin (HBIL) indicating whether the high or low byte is being transmitted. Two control pins, HCNTL1 and HCNTL0, control host access to the HPIA, HPI data (with an optional automatic address increment), or the HPIC. The host can interrupt the DSP device by writing to HPIC. The DSP device can interrupt the host with a dedicated \overline{HINT} pin that the host can acknowledge and clear.

The HPI has two modes of operation, shared-access mode (SAM) and host-only mode (HOM). In SAM, the normal mode of operation, both the DSP device and the host can access HPI memory. In this mode, asynchronous host accesses are resynchronized internally and, in case of conflict, the host has access priority and the DSP device waits one cycle. The HOM capability allows the host to access HPI memory while the DSP device is in IDLE2 (all internal clocks stopped) or in reset mode. The host can therefore access the HPI RAM while the DSP device is in its optimal configuration in terms of power consumption.



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host port interface ('C542, 'LC542, 'VC542, 'LC545, and 'VC545 only) (continued)

The HPI control register has two data strobes, $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$, a read/write strobe $\text{HR}/\overline{\text{W}}$, and an address strobe $\overline{\text{HAS}}$, to enable a glueless interface to a variety of industry-standard host devices. The HPI is interfaced easily to hosts with multiplexed address/data bus, separate address and data buses, one data strobe, and a read/write strobe, or two separate strobes for read and write.

The HPI supports high-speed back-to-back accesses. In the shared-access mode, it can handle one byte every five DSP device periods, that is, 64 Mb/s with a 40-MIPS DSP. The HPI is designed so that the host can take advantage of this high bandwidth and run at frequencies up to $(f \times n) + 5$, where n is the number of host cycles for an external access and f is the DSP device frequency. In host-only mode, the HPI supports even higher speed back-to-back host accesses: 1 byte every 50 ns, that is, 160 Mb/s, independently of the DSP device-clock rate.

serial ports

The 'C54x/'LC54x/'VC54x devices provide high-speed full-duplex serial ports that allow direct interface to other 'C54x/'LC54x/'VC54x devices, codecs, and other devices in a system. There is a general-purpose serial port, a time-division-multiplexed (TDM) serial port, and an auto-buffered serial port (BSP).

The general-purpose serial port utilizes two memory-mapped registers for data transfer: the data transmit register (DXR) and the data receive register (DRR). Both of these registers can be accessed in the same manner as any other memory location. The transmit and receive sections of the serial port each have associated clocks, frame-synchronization pulses, and serial-shift registers, and serial data can be transferred either in bytes or in 16-bit words. Serial port receive and transmit operations can generate their own maskable transmit and receive interrupts (XINT and RINT), allowing serial-port transfers to be managed through software. The 'C54x/'LC54x/'VC54x serial ports are double buffered and fully static.

The TDM port allows the device to communicate through time-division multiplexing with up to seven other 'C54x/'LC54x/'VC54x devices with TDM ports. Time-division multiplexing is the division of time intervals into a number of subintervals with each subinterval representing a prespecified communications channel. The TDM port serially transmits 16-bit words on a single data line (TDAT) and destination addresses on a single address line (TADD). Each device can transmit data on a single channel and receive data from one or more of the eight channels providing a simple and efficient interface for multiprocessing applications. A frame synchronization pulse occurs once every 128 clock cycles corresponding to transmission of one 16-bit word on each of the eight channels. Like the general-purpose serial port, the TDM port is double buffered on both input and output data. The TDM port can also be configured in software to operate as a general-purpose serial port as described above. Both types of ports described above are capable of operating at up to one-fourth the machine cycle rate (CLKOUT).

The buffered-serial port (BSP) consists of a full-duplex double-buffered serial-port interface (SPI) and an auto-buffering unit (ABU). The SPI block of the BSP is an enhanced version of the general-purpose serial port. The auto-buffering unit allows the SPI to read/write directly to 'C54x/'LC54x/'VC54x internal memory using a dedicated bus independently of the CPU. This results in minimal overhead for SPI transactions and faster data rates.

When auto-buffering capability is disabled (standard mode), transfers with SPI are performed under software control through interrupts. In this mode, the ABU is transparent and the word-based interrupts (WXINT and WRINT) provided by the SPI are sent to the CPU as transmit interrupt (XINT) and receive interrupt (RINT). When auto buffering is enabled, word transfers are done directly between the SPI and the 'C54x/'LC54x/'VC54x internal memory using ABU-embedded address generators.

serial ports (continued)

The ABU has its own set of circular-addressing registers with corresponding address-generation units. Memory for the buffers resides in 2K words of 'C54x/'LC54x/'VC54x internal memory. The length and starting addresses of the buffers are user programmable. A buffer-empty/-full interrupt can be posted to the CPU. Buffering is easily halted by an auto-disabling capability. Auto-buffering capability can be enabled separately for transmit and receive sections. When auto buffering is disabled, operation is similar to the general-purpose serial port.

The SPI allows transfer of 8-, 10-, 12-, or 16-bit data packets. In burst mode, data packets are directed by a frame synchronization pulse for every packet. In continuous mode, the frame synchronization pulse occurs when the data transmission is initiated and no further pulses occur. The frame and clock strobes are frequency and polarity programmable. The SPI is fully static and operates at arbitrarily low clock frequencies. The maximum operating frequency is CLKOUT (40 Mb/s at 25 ns).

Table 3 provides a comparison of the serial ports available in the 'C54x/'LC54x/'VC54x generation.

Table 3. Serial Port Configurations for the 'C54x/'LC54x/'VC54x

DEVICE	GENERAL-PURPOSE SERIAL PORT	BUFFERED SERIAL PORT	TDM SERIAL PORT
TMS320C541	2		
TMS320LC541	2		
TMS320VC541	2		
TMS320C542		1	1
TMS320LC542		1	1
TMS320VC542		1	1
TMS320LC543		1	1
TMS320VC543		1	1
TMS320LC544	2		
TMS320VC544	2		
TMS320LC545	1	1	
TMS320VC545	1	1	
TMS320LC546	1	1	
TMS320VC546	1	1	

hardware timer

The 'C54x/'LC54x/'VC54x devices feature a 16-bit timing circuit with a four-bit prescaler. The timer counter is decremented by one at every CLKOUT cycle. Each time the counter decrements to zero, a timer interrupt is generated. The timer can be stopped, restarted, reset, or disabled by specific status bits.

clock generator

The clock generator consists of an internal oscillator and a phase-locked loop (PLL) circuit. The clock generator can be driven internally by connecting a crystal resonator circuit, or driven by an external clock source. The PLL circuit can generate an internal CPU clock by multiplying the clock source frequency by a specific factor. Therefore, you can use a clock source with a lower frequency than that of the CPU.



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memory-mapped registers

All 'C54x/LC54x/VC54x devices have 26 memory-mapped CPU registers, which are mapped in data memory space address 0h to 1Fh. Each of these devices also has a set of memory-mapped registers associated with peripherals. Table 4 gives a list of CPU memory-mapped registers (MMR) common to all 'C54x/LC54x/VC54x devices. Table 5 shows additional peripheral MMRs associated with the 'C541/LC541/VC541/LC544/VC544 devices. Table 6 shows additional peripheral MMRs associated with the 'LC545/VC545/LC546/VC546 devices. Table 7 shows additional peripheral MMRs associated with the 'C542/LC542/VC542/LC543/VC543 devices.

Table 4. Core Processor Memory-Mapped Registers

NAME	ADDRESS		DESCRIPTION
	Dec	Hex	
IMR	0	0	Interrupt mask register
IFR	1	1	Interrupt flag register
–	2–5	2–5	Reserved for testing
ST0	6	6	Status register 0
ST1	7	7	Status register 1
AL	8	8	Accumulator A low word (15–0)
AH	9	9	Accumulator A high word (31–16)
AG	10	A	Accumulator A guard bits (39–32)
BL	11	B	Accumulator B low word (15–0)
BH	12	C	Accumulator B high word (31–16)
BG	13	D	Accumulator B guard bits (39–32)
TREG	14	E	Temporary register
TRN	15	F	Transition register
AR0	16	10	Auxiliary register 0
AR1	17	11	Auxiliary register 1
AR2	18	12	Auxiliary register 2
AR3	19	13	Auxiliary register 3
AR4	20	14	Auxiliary register 4
AR5	21	15	Auxiliary register 5
AR6	22	16	Auxiliary register 6
AR7	23	17	Auxiliary register 7
SP	24	18	Stack pointer register
BK	25	19	Circular buffer size register
BRC	26	1A	Block repeat Counter
RSA	27	1B	Block repeat start address
REA	28	1C	Block repeat end address
PMST	29	1D	Processor mode status (PMST) register
–	30–31	1E–1F	Reserved

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Table 5. Peripheral Memory-Mapped Registers ('C541, 'LC541, 'VC541, 'LC544 and 'VC544 Only)

NAME	ADDRESS		DESCRIPTION
	Dec	Hex	
DRR0	32	20	Serial port 0 data receive register
DXR0	33	21	Serial port 0 data transmit register
SPC0	34	22	Serial port 0 control register
—	35	23	Reserved
TIM	36	24	Timer register
PRD	37	25	Timer period register
TCR	38	26	Timer control register
—	39	27	Reserved
SWWSR	40	28	S/W wait-state register
BSCR	41	29	Bank switching control register
—	42–47	2A–2F	Reserved
DRR1	48	30	Serial port 1 data receive register
DXR1	49	31	Serial port 1 transmit register
SPC1	50	32	Serial port 1 control register
—	51	33	Reserved
—	52–95	34–5F	Reserved

Table 6. Peripheral Memory-Mapped Registers ('LC545, 'VC545, 'LC546 and 'VC546 Only)

NAME	ADDRESS		DESCRIPTION	TYPE
	Dec	Hex		
DRR	32	20	Data receive register	BSP
DXR	33	21	Data transmit register	BSP
SPC	34	22	Serial port control register	BSP
SPCE	35	23	BSP control extension register	BSP
TIM	36	24	Timer register	Timer
PRD	37	25	Timer period counter	Timer
TCR	38	26	Timer control register	Timer
—	39	27	Reserved	
SWWSR	40	28	S/W wait-state register	External bus
BSCR	41	29	Bank switching control register	External bus
—	42 – 43	2A – 2B	Reserved	
HPIC	44	2C	HPI control register	HPI†
—	45 – 47	2D – 2F	Reserved	
DRR1	48	30	Data receive register	Serial port
DXR1	49	31	Transmit register	Serial port
SPC1	50	32	Serial port control register	Serial port
—	51 – 55	33 – 37	Reserved	
AXR	56	38	ABU‡ transmit address register	BSP
BKX	57	39	ABU‡ transmit buffer size register	BSP
ARR	58	3A	ABU‡ receive address register	BSP
BKR	59	3B	ABU‡ receive buffer size register	BSP

† Host port interface (HPI) on 'LC545, 'VC545, only

‡ Auto-buffering unit (ABU)



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Table 7. Peripheral Memory-Mapped Registers ('C542, 'LC542, 'VC542, 'LC543 and 'VC543 Only)

NAME	ADDRESS		DESCRIPTION	TYPE
	Dec	Hex		
DRR	32	20	Data receive register	BSP
DXR	33	21	Data transmit register	BSP
SPC	34	22	Serial port control register	BSP
SPCE	35	23	BSP control extension register	BSP
TIM	36	24	Timer register	Timer
PRD	37	25	Timer period counter	Timer
TCR	38	26	Timer control register	Timer
—	39	27	Reserved	
SWWSR	40	28	S/W wait-state register	External bus
BSCR	41	29	Bank switching control register	External bus
—	42 – 43	2A – 2B	Reserved	
HPIC	44	2C	HPI control register	HPI†
—	45 – 47	2D – 2F	Reserved	
TRCV	48	30	Data receive register	TDM
TDXR	49	31	Transmit register	TDM
TSPC	50	32	Serial port control register	TDM
TCSR	51	33	Channel select register	TDM
TRTA	52	34	Receive/transmit register	TDM
TRAD	53	35	Receive address register	TDM
—	54 – 55	36 – 37	Reserved	
AXR	56	38	ABU‡ transmit address register	BSP
BKX	57	39	ABU‡ transmit buffer size register	BSP
ARR	58	3A	ABU‡ receive address register	BSP
BKR	59	3B	ABU‡ receive buffer size register	BSP

† Host port interface (HPI) on 'LC545, 'VC545, only

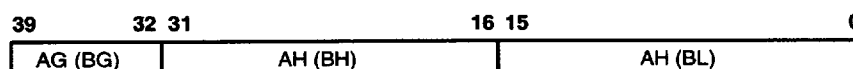
‡ Auto-buffering unit (ABU)

status register (ST0, ST1)

The status registers, ST0 and ST1, contain the status of the various conditions and modes for the 'C54x/'LC54x/'VC54x devices. ST0 contains the flags (OV, C, and TC) produced by arithmetic operations and bit manipulations in addition to the DP and the ARP fields. ST1 contains the various modes and instructions that the processor operates on and executes.

accumulators (AL, AH, AG, and BL, BH, BG)

The 'C54x/'LC54x/'VC54x devices have two 40-bit accumulators; accumulator A and accumulator B. Each accumulator is memory-mapped and partitioned into accumulator low word (AL, BL), accumulator high word (AH, BH), and accumulator guard bits (AG, BG).



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auxiliary registers (AR0–AR7)

The eight 16-bit auxiliary registers (AR0–AR7) can be accessed by the CALU and modified by the auxiliary register arithmetic units (ARAUs). The primary function of the auxiliary registers is generating 16-bit addresses for data space. However, these registers also can act as general-purpose registers or counters.

temporary register (TREG)

The TREG is used to hold one of the multiplicands for multiply and multiply/accumulate instructions. It can hold a dynamic (execution-time programmable) shift count for instructions with shift operation such as ADD, LD, and SUB instructions. It also can hold a dynamic bit address for the BITT instruction. The EXP instruction stores the exponent value computed onto the TREG, while the NORM instruction uses the TREG value to normalize the number. For ACS operation of Viterbi decoding, TREG holds branch metrics used by the DADST and DSADT instructions.

transition register (TRN)

The TRN is a 16-bit register that is used to hold the transition decision for the path to new metrics to perform the Viterbi algorithm. The CMPS (compare, select, max, and store) instruction updates the contents of the TRN based on the comparison between the accumulator high word and the accumulator low word.

stack-pointer register (SP)

The SP is a 16-bit register that contains the address at the top of the system. The SP always points to the last element pushed onto the stack. The stack is manipulated by interrupts, traps, calls, returns, and the PUSH, PSHM, POPD, and POPM instructions. Pushes and pops of the stack predecrement and postincrement, respectively, all 16 bits of the SP.

circular-buffer-size register (BK)

The 16-bit BK is used by the ARAUs in circular addressing to specify the data block size.

block repeat registers (BRC, RSA, REA)

The block-repeat counter (BRC) is a 16-bit register used to specify the number of times a block of code is to be repeated when performing a block repeat. The block-repeat start address (RSA) is a 16-bit register containing the starting address of the block of program memory to be repeated when operating in the repeat mode. The 16-bit block repeat-end address (REA) contains the ending address if the block of program memory is to be repeated when operating in the repeat mode.

interrupt registers (IMR, IFR)

The interrupt-mask register (IMR) is used to mask off specific interrupts individually at required times. The interrupt-flag register (IFR) indicates the current status of the interrupts.

processor mode status register (PMST)

The processor-mode status register (PMST) controls memory configurations of the 'C54x/LC54x/VC54x devices.



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electrical characteristics and operating conditions ('C541, 'C542)

absolute maximum ratings over specified temperature range (unless otherwise noted)[†]

Supply voltage range, V_{DD} ‡	–0.3 V to 7 V
Input voltage range	–0.3 V to 7 V
Output voltage range	–0.3 V to 7 V
Operating case temperature range, T_C	–40°C to 100°C
Storage temperature range, T_{stg}	–55°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to V_{SS} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	RS, INTn, NMI, CNT, CLKMDn X2/CLKIN		$V_{DD} + 0.3$	V
		All other inputs		$V_{DD} + 0.3$	
V_{IL}	Low-level input voltage	–0.3		0.8	V
I_{OH}	High-level output current			–300	μA
I_{OL}	Low-level output current			2	mA
T_C	Operating case temperature	–40		100	°C

Refer to Figure 7 for 5-V device test load circuit values.

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electrical characteristics and operating conditions ('C541, 'C542) (continued)

electrical characteristics over recommended operating case temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH}	High-level output voltage ‡	I _{OH} = –300 µA	2.4			V
V _{OL}	Low-level output voltage ‡	I _{OL} = 2 mA			0.6	V
I _{IZ}	Input current in high impedance	V _{DD} = 5.25 V, V _O = V _{SS} to V _{DD}	–20		20	µA
I _I	Input current (V _I = V _{SS} to V _{DD})	TRST	With internal pulldown	–10	800	µA
		TMS, TCK, TDI	With internal pullups	–500	10	
		D[15:0]	Bus holders enabled, V _{DD} = Nom, V _I = V _{IL} Max		75	
			Bus holders enabled, V _{DD} = Nom, V _I = V _{IH} Min	–75		
		All other input-only pins		–10	10	
I _{DDC}	Supply current, core CPU	V _{DD} = 5 V, f _x = 40 MHz, § T _A = 25°C		120¶		mA
I _{DDP}	Supply current, pins	V _{DD} = 5 V, f _x = 40 MHz, § T _A = 25°C				mA
I _{DD}	Supply current, standby	IDLE2	PLL x 1 mode, 40 MHz input	4		mA
		IDLE3		5		µA
C _I	Input capacitance			10		pF
C _O	Output capacitance			10		pF

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

‡ All input and output voltage levels except \overline{RS} , $\overline{INT0}$ – $\overline{INT3}$, \overline{NMI} , \overline{CNT} , X2/CLKIN, CLKMD0–CLKMD3 are TTL-compatible.

§ Clock mode: PLLx1 with external source

¶ This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.

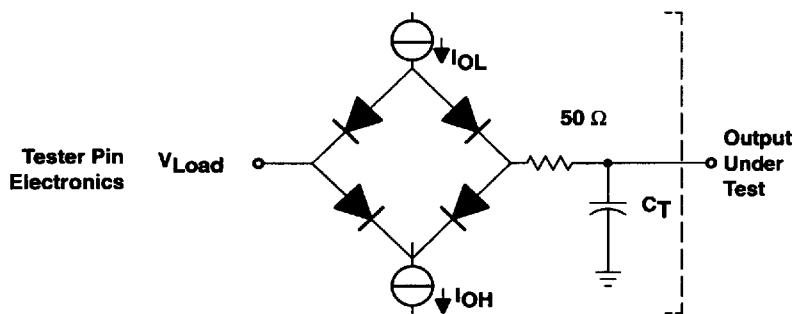
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Where: I_{OL} = 2 mA (all outputs)
 I_{OH} = 300 μ A (all outputs)
 V_{Load} = 1.5 V
 C_T = 40 pF typical load circuit capacitance.

Figure 7. 5-V Test Load Circuit

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows.

For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V. For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

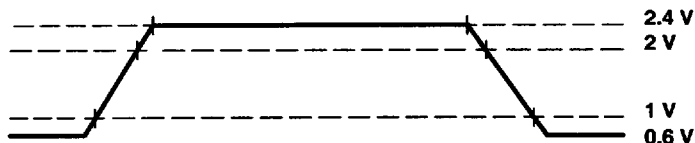


Figure 8. TTL-Level Outputs (5-V Devices)

Transition times for TTL-compatible inputs are specified as follows. For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.88 V and the level at which the input is said to be low is 0.92 V. For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.92 V and the level at which the input is said to be high is 1.88 V.

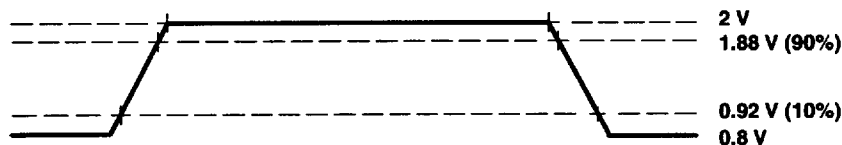


Figure 9. TTL-Level Inputs (5-V Devices)

electrical characteristics and operating conditions ('LC54x and 'VC54x only)

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} ‡	–0.3 V to 4.6 V
Input voltage range	–0.3 V to 4.6 V
Output voltage range	–0.3 V to 4.6 V
Operating case temperature range, T_C	–40°C to 100°C
Storage temperature range, T_{stg}	–55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltage values are with respect to V_{SS} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD} Supply voltage	'LC54x	3	3.3	3.6	V
	'VC54x	2.7	3.0	3.3	V
V_{SS} Supply voltage		0			V
V_{IH} High-level input voltage	RS, INTn, NMI, CNT, X2/CLKIN, CLKMDn, $V_{DD} = 3.3 \pm 0.3$ V	2.5		$V_{DD} + 0.3$	V
	RS, INTn, NMI, CNT, X2/CLKIN, CLKMDn, $V_{DD} = 2.7$ V	2.2		$V_{DD} + 0.3$	
	All other inputs	2		$V_{DD} + 0.3$	
V_{IL} Low-level input voltage		–0.3		0.8	V
I_{OH} High-level output current				–300	μ A
I_{OL} Low-level output current				+1.5	mA
T_C Operating case temperature		–40		100	°C

Refer to Figure 10 for 3.3-V and 2.7-V device test load circuit values.

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electrical characteristics and operating conditions ('LC54x and 'VC54x only) (continued)

electrical characteristics over recommended operating case temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VOH	High-level output voltage ‡	VDD = 3.3 ± 0.3 V, IOH = MAX	2.4			V
		VDD = 2.7 V, IOH = MAX	2.2			V
VOL	Low-level output voltage ‡	IOL = MAX			0.4	V
IIZ	Input current in high impedance	VDD = MAX, VO = VSS to VDD	–10		10	µA
II	Input current (VI = VSS to VDD)	TRST	With internal pulldown	–10	800	µA
		TMS, TCK, TDI	With internal pullups	–400	10	
		D[15:0]	Bus holders enabled, VDD = Nom, VI = VIL Max		75	
			Bus holders enabled, VDD = Nom, VI = VIH Min	–75		
		All other input-only pins		–10	10	
IDDC	Supply current, core CPU	VDD = 3.0 V, fX = 40 MHz,§ TA = 25°C		64¶		mA
IDDP	Supply current, pins	VDD = 3.0 V, fX = 40 MHz,§ TA = 25°C				mA
IDD	Supply current, standby	IDLE2	PLL x 1 mode, 40 MHz input	2		mA
		IDLE3		5		µA
Ci	Input capacitance			10		pF
Co	Output capacitance			10		pF

† All typical values are at VDD = 3.3 V, TA = 25°C.

‡ All input and output voltage levels except RS, INT0–INT3, NMI, CNT, X2/CLKIN, CLKMD0–CLKMD3 are LVTTTL-compatible.

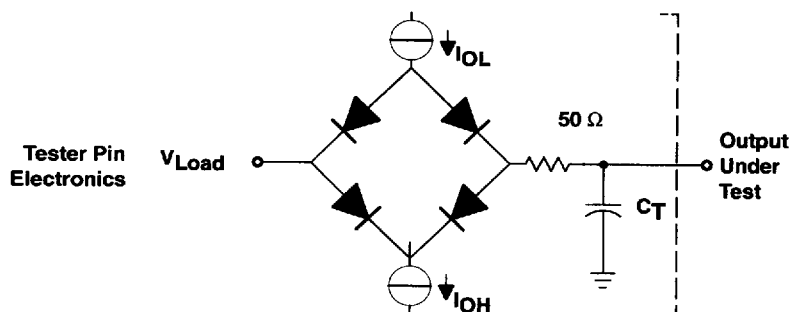
§ Clock mode: PLLx1 with external source

¶ This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.

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Where: I_{OL} = 1.5 mA (all outputs)
 I_{OH} = 300 μ A (all outputs)
 V_{Load} = 1.5 V
 C_T = 40 pF typical load circuit capacitance.

Figure 10. 3.3-V/2.7-V Test Load Circuit

signal transition levels

LVTTL-level outputs are driven to a minimum logic-high level of 2.4/2.2 V ('LC54x/'VC54x) and to a maximum logic-low level of 0.4 V. Output transition times are specified as follows.

For a high-to-low transition on a LVTTL-compatible output signal, the level at which the output is said to be no longer high is 2 V ('LC device) or 1.8 V ('VC device), and the level at which the output is said to be low is 0.8 V. For a low-to-high transition, the level at which the output is said to be no longer low is 0.8 V, and the level at which the output is said to be high is 2 V ('LC device) or 1.8 V ('VC device).

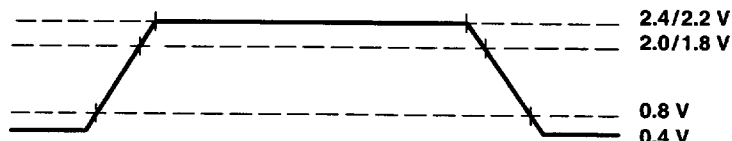


Figure 11. TTL-Level Outputs (3.3-V/2.7-V Devices)

LVTTL-compatible input transitions are specified as follows. For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.88 V and the level at which the input is said to be low is 0.92 V. For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.92 V and the level at which the input is said to be high is 1.88 V.

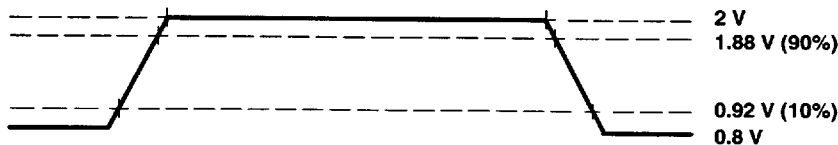


Figure 12. TTL-Level Inputs (3.3-V/2.7-V Devices)

CLOCK CHARACTERISTICS AND TIMING

The 'C54x, 'LC54x and 'VC54x can use either an internal oscillator or an external frequency source for a clock. The clock mode is determined by the CLKMD1, CLKMD2 and CLKMD3 clock mode pins. Table 8 outlines the selection of the clock mode by these pins.

Table 8. Clock Mode Configurations

MODE-SELECT PINS			CLOCK MODE	
CLKMD1	CLKMD2	CLKMD3	OPTION [†]	OPTION 2 [†]
0	0	0	PLL × 3 with external source	PLL × 5 with external source
1	1	0	PLL × 2 with external source	PLL × 4 with external source
1	0	0	PLL × 3 with internal source	PLL × 5 with internal source
0	1	0	PLL × 1.5 with external source	PLL × 4.5 with external source
0	0	1	Divide-by-two with external source	Divide-by-two with external source
0	1	1	Stop mode [‡]	Stop mode [‡]
1	0	1	PLL × 1 with external source	PLL × 1 with external source
1	1	1	Divide-by-two with internal source	Divide-by-two with internal source

[†] Option: Option 1 or option 2 can be selected when ordering the device.

[‡] Stop mode: The function of the stop mode is equivalent to that of the power-down mode of IDLE3. The IDLE3 instruction is recommended, rather than the stop mode, to realize full power saving.

internal divide-by-two clock option with external crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT is one-half the crystal's oscillating frequency. The crystal should be either fundamental or overtone operation, and parallel resonant, with an effective series resistance of 30 Ω and power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF.

recommended operating conditions

	'C54x-40 'LC54x-40/'VC54x-40			'LC54x-50 'VC54x-50			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
f _x Input clock frequency	0 [§]		80	0 [§]		100	MHz
C1, C2		10			10		pF

[§] This device utilizes a fully static design and therefore can operate with t_c(C1) approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 3.3 MHz to meet device test time requirement.

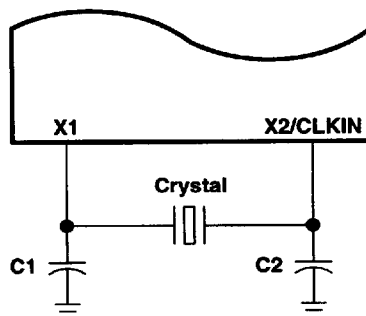


Figure 13. Internal Clock Option

external divide-by-two clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected, CLKMD1 and CLKMD2 set low, and CLKMD3 set high. This external frequency is divided by two to generate the internal machine cycle.

The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [$H = 0.5t_{c(CO)}$]

PARAMETER	'C54x-40 'LC54x-40/'VC54x-40			'LC54x-50 'VC54x-50			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
$t_{c(CO)}$ Cycle time, CLKOUT	25	$2t_{c(CI)}$	†	20	$2t_{c(CI)}$	†	ns
$t_{d(CIH-CO)}$ Delay time, X2/CLKIN high to CLKOUT high/low	6	12	18	6	12	18	ns
$t_f(CO)$ Fall time, CLKOUT	2			2			ns
$t_r(CO)$ Rise time, CLKOUT	2			2			ns
$t_w(COL)$ Pulse duration, CLKOUT low	H-4	H-2	H	H-4	H-2	H	ns
$t_w(COH)$ Pulse duration, CLKOUT high	H-4	H-2	H	H-4	H-2	H	ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞ . The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 3.35 MHz to meet device test time requirements.

timing requirements over recommended operating conditions

	'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
	MIN	MAX	MIN	MAX	UNIT
$t_{c(CI)}$ Cycle time, X2/CLKIN	12.5	‡	10	‡	ns
$t_f(CI)$ Fall time, X2/CLKIN §	4		4		ns
$t_r(CI)$ Rise time, X2/CLKIN §	4		4		ns
$t_w(CIL)$ Pulse duration, X2/CLKIN low	3	‡	3	‡	ns
$t_w(CIH)$ Pulse duration, X2/CLKIN high	3	‡	3	‡	ns

‡ This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞ . The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 6.7 MHz to meet device test time requirements.

§ Values derived from characterization data and not tested.

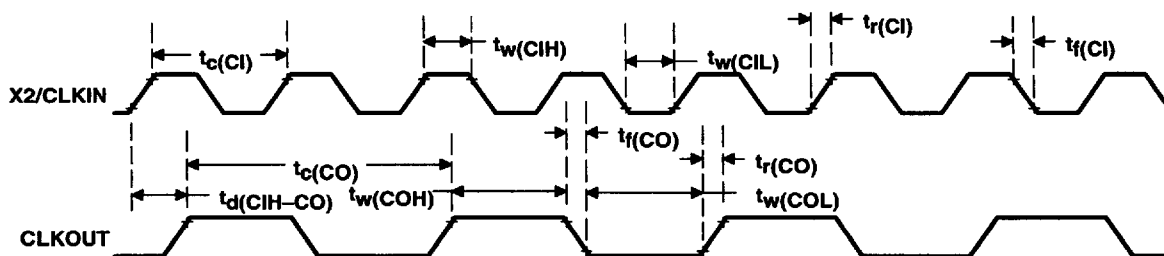


Figure 14. External Divide-by-Two Clock Timing



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external multiply-by-N clock option

An external frequency can be used by injecting the frequency directly into X2/CLKIN, with X1 left unconnected, CLKMD1, CLKMD2, and CLKMD3 set according to the clock mode configuration table (Table 8). This external frequency is multiplied by N to generate the internal machine cycle.

The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [$H = 0.5t_{c(CO)}$]

PARAMETER			'C54x-40 'LC54x-40/'VC54x-40			'LC54x-50 'VC54x-50			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT		25	$t_{c(CI)}/N$		20	$t_{c(CI)}/N$		ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN low to CLKOUT high	$N=1, 2, 3, 4, 5, 9$	6	12	18	6	12	18	ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN high to CLKOUT high/low	$N=1.5, 2.5, 4.5$	6	12	18	6	12	18	ns
$t_f(CO)$	Fall time, CLKOUT		2			2			ns
$t_r(CO)$	Rise time, CLKOUT		2			2			ns
$t_w(COL)$	Pulse duration, CLKOUT low		H-4	H-2	H	H-4	H-2	H	ns
$t_w(COH)$	Pulse duration, CLKOUT high		H-4	H-2	H	H-4	H-2	H	ns
t_p	PLL lock-up time		50†			50†			μs

† Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

			'C54x-40 'LC54x-40/'VC54x-40		'LC54x-50 'VC54x-50		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, X2/CLKIN	$N=1, 2, 3, 4, 5, 9$	25N	200N	20N	200N	ns
		$N=1.5, 2.5, 4.5$	25N	100N	20N	100N	
$t_f(CI)$	Fall time, X2/CLKIN †		4		4		ns
$t_r(CI)$	Rise time, X2/CLKIN †		4		4		ns
$t_w(CIL)$	Pulse duration, X2/CLKIN low		8		6		ns
$t_w(CIH)$	Pulse duration, X2/CLKIN high		8		6		ns

† Values derived from characterization data and not tested.

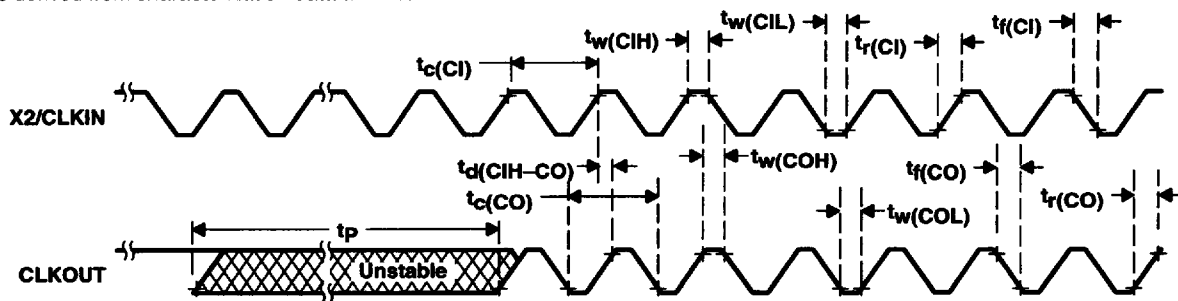


Figure 15. External Multiply-by-One Clock Timing



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memory and parallel I/O interface timing

timing parameters for a memory ($\overline{\text{MSTRB}} = 0$) read [$H = 0.5 t_{c(CO)}$]^{†‡} (see Figure 16)

		'LC542-40 'VC54x-40 'LC543-40		'C54x-40 'LC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)M}$	Access time, read data access from address valid		2H-12		2H-10		2H-10	ns
$t_{a(MSTRBL)}$	Access time, read data access from MSTRB low		2H-12		2H-10		2H-10	ns
$t_{su(D)R}$	Setup time, read data before CLKOUT low	7		5		5		ns
$t_d(CLKL-A)$	Delay time, address valid from CLKOUT low [§]	0 [¶]	5	0 [¶]	5	0 [¶]	5	ns
$t_d(CLKH-A)$	Delay time, address valid from CLKOUT high (transition) [#]	0 [¶]	5	0 [¶]	5	0 [¶]	5	ns
$t_d(CLKL-MSL)$	Delay time, $\overline{\text{MSTRB}}$ low from CLKOUT low	0	5	0	5	0	5	ns
$t_d(CLKL-MSH)$	Delay time, $\overline{\text{MSTRB}}$ high from CLKOUT low	-2	3	-2	3	-2	3	ns
$t_h(CLKL-A)R$	Hold time, address valid after CLKOUT low	0	5 [¶]	0	5 [¶]	0	5 [¶]	ns
$t_h(CLKH-A)R$	Hold time, address valid after CLKOUT high	0	5 [¶]	0	5 [¶]	0	5 [¶]	ns
$t_h(D)R$	Hold time, read data time after CLKOUT low	0		0		0		ns
$t_h(A-D)R$	Hold time, read data after address invalid	0		0		0		ns

[†] A15-A0, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.

[‡] See Figure 20 for address bus timing variation with load capacitance.

[§] In the case of a memory read preceded by a memory read

[¶] Values derived from characterization data and not tested

[#] In the case of a memory read preceded by a memory write

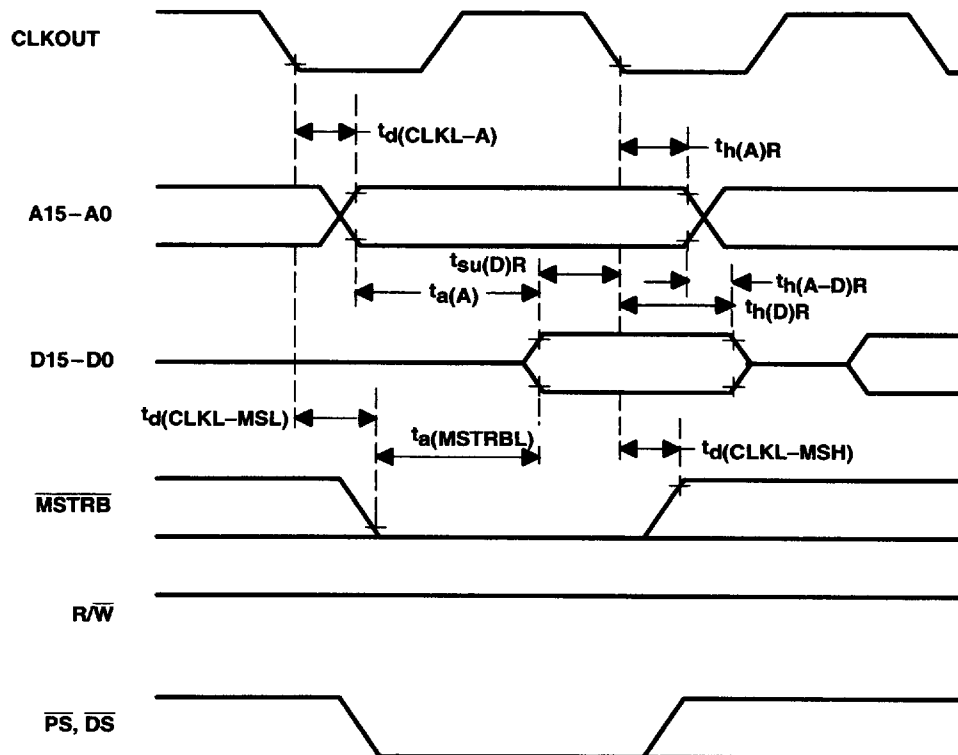


Figure 16. Memory Read ($\overline{\text{MSTRB}} = 0$)



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memory and parallel I/O interface timing (continued)

timing parameters for a memory ($\overline{\text{MSTRB}} = 0$) write [$H = 0.5 t_{c(CO)}$]^{†‡} (see Figure 17)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_d(\text{CLKH-A})$	Delay time, address valid from CLKOUT high [§]	0 [¶]	5	0 [¶]	5	ns
$t_d(\text{CLKL-A})$	Delay time, address valid from CLKOUT low (transition) [#]	0 [¶]	5	0 [¶]	5	ns
$t_d(\text{CLKL-MSL})$	Delay time, $\overline{\text{MSTRB}}$ low from CLKOUT low	0	5	0	5	ns
$t_d(\text{CLKL-D})W$	Delay time, data valid from CLKOUT low		10		10	ns
$t_d(\text{CLKL-MSH})$	Delay time, $\overline{\text{MSTRB}}$ high from CLKOUT low	-2	3	-2	3	ns
$t_d(\text{CLKH-RWL})$	Delay time, R/W low from CLKOUT high	0	5	0	5	ns
$t_d(\text{CLKH-RWH})$	Delay time, R/W high from CLKOUT high	-2	3	-2	3	ns
$t_h(\text{A})W$	Hold time, address valid after CLKOUT high	0	5 [¶]	0	5 [¶]	ns
$t_h(\text{D})MSH$	Hold time, write data valid after $\overline{\text{MSTRB}}$ high	H-5	H+5 [¶]	H-5	H+5 [¶]	ns
$t_w(\text{SL})MS$	Pulse duration, $\overline{\text{MSTRB}}$ low	2H-5		2H-5		ns
$t_{su}(\text{A})W$	Setup time, address valid before $\overline{\text{MSTRB}}$ low	2H-5		2H-5		ns
$t_{su}(\text{D})MSH$	Setup time, write data valid before $\overline{\text{MSTRB}}$ high	2H-10	2H+10 [¶]	2H-10	2H+10 [¶]	ns

[†] A15-A0, $\overline{\text{PS}}$, $\overline{\text{DS}}$ timings are all included in timings referenced as address.

[‡] See Figure 20 for address bus timing variation with load capacitance.

[§] In the case of a memory write preceded by a memory write.

[¶] In the case of a memory write preceded by an I/O write.

[#] Values derived from characterization data and not tested

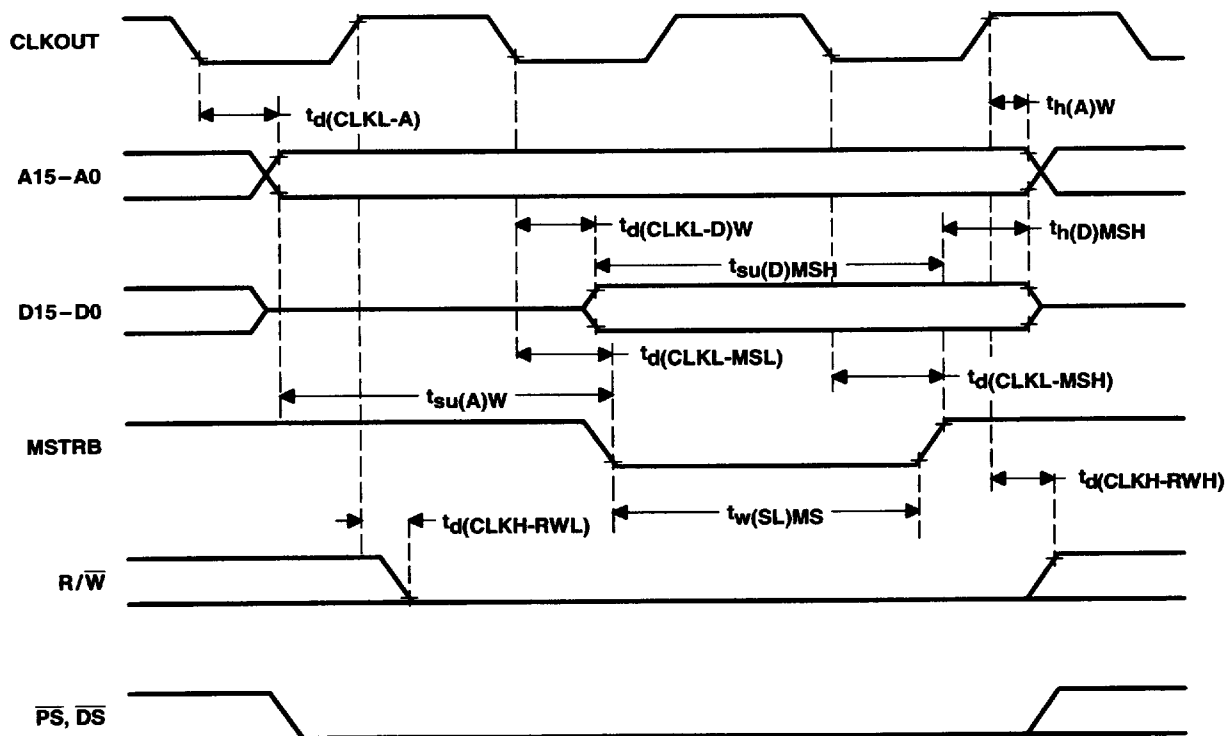


Figure 17. Memory Write ($\overline{\text{MSTRB}} = 0$)



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memory and parallel I/O interface timing (continued)

timing parameters for a parallel I/O port ($\overline{\text{IOSTRB}} = 0$) read [$H = 0.5 t_{c(CO)}$]^{†‡} (see Figure 18)

		'LC542-40 'VC54x-40 'LC543-40	'C54x-40 'LC54x-40	'LC54x-50 'VC54x-50	UNIT
		MIN	MAX	MIN	
$t_{a(A)IO}$	Access time, read data access from address valid		3H–12	3H–10	ns
$t_{a(ISTRBL)IO}$	Access time, read data access from $\overline{\text{IOSTRB}}$ low		3H–12	3H–10	
$t_{su(D)IOR}$	Setup time, read data before CLKOUT high	7		5	
$t_d(CLKL-A)$	Delay time, address valid from CLKOUT low	0§	5	0§	
$t_d(CLKH-ISTRBL)$	Delay time, $\overline{\text{IOSTRB}}$ low from CLKOUT high	0	5	0	
$t_d(CLKH-ISTRBH)$	Delay time, $\overline{\text{IOSTRB}}$ high from CLKOUT high	–2	3	–2	
$t_h(A)IOR$	Hold time, address after CLKOUT low	0	5§	0	
$t_h(D)IOR$	Hold time, read data after CLKOUT high	0		0	
$t_h(ISTRBH-D)R$	Hold time, read data after $\overline{\text{IOSTRB}}$ high	0		0	

[†] A15–A0 and $\overline{\text{IS}}$ timings are included in timings referenced as address.

[‡] See Figure 20 for address bus timing variation with load capacitance.

§ Values derived from characterization data and not tested

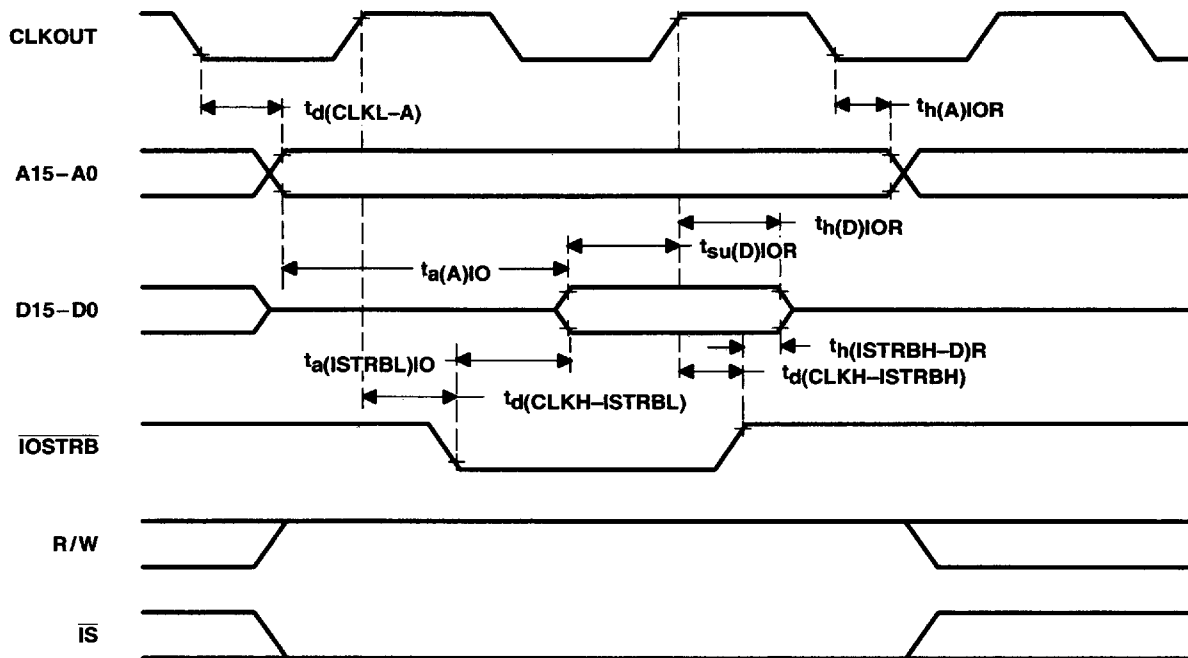


Figure 18. Parallel I/O Port Read ($\overline{\text{IOSTRB}} = 0$)



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memory and parallel I/O interface timing (continued)

timing parameters for a parallel I/O port ($\overline{\text{IOSTRB}} = 0$) write [$H = 0.5 t_{c(CO)}$] (see Figure 19)[†]

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_d(\text{CLKL-A})$	Delay time, address valid from CLKOUT low [‡]	0§	5	0§	5	ns
$t_d(\text{CLKH-ISTRBL})$	Delay time, $\overline{\text{IOSTRB}}$ low from CLKOUT high	0	5	0	5	ns
$t_d(\text{CLKH-D})_{\text{IOW}}$	Delay time, write data valid from CLKOUT high	H-5§	H+10	H-5§	H+10	ns
$t_d(\text{CLKH-ISTRBH})$	Delay time, $\overline{\text{IOSTRB}}$ high from CLKOUT high	-2	3	-2	3	ns
$t_d(\text{CLKL-RWL})$	Delay time, R/W low from CLKOUT low	0	5	0	5	ns
$t_d(\text{CLKL-RWH})$	Delay time, R/W high from CLKOUT low	-2	3	-2	3	ns
$t_h(\text{A})_{\text{IOW}}$	Hold time, address valid from CLKOUT low [‡]	0	5§	0	5§	ns
$t_h(\text{D})_{\text{IOW}}$	Hold time, write data after $\overline{\text{IOSTRB}}$ high	H-5	H+5§	H-5	H+5§	ns

[†] See Figure 20 for address bus timing variation with load capacitance.

[‡] A15-A0, and $\overline{\text{IS}}$ timings are included in timings referenced as address.

§ Values derived from characterization data and not tested

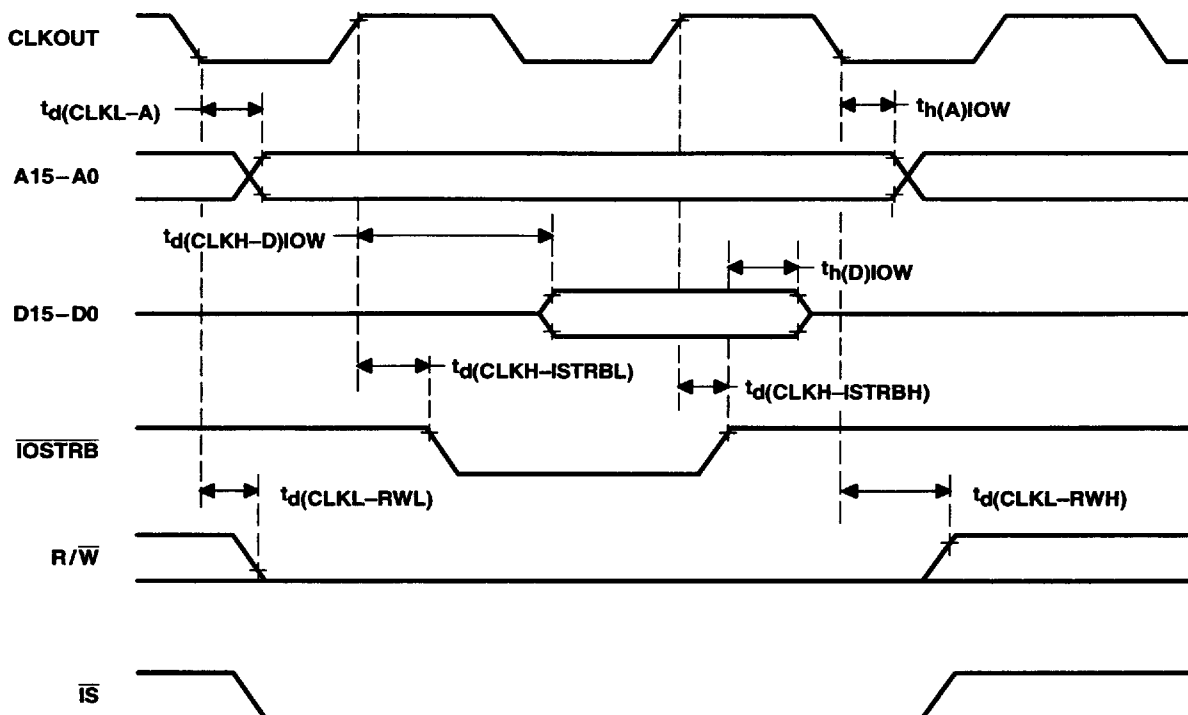


Figure 19. Parallel I/O Port Write ($\overline{\text{IOSTRB}} = 0$)



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memory and parallel I/O interface timing (continued)

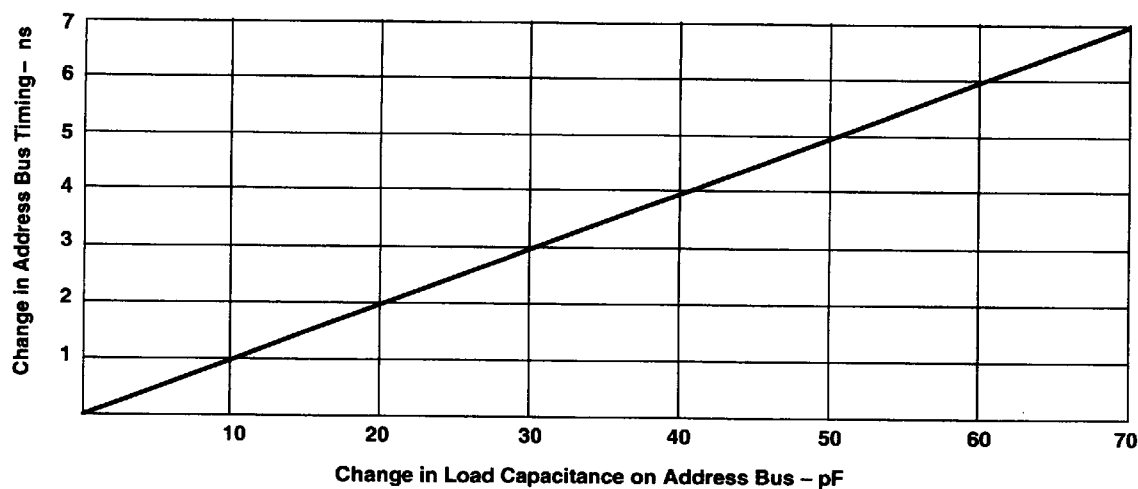


Figure 20. Address Bus Timing Variation with Load Capacitance

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ready timing for externally generated wait states

timing parameters for externally generated wait states [$H = 0.5 t_{c(CO)}$][†]

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{su}(RDY)$	Setup time, READY before CLKOUT low	10		8		ns
$t_h(RDY)$	Hold time, READY after CLKOUT low	0		0		ns
$t_v(RDY)MSTRB$	Valid time, READY after MSTRB low	4H–15		4H–15		ns
$t_h(RDY)MSTRB$	Hold time, READY after MSTRB low	4H		4H		ns
$t_v(RDY)IOSTRB$	Valid time, READY after IOSTRB low	5H–15		5H–15		ns
$t_h(RDY)IOSTRB$	Hold time, READY after IOSTRB low	5H		5H		ns
$t_v(MSCL)$	Valid time, \overline{MSC} low after CLKOUT low	0	5	0	5	ns
$t_v(MSCH)$	Valid time, \overline{MSC} high after CLKOUT low	–2	3	–2	3	ns

[†] The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the software wait states.

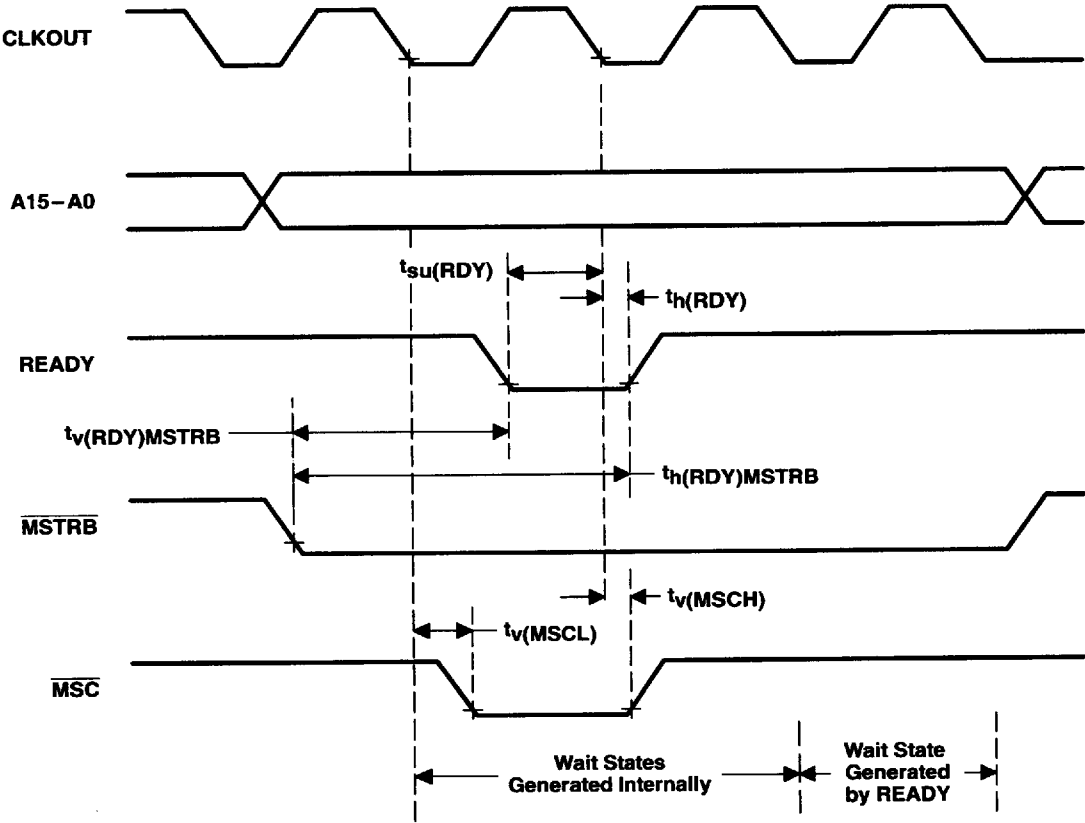


Figure 21. Memory Read With Externally Generated Wait States

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ready timing for externally generated wait states (continued)

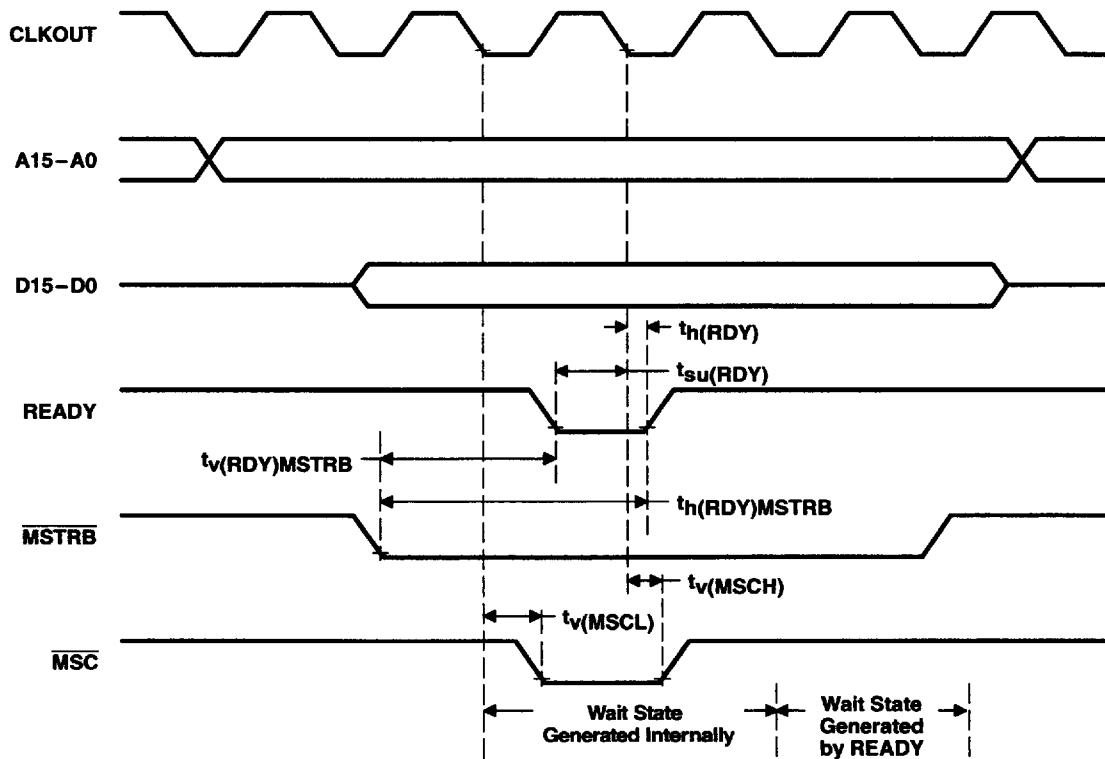


Figure 22. Memory Write With Externally Generated Wait States

ready timing for externally generated wait states (continued)

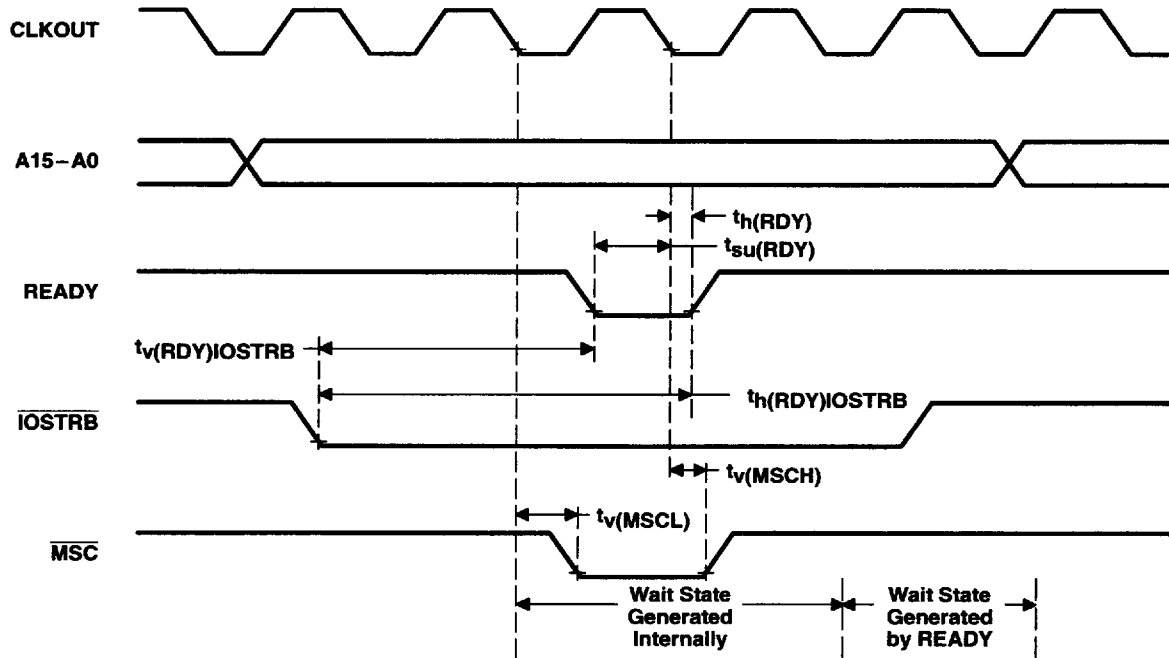


Figure 23. I/O Read With Externally Generated Wait States

ready timing for externally generated wait states (continued)

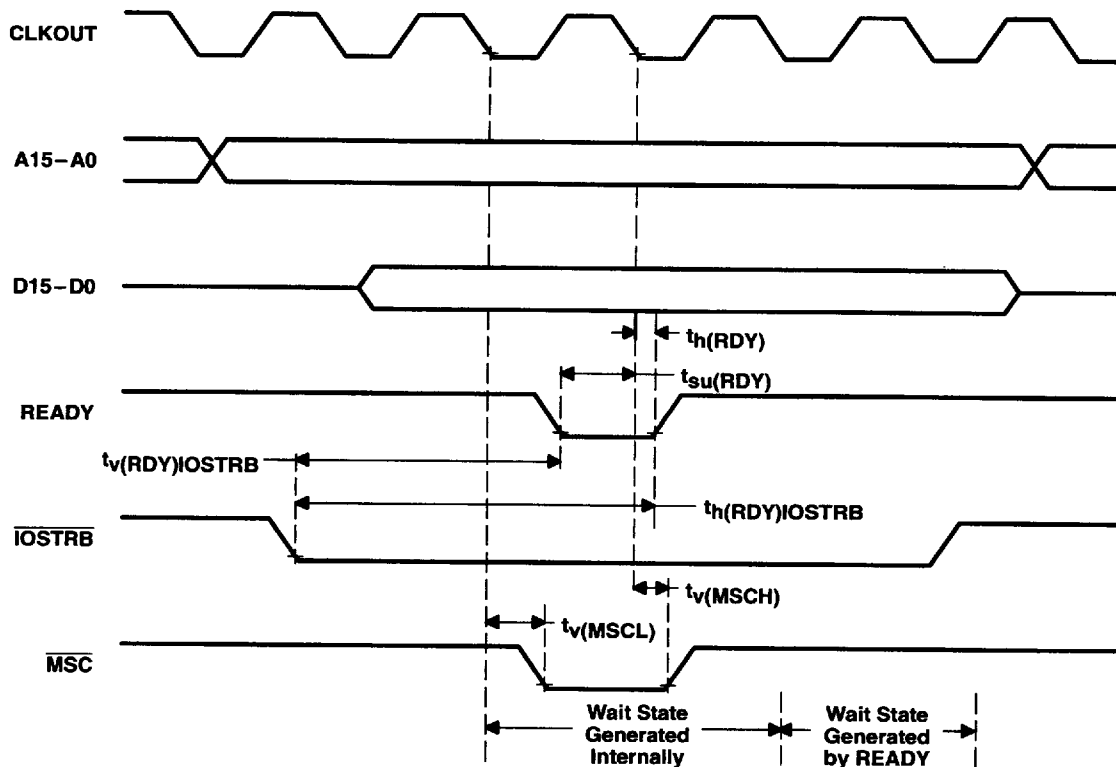


Figure 24. I/O Write With Externally Generated Wait States

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HOLD and HOLDA Timing

timing parameters for $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ [$H = 0.5 t_{c(CO)}$]

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{dis}(\text{CLKL-A})$	Disable time, CLKOUT low to address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$		5 [†]		5 [†]	ns
$t_{dis}(\text{CLKL-RW})$	Disable time, CLKOUT low to $\overline{\text{R/W}}$		5 [†]		5 [†]	ns
$t_{dis}(\text{CLKL-S})$	Disable time, CLKOUT low to $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$		5 [†]		5 [†]	ns
$t_{en}(\text{CLKL-A})$	Enable time, CLKOUT low to address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$		2H + 5		2H + 5	ns
$t_{en}(\text{CLKL-RW})$	Enable time, CLKOUT low to $\overline{\text{R/W}}$ enabled		2H + 5		2H + 5	ns
$t_{en}(\text{CLKL-S})$	Enable time, CLKOUT low to $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ enabled		2H + 5		2H + 5	ns
$t_w(\text{HOLD})$	Pulse duration, $\overline{\text{HOLD}}$ low duration	4H + 10		4H + 10		ns
$t_w(\text{HOLDA})$	Pulse duration, $\overline{\text{HOLDA}}$ low duration	2H + 10		2H + 10		ns
$t_{su}(\text{HOLD})$	Setup time, $\overline{\text{HOLD}}$ before CLKOUT low	10		10		ns
$t_v(\text{HOLDA})$	Valid time, $\overline{\text{HOLDA}}$ after CLKOUT low	-2	5	-2	5	ns

[†] Values derived from characterization data and not tested.

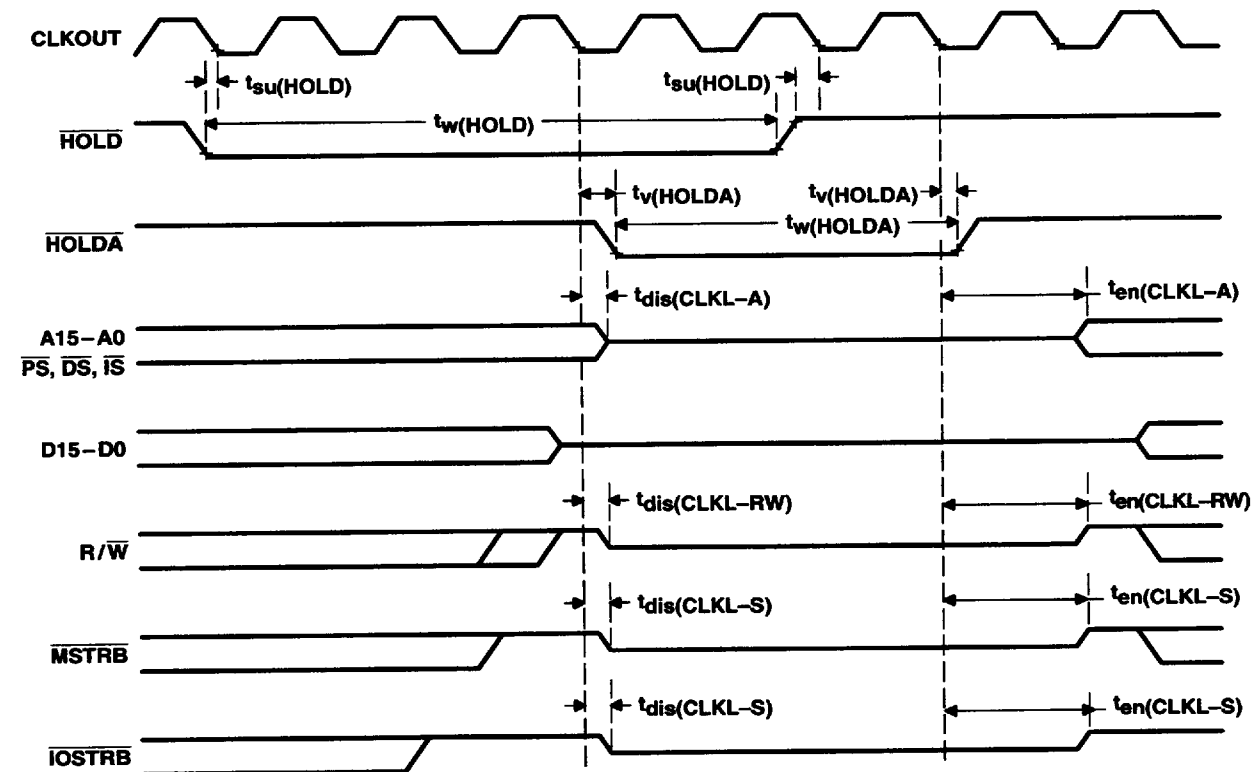


Figure 25. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing ($H = 1$)



reset, interrupt, $\overline{\text{BIO}}$, and $\text{MP}/\overline{\text{MC}}$ timings

timing parameters for reset, interrupt, $\overline{\text{BIO}}$, and $\text{MP}/\overline{\text{MC}}$ [$H = 0.5 t_{\text{c}}(\text{CO})$]

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{\text{h}}(\text{RS})$	Hold time, $\overline{\text{RS}}$ after CLKOUT low	0		0		ns
$t_{\text{h}}(\text{BIO})$	Hold time, $\overline{\text{BIO}}$ after CLKOUT low	0		0		ns
$t_{\text{h}}(\text{INT})$	Hold time, $\overline{\text{INT}}_n$, $\overline{\text{NMI}}$, after CLKOUT low [†]	0		0		ns
$t_{\text{h}}(\text{MPMC})$	Hold time, $\text{MP}/\overline{\text{MC}}$ after CLKOUT low [‡]	0		0		ns
$t_{\text{w}}(\text{RSL})$	Pulse duration, $\overline{\text{RS}}$ low [§] ¶	4H+10		4H+10		ns
$t_{\text{w}}(\text{BIO})_{\text{S}}$	Pulse duration, $\overline{\text{BIO}}$ low, synchronous	2H+15		2H+12		ns
$t_{\text{w}}(\text{BIO})_{\text{A}}$	Pulse duration, $\overline{\text{BIO}}$ low, asynchronous¶	4H		4H		ns
$t_{\text{w}}(\text{INTH})$	Pulse duration, $\overline{\text{INT}}_n$, $\overline{\text{NMI}}$ high					ns
$t_{\text{w}}(\text{INTL})_{\text{S}}$	Pulse duration, $\overline{\text{INT}}_n$, $\overline{\text{NMI}}$ low (synchronous)	2H+15		2H+12		ns
$t_{\text{w}}(\text{INTL})_{\text{A}}$	Pulse duration, $\overline{\text{INT}}_n$, $\overline{\text{NMI}}$ low (asynchronous)¶	4H		4H		ns
$t_{\text{w}}(\text{INTL})_{\text{WKP}}$	Pulse duration, $\overline{\text{INT}}_n$, $\overline{\text{NMI}}$ low for IDLE2/IDLE3 wakeup [‡]	10		10		ns
$t_{\text{su}}(\text{RS})$	Setup time, $\overline{\text{RS}}$ before X2/CLKIN low [#]	5		5		ns
$t_{\text{su}}(\text{BIO})$	Setup time, $\overline{\text{BIO}}$ before CLKOUT low	15		12		ns
$t_{\text{su}}(\text{INT})$	Setup time, $\overline{\text{INT}}_n$, $\overline{\text{NMI}}$, $\overline{\text{RS}}$ before CLKOUT low	15		12		ns
$t_{\text{su}}(\text{MPMC})$	Setup time, $\text{MP}/\overline{\text{MC}}$ before CLKOUT low [‡]	10		10		ns

[†] The external interrupts ($\overline{\text{INT}}_0$ – $\overline{\text{INT}}_3$, $\overline{\text{NMI}}$) are synchronized to the core CPU via a two flip-flop synchronizer which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1–0–0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.

[‡] Values ensured by design but not tested.

[§] If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{\text{RS}}$ must be held low for at least 50 μs to assure synchronization and lock-in of the PLL.

¶ Values derived from characterization data and not tested.

[#] Divide-by-two mode

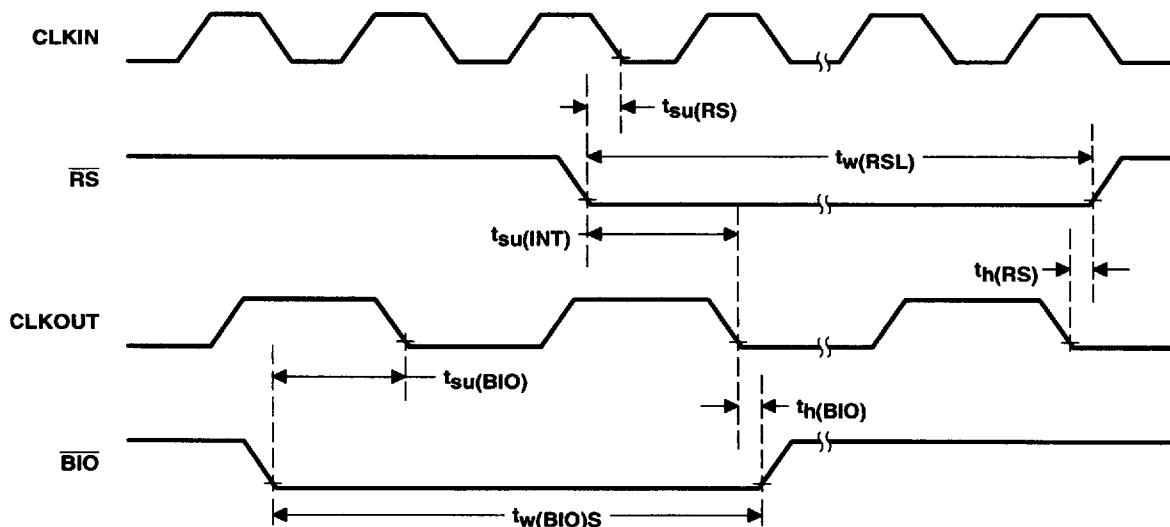


Figure 26. Reset and $\overline{\text{BIO}}$ Timings



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reset, interrupt, $\overline{\text{BIO}}$, and $\text{MP}/\overline{\text{MC}}$ timings (continued)

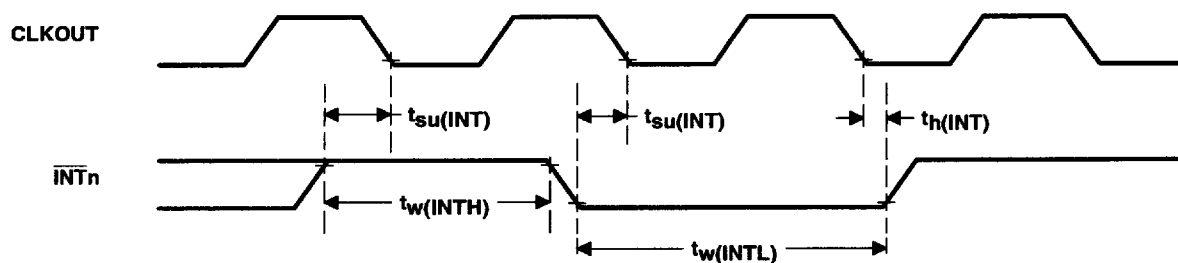


Figure 27. Interrupt Timing

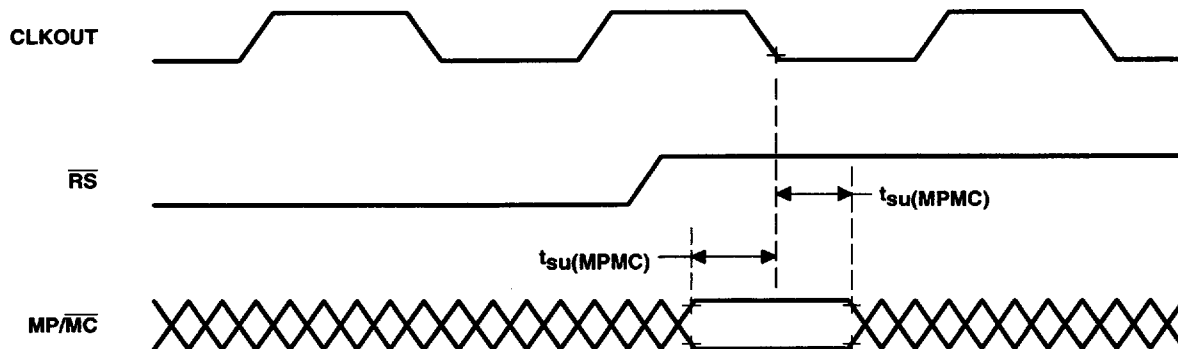


Figure 28. $\text{MP}/\overline{\text{MC}}$ Timing

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instruction acquisition ($\overline{\text{IAQ}}$), interrupt acknowledge ($\overline{\text{IACK}}$), external flag (XF), and TOUT timing
timing parameters for $\overline{\text{IAQ}}$ and $\overline{\text{IACK}}$ ($H = 0.5 t_{c(CO)}$) (see Figure 29)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_d(\text{CLKL-IAQL})$	Delay time, $\overline{\text{IAQ}}$ valid from CLKOUT low	0	5	0	5	ns
$t_d(\text{CLKL-IAQH})$	Delay time, $\overline{\text{IAQ}}$ high from CLKOUT low	-2	3	-2	3	ns
$t_d(\text{A})\text{IAQ}$	Delay time, address valid after $\overline{\text{IAQ}}$ low		5		5	ns
$t_d(\text{CLKL-IACKL})$	Delay time, $\overline{\text{IACK}}$ valid from CLKOUT low	0	5	0	5	ns
$t_d(\text{CLKL-IACKH})$	Delay time, $\overline{\text{IACK}}$ high from CLKOUT low	-2	3	-2	3	ns
$t_d(\text{A})\text{IACK}$	Delay time, address valid after $\overline{\text{IACK}}$ low		5		5	ns
$t_h(\text{A})\text{IAQ}$	Hold time, address valid after $\overline{\text{IAQ}}$ high	0		0		ns
$t_h(\text{A})\text{IACK}$	Hold time, address valid after $\overline{\text{IACK}}$ high	0		0		ns
$t_w(\text{IAQL})$	Pulse duration, $\overline{\text{IAQ}}$ low	2H-10		2H-10		ns
$t_w(\text{IACKL})$	Pulse duration, $\overline{\text{IACK}}$ low	2H-10		2H-10		ns

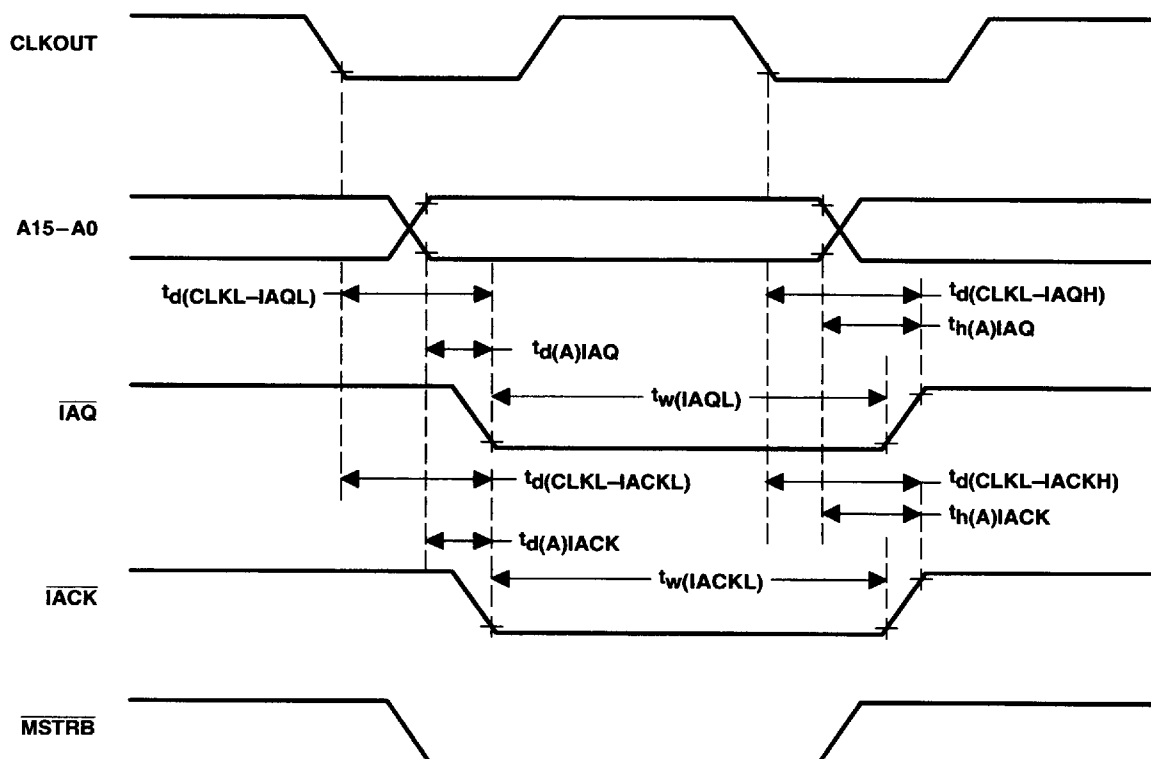


Figure 29. Instruction Acquisition ($\overline{\text{IAQ}}$) and Interrupt Acknowledge ($\overline{\text{IACK}}$) Timing

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instruction acquisition (\overline{IAQ}), interrupt acknowledge (\overline{IACK}), external flag (XF), and TOUT timing
(continued)

timing parameters for external flag (XF) and TOUT [$H = 0.5 t_{c(CO)}$] (see Figure 30 and Figure 31)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_d(XF)$	Delay time, XF valid after CLKOUT low	- 2	5	- 2	5	ns
$t_d(TOUTH)$	Delay time, TOUT high after CLKOUT low	- 2	3	- 2	3	ns
$t_d(TOUTL)$	Delay time, TOUT low after CLKOUT low	0	5	0	5	ns
$t_w(TOUT)$	Pulse duration, TOUT	2H-10		2H-10		ns

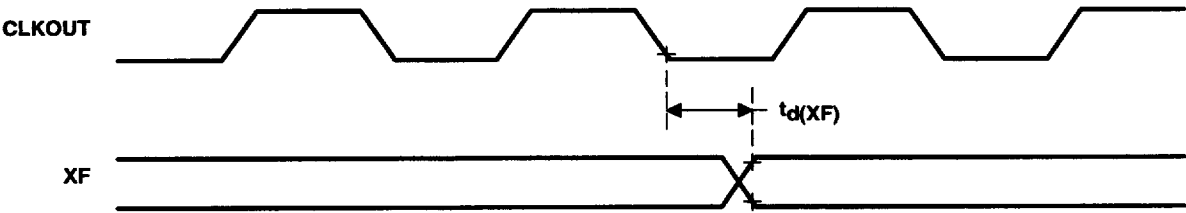


Figure 30. External Flag (XF) Timing

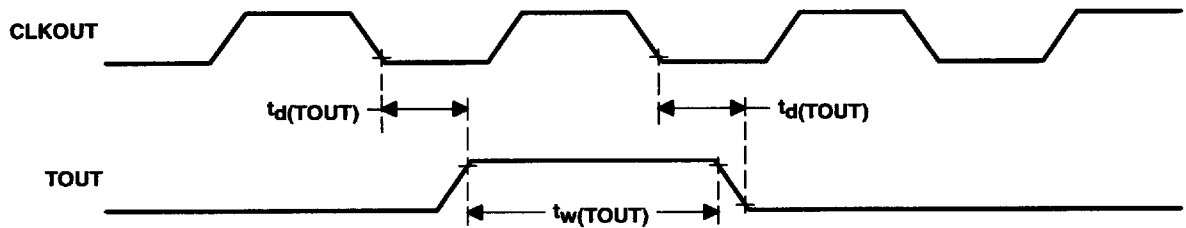


Figure 31. TOUT Timing

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serial port timing

timing parameters for serial port receive [$H = 0.5 t_{c(CO)}$] (see Figure 32)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	6H	†	6H	†	ns
$t_f(SCK)$	Fall time, serial port clock‡		6		6	ns
$t_r(SCK)$	Rise time, serial port clock‡		6		6	ns
$t_w(SCK)$	Pulse duration, serial port clock low/high	3H		3H		ns
$t_h(FSR)$	Hold time, FSR after CLKR falling edge	7		6		ns
$t_h(DR)$	Hold time, DR after CLKR falling edge	7		6		ns
$t_{su}(FSR)$	Setup time, FSR before CLKR falling edge	7		6		ns
$t_{su}(DR)$	Setup time, DR before CLKR falling edge	7		6		ns

† The serial port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞ . It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

‡ Values ensured by design but not tested

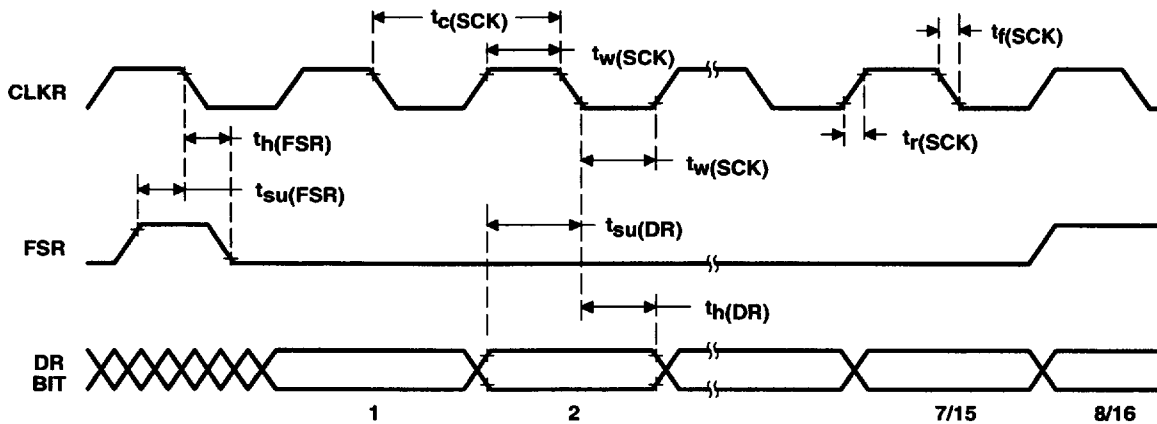


Figure 32. Serial Port Receive Timing

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serial port timing (continued)

timing parameters for serial port transmit with external clocks and frames [$H = 0.5t_{c(CO)}$]
(see Figure 33)

	'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
	MIN	MAX	MIN	MAX	
$t_{c(SCK)}$ Cycle time, serial port clock	6H	†	6H	†	ns
$t_{d(DX)}$ Delay time, DX valid after CLKX rising		25		25	ns
$t_{d(FSX)}$ Delay time, FSX after CLKX rising edge		2H-8		2H-5	ns
$t_{dis(DX)}$ Disable time, DX after CLKX rising ‡		40		40	ns
$t_{h(DX)}$ Hold time, DX valid after CLKX rising	-5		-5		ns
$t_{h(FSX)}$ Hold time, FSX after CLKX falling edge (see Note 1)	7		6		ns
$t_{h(FSX)H}$ Hold time, FSX after CLKX rising edge (see Note 1)		2H-8§		2H-5§	ns
$t_f(SCK)$ Fall time, serial port clock ¶		6		6	ns
$t_r(SCK)$ Rise time, serial port clock ¶		6		6	ns
$t_w(SCK)$ Pulse duration, serial port clock low/high	3H		3H		ns

† The serial port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞ . It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

‡ Values derived from characterization data and not tested.

§ If the FSX pulse does not meet this specification, the first bit of serial data is driven on DX until the falling edge of FSX. After the falling edge of FSX, data is shifted out on DX. The transmit buffer-empty interrupt is generated when the $t_{h(FS)}$ and $t_{h(FSX)H}$ specification is met.

¶ Values ensured by design but not tested.

NOTE 1: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

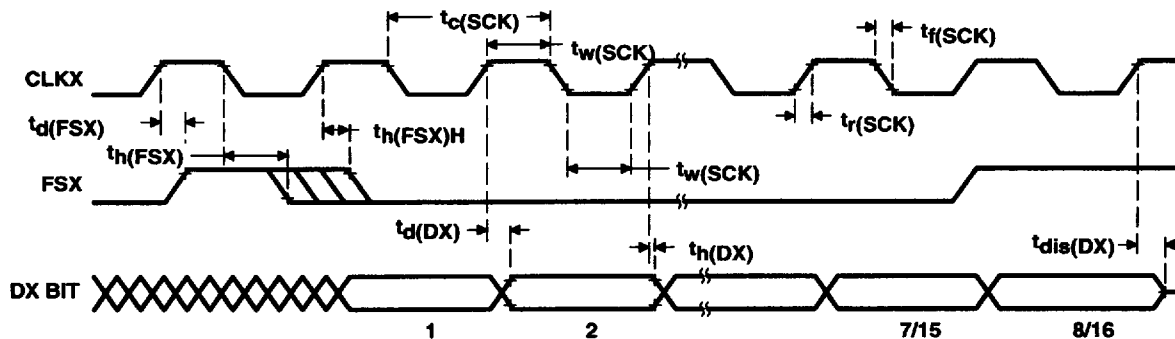


Figure 33. Serial Port Transmit Timing With External Clocks and Frames

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serial port timing (continued)

timing parameters for serial port transmit with internal clocks and frames [$H = 0.5t_c(\text{CO})$]
(see Figure 34)

		'C54x-40 'LC54x-40/'VC54x-40			'LC54x-50 'VC54x-50			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_c(\text{SCK})$	Cycle time, serial port clock		8H			8H		ns
$t_d(\text{FSX})$	Delay time, CLKX rising to FSX			15			15	ns
$t_d(\text{DX})$	Delay time, CLKX rising to DX			15			15	ns
$t_{\text{dis}}(\text{DX})$	Disable time, CLKX rising to DX †			20			20	ns
$t_h(\text{DX})$	Hold time, DX valid after CLKX rising edge	-5			-5			ns
$t_f(\text{SCK})$	Fall time, serial port clock		4			4		ns
$t_r(\text{SCK})$	Rise time, serial port clock		4			4		ns
$t_w(\text{SCK})$	Pulse duration, serial port clock low/high	4H-8			4H-8			ns

† Values derived from characterization data and not tested

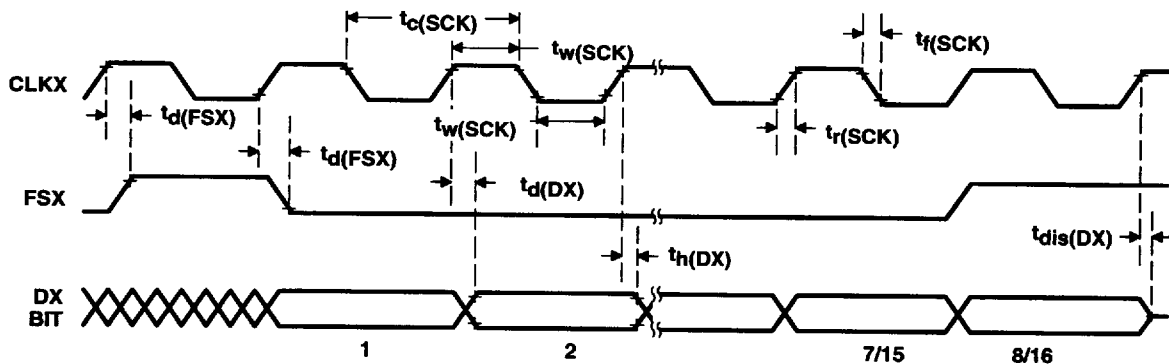


Figure 34. Serial Port Transmit Timing With Internal Clocks and Frames

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buffered serial port receive timing

timing requirements over recommended operating conditions (see Figure 35)

	'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
	MIN	MAX	MIN	MAX	
$t_c(\text{SCK})$ Cycle time, serial port clock	25	†	20	†	ns
$t_f(\text{SCK})$ Fall time, serial port clock ‡		4		4	ns
$t_r(\text{SCK})$ Rise time, serial port clock ‡		4		4	ns
$t_w(\text{SCK})$ Pulse duration, serial port clock low/high‡	8.5		6		ns
$t_{su}(\text{FSR})$ Setup time, FSR before CLKR falling edge (see Note 2)	2		2		ns
$t_h(\text{FSR})$ Hold time, FSR after CLKR falling edge (see Note 2)	10	$t_c(\text{SCK}) - 2^{\S}$	10	$t_c(\text{SCK}) - 2^{\S}$	ns
$t_{su}(\text{DR})$ Setup time, DR before CLKR falling edge	0		0		ns
$t_h(\text{DR})$ Hold time, DR after CLKR falling edge	10		10		ns

† The serial port design is fully static and therefore can operate with $t_c(\text{SCK})$ approaching 0. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

‡ Values ensured by design but not tested

§ First bit is read when FSR is sampled low by CLKR clock.

NOTE 2: Timings for CLKR and FSR are given with polarity bits (CLKP and FSP) set to 0.

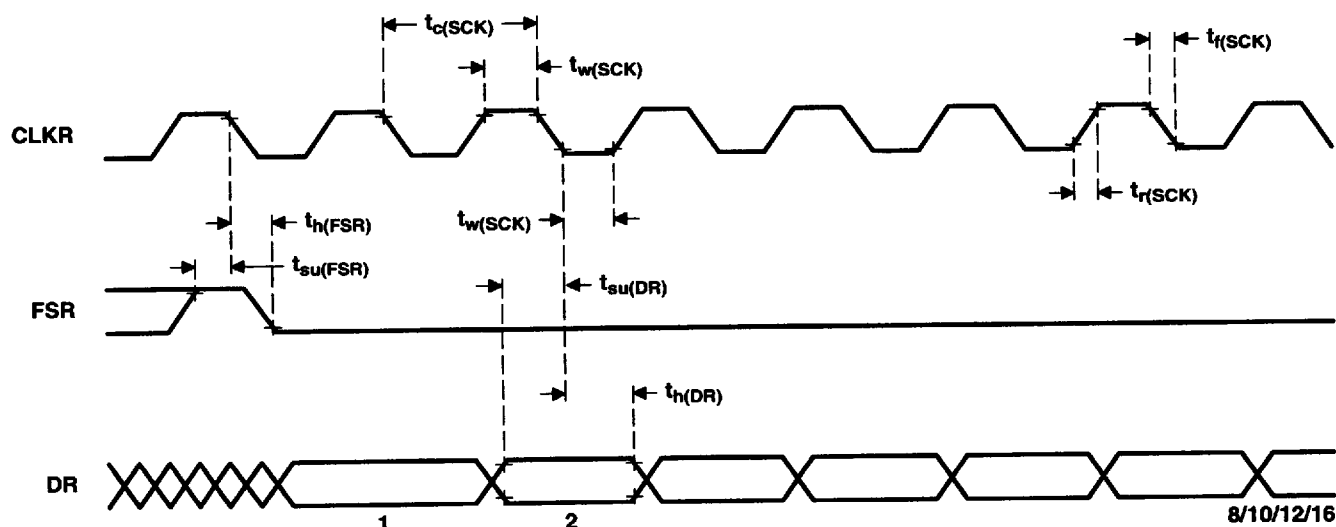


Figure 35. Serial Port Receive Timing

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buffered serial port transmit timing of external frames

switching characteristics over recommended operating conditions (see Figure 36)

PARAMETER	'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
	MIN	MAX	MIN	MAX	
$t_d(DX)$ Delay time, DX valid after CLKX rising		18		18	ns
$t_{dis}(DX)$ Disable time, DX after CLKX rising [†]	4	6	4	6	ns
$t_{dis}(DX)_{pcm}$ Disable time, PCM mode, DX after CLKX rising [†]		6		6	ns
$t_{en}(DX)_{pcm}$ Enable time, PCM mode, DX after CLKX rising [†]	8		8		ns
$t_h(DX)$ Hold Time, DX valid after CLKX rising	4		4		ns

[†] Values derived from characterization data but not tested.

timing requirements over recommended operating conditions (see Figure 36)

	'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
	MIN	MAX	MIN	MAX	
$t_c(SCK)$ Cycle time, serial port clock	25	‡	20	‡	ns
$t_f(SCK)$ Fall time, serial port clock §		4		4	ns
$t_r(SCK)$ Rise time, serial port clock §		4		4	ns
$t_w(SCK)$ Pulse duration, serial port clock low/high §	8.5		6		ns
$t_h(FSX)$ Hold time, FSX after CLKX falling edge (see Notes 1 and 3)	6	$t_c(SCK) - 6^{\parallel}$	6	$t_c(SCK) - 6^{\parallel}$	ns
$t_{su}(FSX)$ Setup time, FSX before CLKX falling edge (see Notes 1 and 3)	6		6		ns

‡ The serial port design is fully static and therefore can operate with $t_c(SCK)$ approaching 0. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

§ Values ensured by design but not tested.

[¶] If FSX does not meet this specification, the first bit of the serial data is driven on DX until FSX goes low (sampled on falling edge of CLKX). After falling edge of the FSX, data will be shifted out on the DX pin.

NOTES: 1. Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependant upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independant of the source of CLKX.

3. Timings for CLKX and FSX are given with polarity bits (CLKP and FSP) set to 0.



buffered serial port transmit timing of external frames (continued)

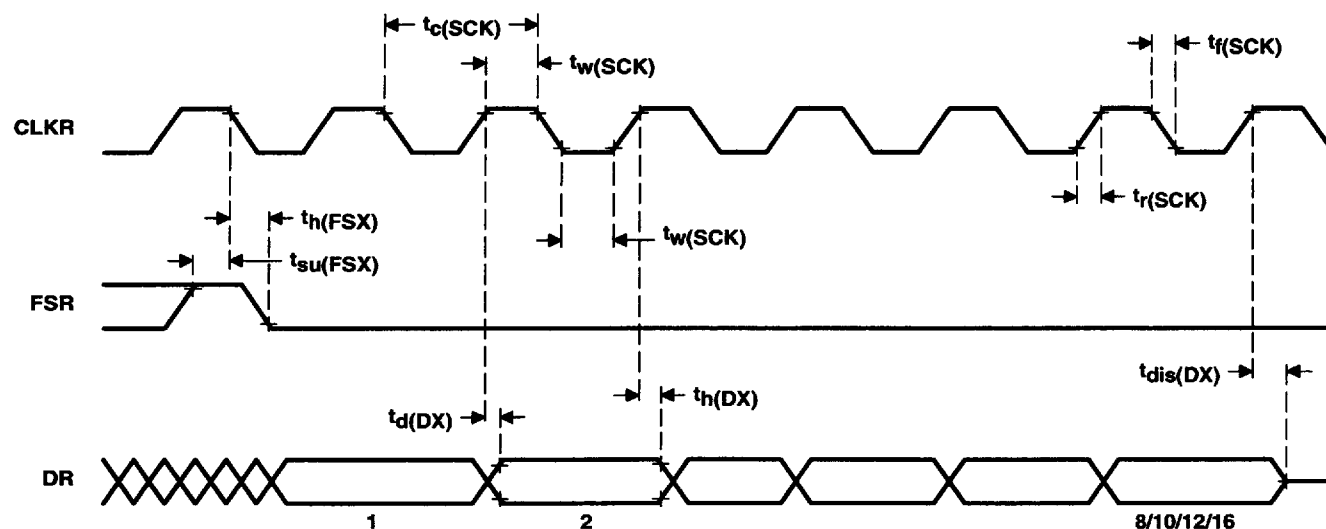


Figure 36. Serial Port Transmit Timing of External Clocks and External Frames

buffered serial port transmit timing of internal frame and internal clock

switching characteristics over recommended operating conditions [$H = 0.5t_{c(CO)}$] (see Figure 37)

PARAMETER	'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
	MIN	MAX	MIN	MAX	
$t_c(SCK)$ Cycle time, serial port clock	2H	62H	2H	62H	ns
$t_d(FSX)$ Delay time, FSX after CLKX rising edge (see Notes 1 and 3)		10		10	ns
$t_d(DX)$ Delay time, DX valid after CLKX rising edge		8		8	ns
$t_{dis}(DX)$ Disable time, DX after CLKX rising edge †	0	5	0	5	ns
$t_{dis}(DX)_{pcm}$ Disable time, PCM mode, DX after CLKX rising edge †		5		5	ns
$t_{en}(DX)_{pcm}$ Enable time, PCM mode, DX after CLKX rising edge †	7		7		ns
$t_h(DX)$ Hold time, DX valid after CLKX rising edge	0		0		ns
$t_f(SCK)$ Fall time, serial port clock ‡		4		4	ns
$t_r(SCK)$ Rise time, serial port clock ‡		4		4	ns
$t_w(SCK)$ Pulse duration, serial port clock low/high‡	H-4		H-4		ns

† Values derived from characterization data but not tested.

‡ Values ensured by design but not tested.

NOTES: 1. Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependant upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independant of the source of CLKX.

3. Timings for CLKX and FSX are given with polarity bits (CLKP and FSP) set to 0.

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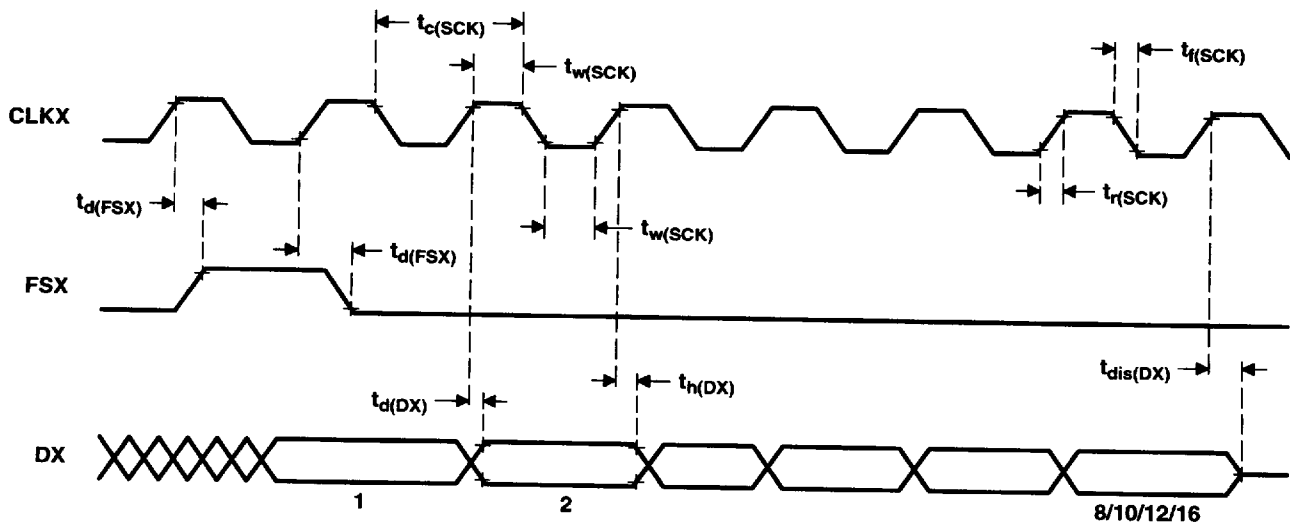


Figure 37. Serial Port Transmit Timing of Internal Clocks and Internal Frames



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serial-port receive timing in TDM mode

timing requirements over recommended ranges of supply voltage and operating free-air temperature [$H = 0.5t_c(CO)$] (see Figure 38)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX†	MIN	MAX†	
$t_c(SCK)$	Cycle time, serial-port clock	8H	‡	8H	‡	ns
$t_f(SCK)$	Fall time, serial-port clock		6		6	ns
$t_r(SCK)$	Rise time, serial-port clock		6		6	ns
$t_w(SCK)$	Pulse duration, serial-port clock low/high	4H		4H		ns
$t_{su}(TD-TCH)$	Setup time, TDAT before TCLK rising edge	25		25		ns
$t_h(TCH-TD)$	Hold time, TDAT after TCLK rising edge	-6		-6		ns
$t_{su}(TA-TCH)$	Setup time, TADD before TCLK rising edge§	25		25		ns
$t_h(TCH-TA)$	Hold time, TADD after TCLK rising edge§	-6		-6		ns
$t_{su}(TF-TCH)$	Setup time, TFRM before TCLK rising edge¶	10		10		ns
$t_h(TCH-TF)$	Hold time, TFRM after TCLK rising edge¶	10		10		ns

† Values ensured by design and are not tested.

‡ The serial-port design is fully static and, therefore, can operate with $t_c(SCK)$ approaching infinity. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

§ These parameters apply only to the first bits in the serial bit string.

¶ TFRM timing and waveforms shown in Figure 38 are for external TFRM. TFRM can also be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in Figure 39.

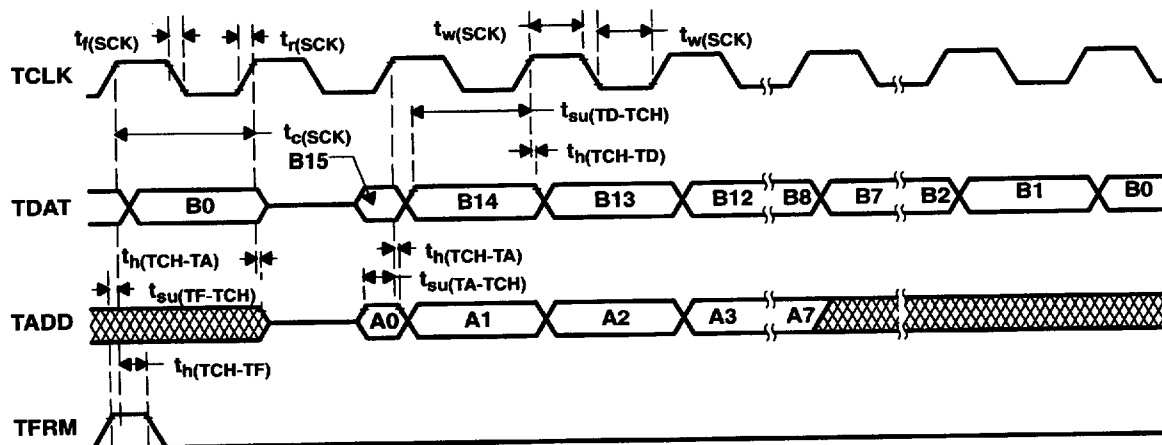


Figure 38. Serial-Port Receive Timing in TDM Mode

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serial-port transmit timing in TDM mode (continued)

switching characteristics over recommended operating conditions [$H = 0.5t_{c(CO)}$] (see Figure 39)

PARAMETER		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_h(TCH-TDV)$	Hold time, external TDAT/TADD valid after TCLK rising edge	0		0		ns
$t_h(TCH-TDV)$	Hold time, internal TDAT/TADD valid after TCLK rising edge	-5		-5		ns
$t_d(TCH-TFV)$	Delay time, TFRM valid after TCLK rising edge, TCLK ext †	H	$3H + 22$	H	$3H + 22$	ns
	Delay time, TFRM valid after TCLK rising edge, TCLK int †	H	$3H + 12$	H	$3H + 12$	ns
$t_d(TC-TDV)$	Delay time, TCLK to valid TDAT/TADD, TCLK ext		22		22	ns
	Delay time, TCLK to valid TDAT/TADD, TCLK int		18		18	ns

† TFRM timing and waveforms shown in Figure 39 are for internal TFRM. TFRM can also be configured as external. The TFRM external case is illustrated in the receive timing diagram in Figure 38.

timing requirements over recommended ranges of supply voltage and operating free-air temperature [$H = 0.5t_{c(CO)}$] (see Figure 39)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_c(SCK)$	Cycle time, serial-port clock	$8H^\ddagger$	$§$	$8H^\ddagger$	$§$	ns
$t_f(SCK)$	Fall time, serial-port clock		6¶		6¶	ns
$t_r(SCK)$	Rise time, serial-port clock		6¶		6¶	ns
$t_w(SCK)$	Pulse duration, serial-port clock low/high	$4H^\ddagger$		$4H^\ddagger$		ns

‡ When SCK is generated internally this value is typical.

§ The serial-port design is fully static and, therefore, can operate with $t_c(SCK)$ approaching ∞ . It is characterized approaching an input frequency of 0 Hz but tested as a much higher frequency to minimize test time.

¶ Values ensured by design but are not tested

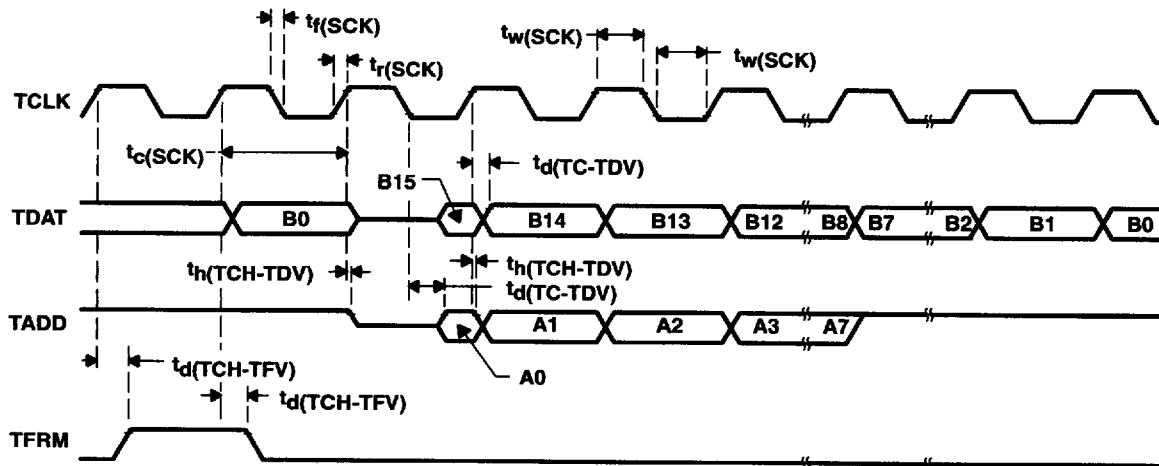


Figure 39. Serial-Port Transmit Timing in TDM Mode

TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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host port interface

switching characteristics over recommended operating conditions [$H = 0.5t_{c(CO)}$] (See Notes 4 and 5) (see Figure 40 through Figure 43)

PARAMETER		MIN	MAX	UNIT
$t_{d(DSL-HDV)}$	Delay time, \overline{DS} low to HD valid	5 [†]	12 [‡]	ns
$t_{d(HEL-HDV1)}$	Delay time, HDS falling to HD valid for first byte of a subsequent read: Case 1: Shared-access mode if $t_{w(HDS)h} < 7H$ § [¶] Case 2: Shared-access mode if $t_{w(HDS)h} > 7H$ Case 3: Host-only mode if $t_{w(HDS)h} < 7H$ Case 4: Host-only mode if $t_{w(HDS)h} > 7H$		$7H+20-t_{w(DSH)}_{20}^{\ddagger}$ $40-t_{w(DSH)}_{20}^{\ddagger}$	ns
$t_{d(DSL-HDV2)}$	Delay time, \overline{DS} low to HD valid, second byte	5 [¶]	20	ns
$t_{d(DSH-HYH)}$	Delay time, \overline{DS} high to HRDY high		10(6)H+10 [‡]	ns
$t_{su(HDV-HYH)}$	Setup time, HD valid before HRDY rising edge	3H–10 [‡]		ns
$t_h(DSH-HDV)$	Hold time, HD valid after \overline{DS} rising edge	0	12 [†] #	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT rising edge to HRDY high		10 [‡]	ns
$t_{d(DSH-HYL)}$	Delay time, \overline{HDS} or \overline{HCS} high to HRDY low		12 [‡]	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT rising edge to \overline{HINT} change		15	ns

[†] Values derived from characterization data and not tested.

[‡] Values ensured by design but not tested.

§ Host-only mode timings apply for read accesses to HPIC or HPIA, write accesses to BOB, and resetting DSPINT or HINT to 0 in shared-access mode. HRDY does not go low for these accesses.

¶ Shared-access mode timings will be met automatically if HRDY is used.

HD release

NOTES: 4. SAM = shared-access mode, HOM = host-only mode

HAD stands for HCNTL0, HCNTL1, and HR/W.

\overline{HDS} refers to either HDS1 or HDS2.

\overline{DS} refers to the logical OR of \overline{HCS} and \overline{HDS} .

5. On host read accesses to the HPI, the setup time of HD before \overline{DS} rising edge depends on the host waveforms and cannot be specified here.

timing requirements over recommended operating conditions [$H = 0.5t_{c(CO)}$] (See Note 4) (see Figure 40 through Figure 43)

	MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HAD/HBIL valid before \overline{DS} falling edge	10	ns
$t_h(DSL-HBV)$	Hold time, HAD/HBIL valid after \overline{DS} falling edge	10	ns
$t_{su(HSL-DSL)}$	Setup time, \overline{HAS} low before \overline{DS} falling edge	12	ns
$t_w(DSL)$	Pulse duration, \overline{DS} low	30 [¶]	ns
$t_w(DSH)$	Pulse duration, \overline{DS} high	10	ns
$t_c(DSH-DSH)^{ }$	Cycle time, \overline{DS} rising edge to next \overline{DS} rising edge: Case 1: When using HRDY (see Figure 39) Case 2a: SAM accesses and HOM active writes to DSPINT or HINT without using HRDY (see Figure 37 and Figure 38) Case 2b: When not using HRDY for other HOM accesses	50 10H [‡] 50	ns
$t_{su(HDV-DSH)}$	Setup time, HD valid before \overline{DS} rising edge	12	ns
$t_h(DSH-HDV)$	Hold time, HD valid after \overline{DS} rising edge	0	ns

[‡] Values ensured by design but not tested.

¶ A host not using HRDY should meet the 10H requirement all the time unless a software handshake is used to change the access rate according to the HPI mode.

NOTE 4: SAM = shared-access mode, HOM = host-only mode

HAD stands for HCNTL0, HCNTL1, and HR/W.

\overline{HDS} refers to either HDS1 or HDS2.

\overline{DS} refers to the logical OR of \overline{HCS} and \overline{HDS} .

ADVANCE INFORMATION



host port interface (continued)

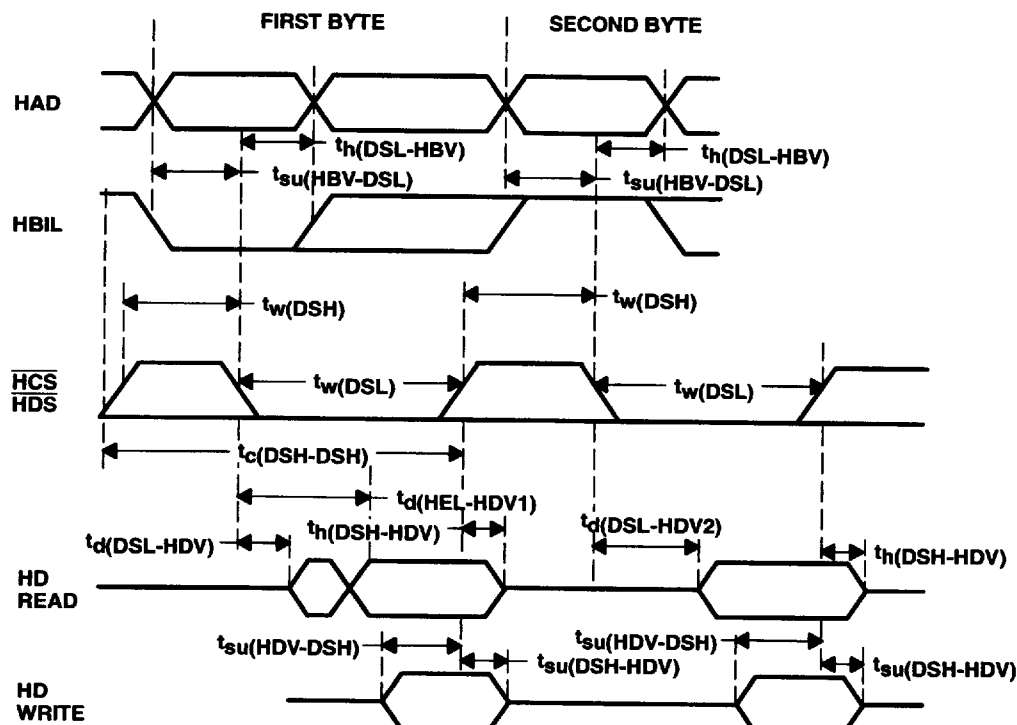


Figure 40. Read/Write Access Timings Without HRDY or HAS

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host port interface (continued)

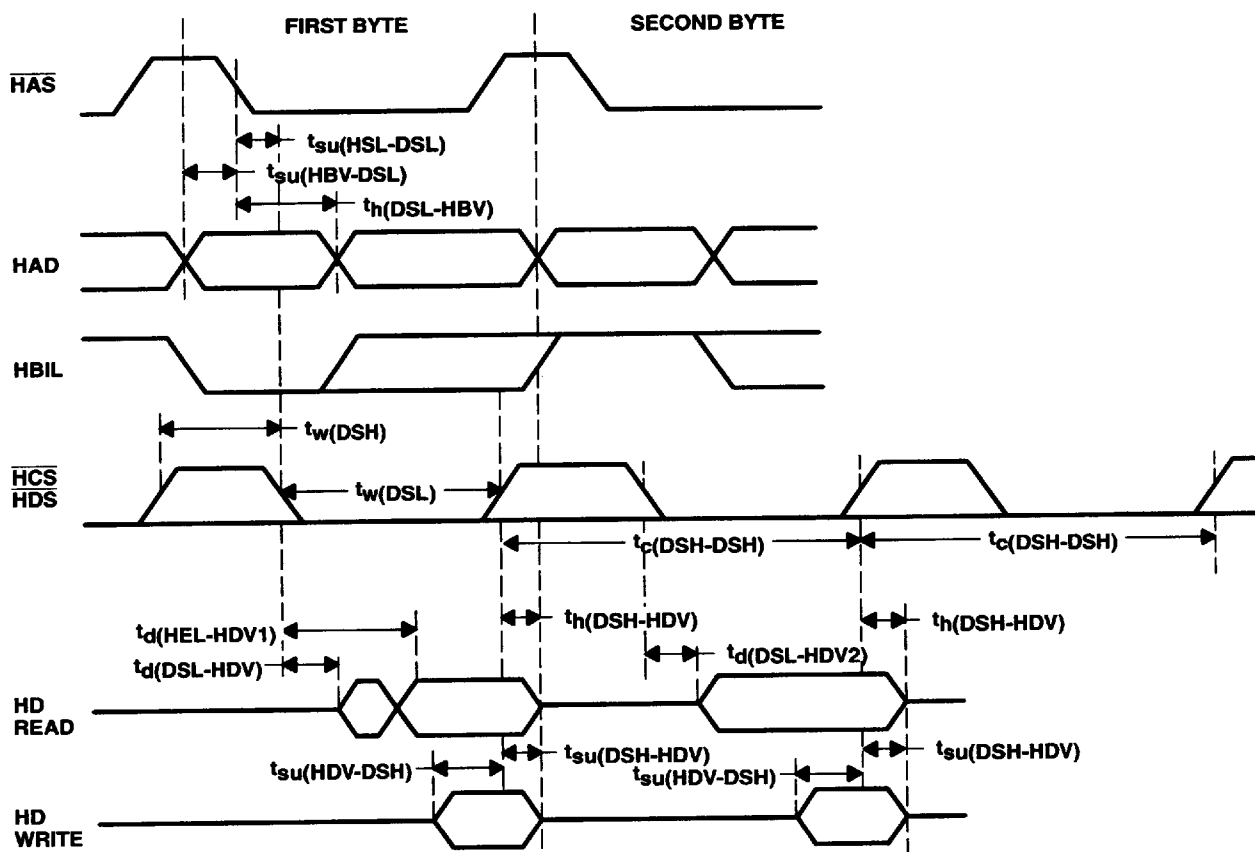


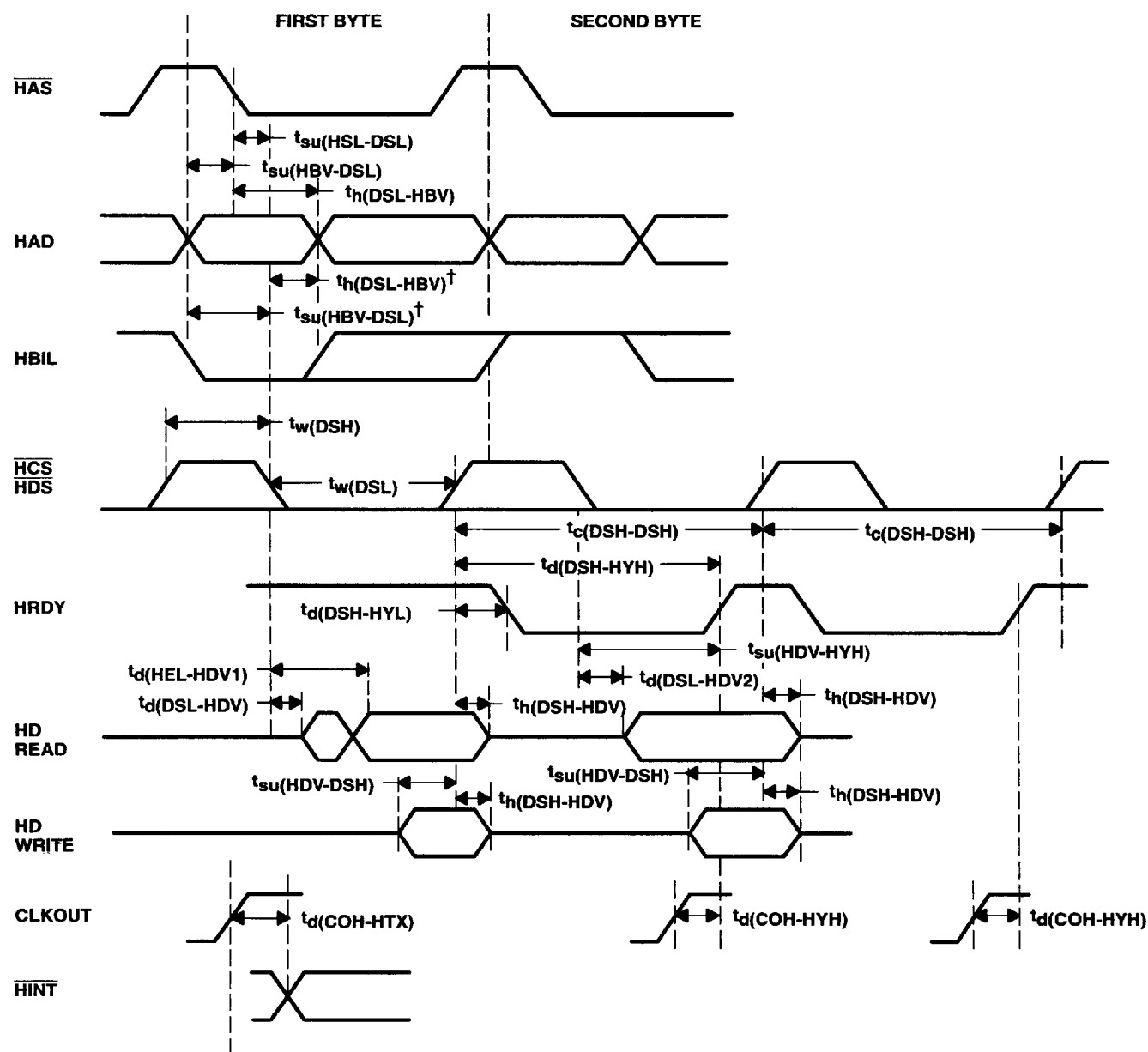
Figure 41. Read/Write Access Timings Using $\overline{\text{HAS}}$ Without HRDY

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host port interface (continued)



† When \overline{HAS} is tied to V_{DD}

Figure 42. Read/Write Access Timing With HRDY

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host port interface (continued)

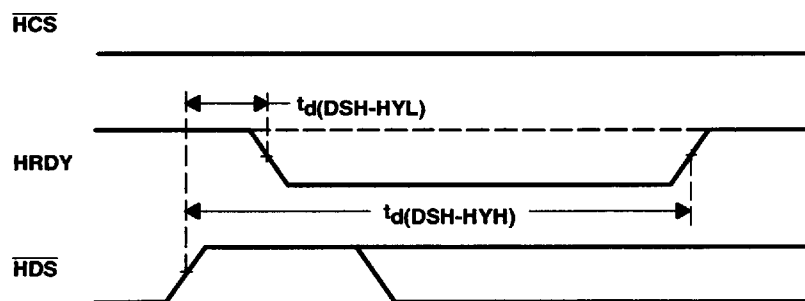
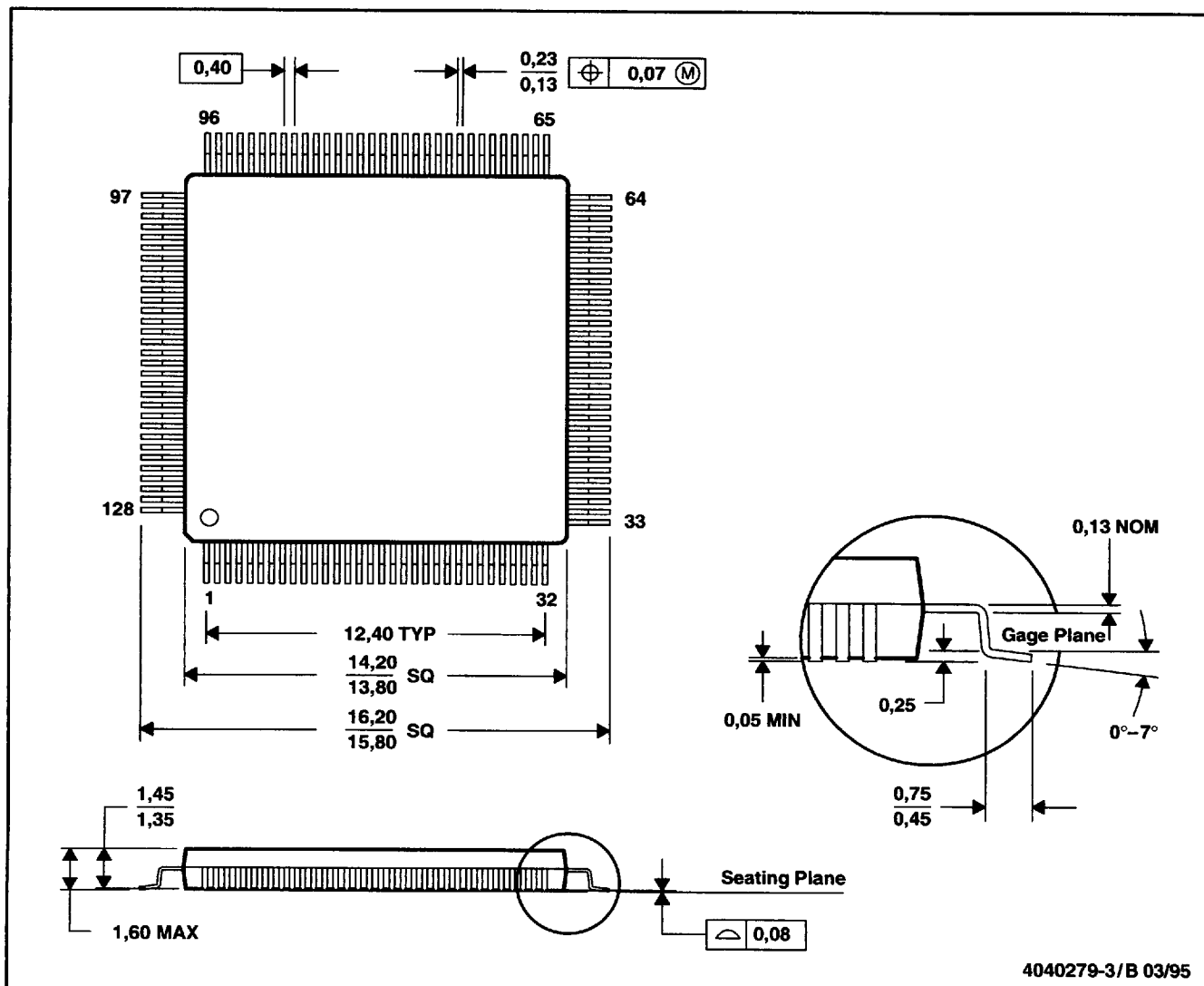


Figure 43. HRDY Signal When \overline{HCS} Is Always Low

MECHANICAL DATA

TMS320LC542/VC542 128-Pin Quad Flatpack Plastic Package
PBK (S-PQFP-G128)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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8961722 0096883 868

TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

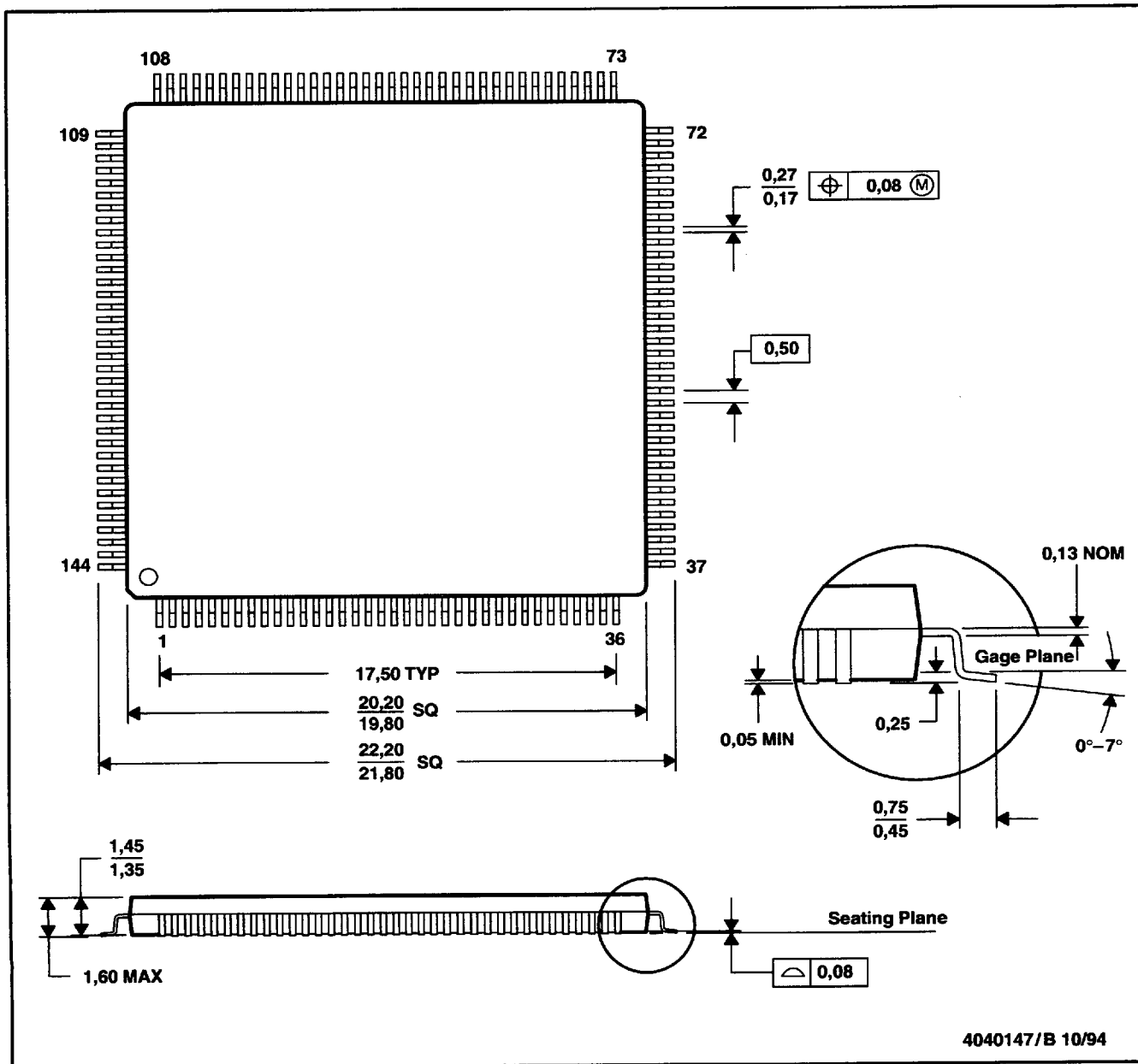
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MECHANICAL DATA

TMS320C542/LC542/VC542 144-Pin Quad Flatpack Plastic Package
PGE (S-PQFP-G144)

PLASTIC QUAD FLATPACK

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- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

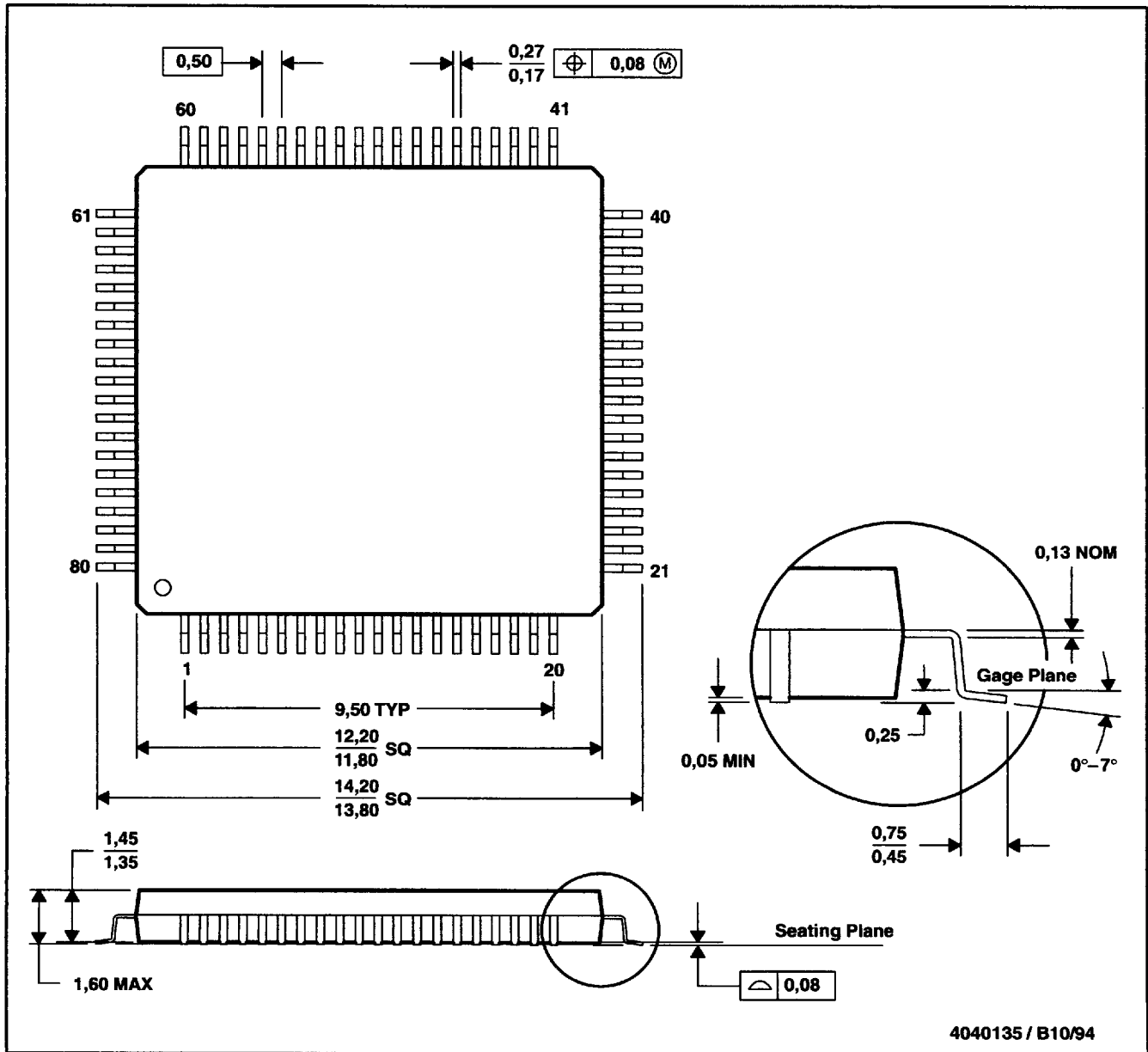
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MECHANICAL DATA

PN (S-PQFP-G80)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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TMS320C54x, TMS320LC54x, TMS320VC54x FIXED-POINT DIGITAL SIGNAL PROCESSORS

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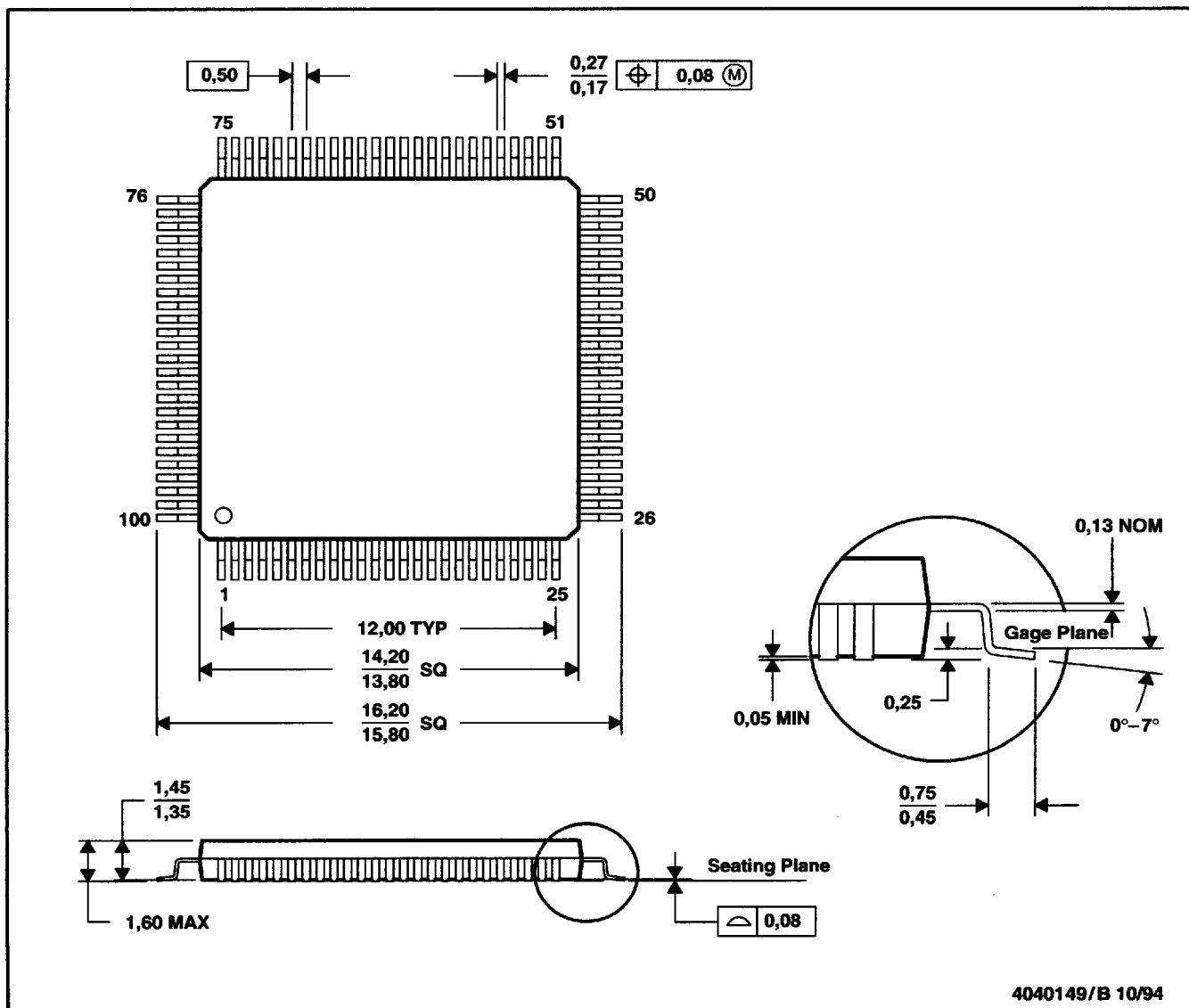
MECHANICAL DATA

TMS320C541/'LC541/'VC541/'LC543/'VC543 100-Pin Thin Quad Flatpack Plastic Package

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK

ADVANCE INFORMATION



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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