REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device 02. Editorial changes throughout.	94-04-08	M.L. Poelking
B	Changes in accordance with NOR 5962-R048-95.	94-12-29	M.L. Poelking
C	Add device 03. Editorial changes throughout.	95-03-29	T. Hess

REV																			
SHEET																			
REV	A	A																	
SHEET	15	16																	

REV STATUS OF SHEETS	REV	C	C	A	A	C	C	C	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Thomas M. Hess

CHECKED BY Thomas M. Hess

APPROVED BY Monica L. Poelking

DRAWING APPROVAL DATE
93-03-01

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, TWO DIMENSIONAL CONVOLVER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-93007
A	67268	

SHEET 1 OF 16

DESC FORM 193
JUL 94

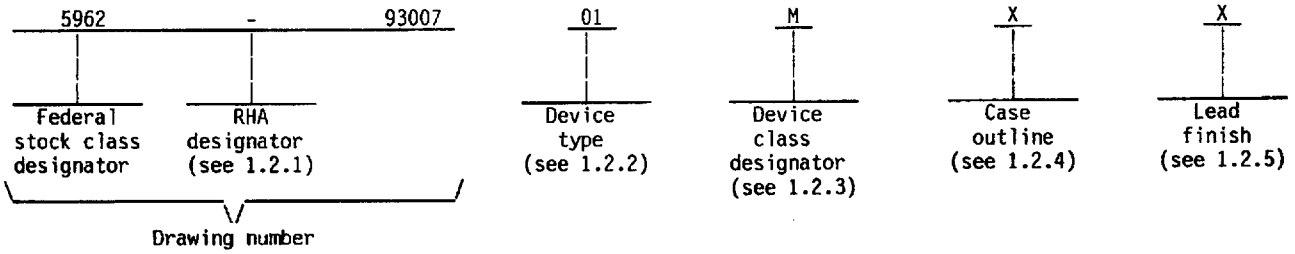
5962-E153-95

9004708 0006637 532

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Speed
01	48908-20	Two dimensional convolver	20 MHz
02	48908-27	Two dimensional convolver	27 MHz
03	48908-40	Two dimensional convolver	40 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P84	84	Pin-grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage	8.0 V
Input, output, or I/O voltage applied range	GND - 0.5 V to V_{CC} + 0.5 V
Storage temperature range (T_S)	-65°C to 150°C
Lead temperature (soldering, 10 seconds)	300°C
Junction temperature (T_J)	175°C
Thermal resistance:	
Junction-to-ambient (θ_{JA})	34.56°C/W
Junction-to-case (θ_{JC})	See MIL-STD-1835
Power dissipation at 125°C	1.45 W

1.4 Recommended operating conditions.

Operating voltage range	4.5 V to 5.5 V
Ambient operating temperature range (T_A)	-55°C to 125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical 1 input voltage	V_{IH}	V_{CC} = 5.5 V	1,2,3	All	2.2		V
Logical 0 input voltage	V_{IL}	V_{CC} = 4.5 V	1,2,3	All		0.8	V
Clock input high voltage	V_{IHC}	V_{CC} = 5.5 V	1,2,3	All	3.0		V
Clock input low voltage	V_{ILC}	V_{CC} = 4.5 V	1,2,3	All		0.8	V
Output high voltage	V_{OH}	I_{OH} = -400 µA, V_{CC} = 4.5 V 2/	1,2,3	01,02 03	2.6 2.8		V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA, V_{CC} = 4.5 V 2/	1,2,3	All		0.4	V
Input leakage current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 5.5 V	1,2,3	All	-10	10	µA
Output or I/O leakage current	I_O	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5 V	1,2,3	All	-10	10	µA
Standby power supply current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5 V, Outputs open	1,2,3	All		500	µA
Operating power supply current	I_{CCOP}	f = 20.0 MHz, V_{CC} = 5.5 V, Outputs open 3/ 4/	1,2,3	All		160	mA
Clock period	t_{CYCLE}	See figure 3	9,10,11	01 02 03	50 37 25		ns
Clock pulse width high	t_{PWH}	See figure 3	9,10,11	01 02 03	20 15 8		ns
Clock pulse width low	t_{PWL}	See figure 3	9,10,11	01 02 03	20 15 8		ns
Data input setup time	t_{DS}	See figure 3	9,10,11	01 02 03	17 16 8		ns

See footnotes at the end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data input hold time	t_{DH}	See figure 3	9,10,11	All	0		ns
Clock to data out	t_{OUT}	See figure 3	9,10,11	01 02 03		28 19 15	ns
Address setup time	t_{AS}	See figure 3	9,10,11	01 02 03	15 15 10		ns
Address hold time	t_{AH}	See figure 3	9,10,11	All	0		ns
Configuration data setup time	t_{CDS}	See figure 3	9,10,11	01 02 03	20 17 10		ns
Configuration data hold time	t_{CDH}	See figure 3	9,10,11	All	0		ns
LD# pulse width	t_{LPW}	See figure 3	9,10,11	01 02 03	20 15 8		ns
LD# setup time	t_{LCS}	See figure 3 5/	9,10,11	01 02 03	37 30 15		ns
CIN7-0 setup to CLK	t_{CS}	See figure 3	9,10,11	01 02 03	20 17 10		ns
CIN7-0 hold from CLK	t_{CH}	See figure 3	9,10,11	All	0		ns
CS# setup to LD#	t_{CSS}	See figure 3	9,10,11	All	0		ns
CS# hold from LD#	t_{CSH}	See figure 3	9,10,11	All	0		ns
RESET# pulse width	t_{RPW}	See figure 3	9,10,11	01 02 03	50 37 8		ns
FRAME# setup to CLK	t_{FS}	See figure 3 6/	9,10,11	01 02 03	30 25 20		ns
FRAME# pulse width	t_{FPW}	See figure 3	9,10,11	01 02 03	50 37 8		ns
EALU setup time	t_{ES}	See figure 3	9,10,11	01 02 03	17 15 10		ns
EALU hold time	t_{EH}	See figure 3	9,10,11	All	0		ns

See footnotes at the end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HOLD setup time	t_{HS}	See figure 3	9,10,11	01 02 03	14 13 9		ns
HOLD hold time	t_{HH}	See figure 3	9,10,11	01 02 03	2 2 0		ns
Output enable time	t_{EN}	See figure 3 7/	9,10,11	01 02 03		28 19 15	ns
Output disable time	t_{OZ}	See figure 3 4/ 8/	9,10,11	01 02 03		40 35 8	ns
Output rise time	t_R	See figure 3, From 0.8 V to 2.0 V 4/ 8/	9,10,11	01 02 03		6 6 5	ns
Output fall time	t_F	From 2.0 V to 0.8 V See figure 3 4/ 8/	9,10,11	01 02 03		6 6 5	ns
Input capacitance	C_{IN}	V_{CC} = Open, f = 1 MHz, All measurements are referenced to device GND, See 4.4.1c, T_A = 25°C 8/	4	All		10	pF
Output capacitance	C_O	V_{CC} = Open, f = 1 MHz, All measurements are referenced to device GND, See 4.4.1c 8/ T_A = 25°C	4	All		12	pF
Functional tests		See 4.4.1b	7,8	All			

1/ All testing to be performed using worst-case test conditions unless otherwise specified. A.C. testing (except subgroup 7,8 functional testing) shall be performed as follows: Input levels (clk input) 4.0 V and 0 V, Input levels (all other inputs) 0 V and 3.0 V. Timing reference levels (clk) = 2.0 V, (others) = 1.5 V. Output load per test load circuit with CL = 40 pF. Output transition is measured at $V_{OH} \ge 1.5$ V and $V_{OL} \le 1.5$ V. The # indicates active low.
2/ Interchanging of force and sense conditions is permitted.
3/ Operating supply current is proportional to frequency, typical rating is 8.0 mA/MHz.
4/ Loading is as specified in the test load circuit with C_L = 40 pF.
5/ This test applies only to the case where the device is being written to during an active convolution cycle. It must be met in order to achieve predictable results at the next rising clock edge. In most applications, the configuration data and coefficients are loaded asynchronously and the T_{LCS} specification may be disregarded.
6/ While FRAME# is an asynchronous signal, it must be deasserted a minimum of T_{FS} ns prior to the rising clock edge which is to begin loading pixel data for a new frame.
7/ Transition is measured at ±200 mV from steady state voltage with loading as specified in test load circuit with C_L = 40 pF.
8/ Parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process design changes.

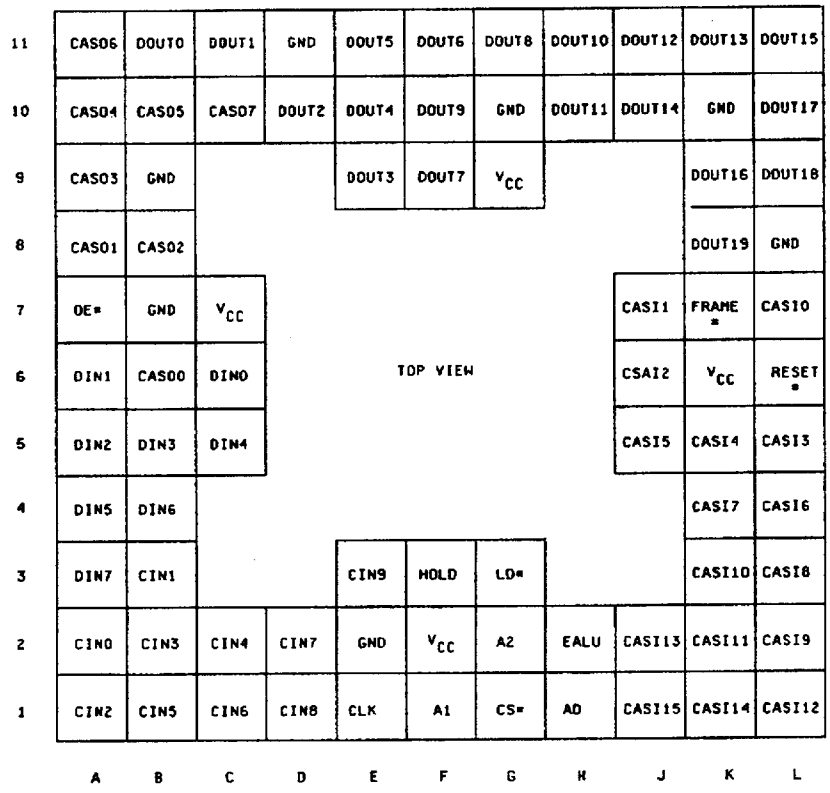


FIGURE 1. Terminal connections.

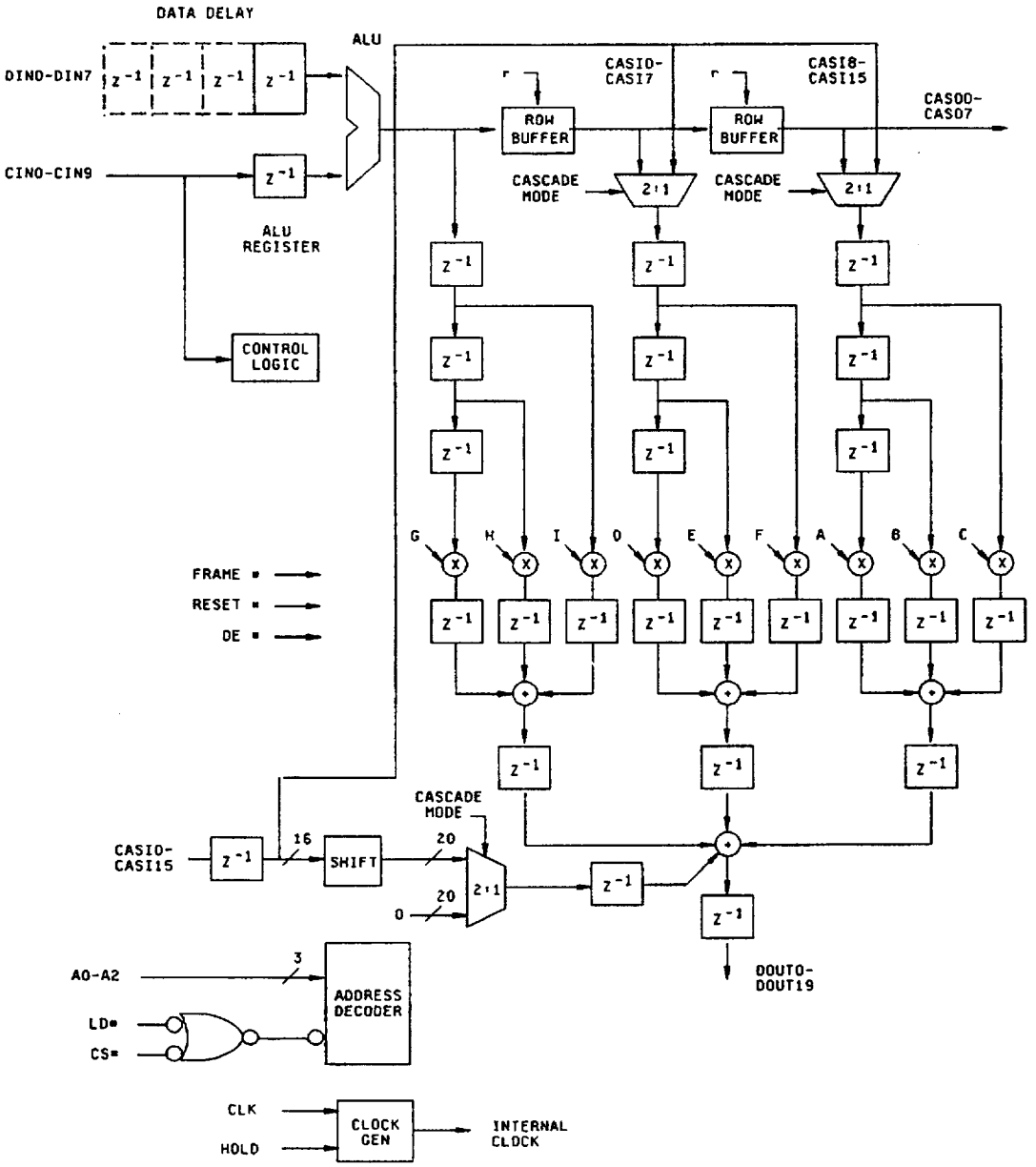


FIGURE 2. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93007
		REVISION LEVEL C	SHEET 9

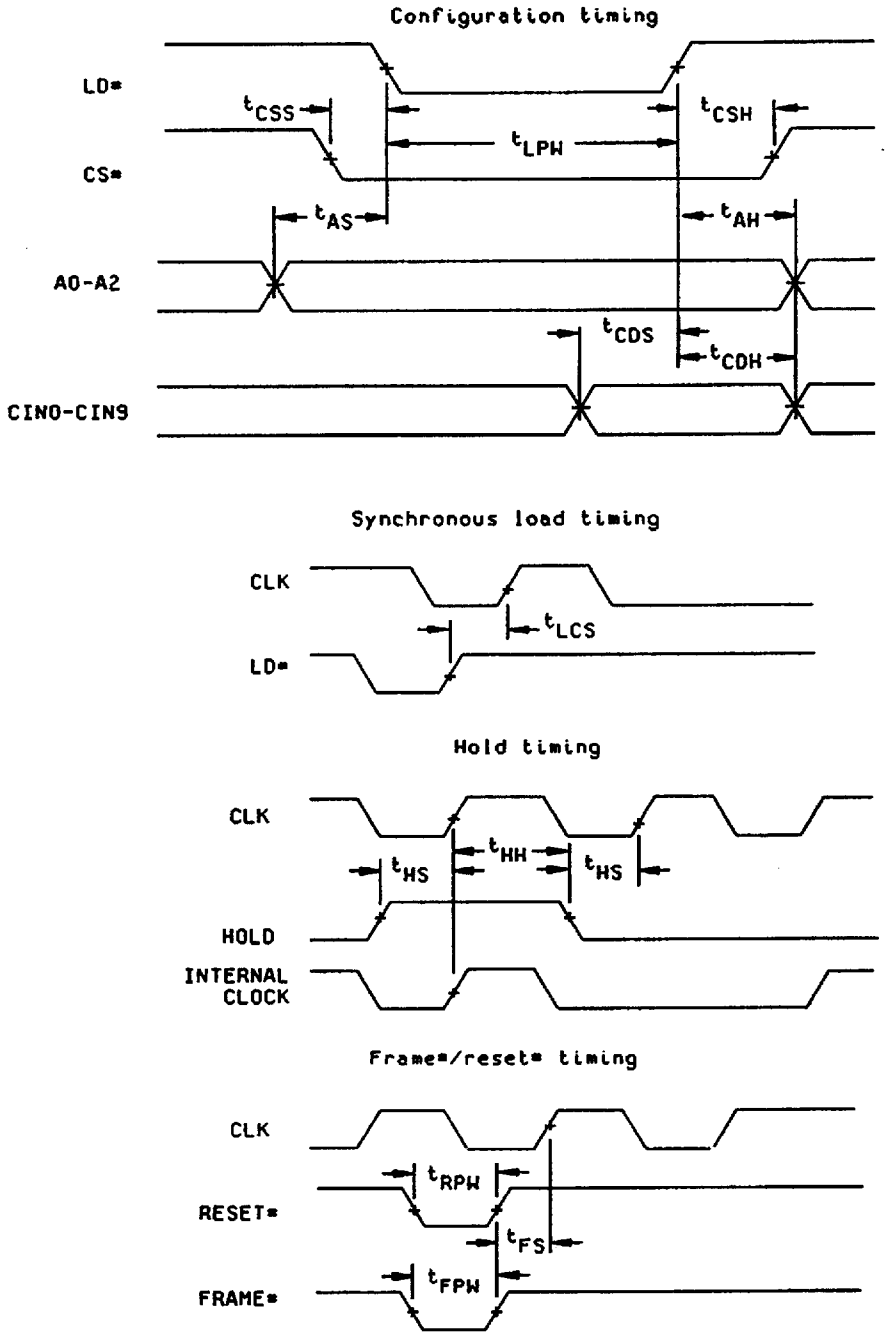
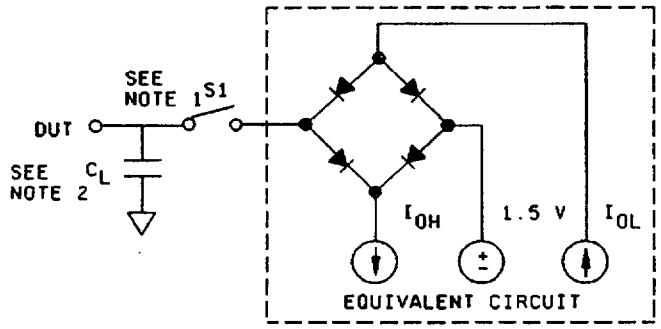


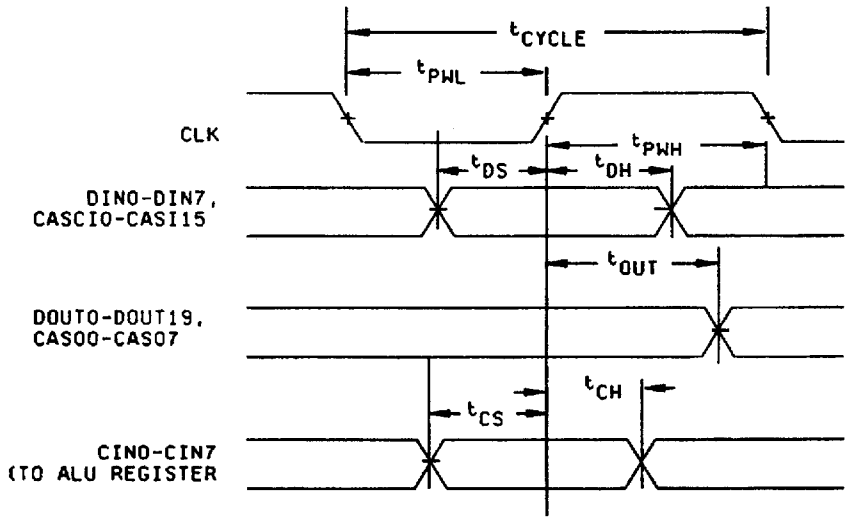
FIGURE 3. Timing waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-93007
		REVISION LEVEL C	SHEET 10

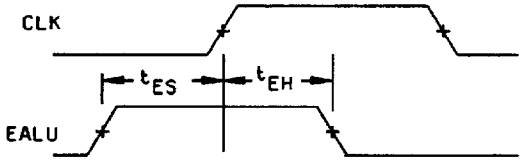


NOTES:
1. Switch S1 open for I_{CCSB} and I_{CCOP} tests.
2. Includes stray and jig capacitance.

Functional timing



EALU timing



Three-state control

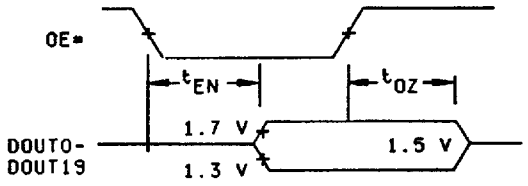


FIGURE 3. Timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein. Interim test is optional at the discretion of the manufacturer.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} and C_O measurement) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 1/ 9, 10, 11	1, 2, 3, 7, 1/ 8, 9, 10, 11	1, 2, 3, 7, 2/ 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)			

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

V_{CC}	The +5 V power supply pins. 0.1 µF capacitors between the V_{CC} and GND pins are recommended.
GND	The device ground.
CLK	Input and System clock. Operations are synchronous with the rising edge of this clock signal.
DIN0-7	Pixel Data input bus. This bus is used to provide the 8-bit pixel input data to the device. The data must be provided in a synchronous fashion, and is latched on the rising edge of the CLK signal.
CIN0-9	Coefficient input bus. This input bus is used to load the Coefficient Mask registers(s), the initialization register, the Row Buffer length register and the ALU microcode. It may also be used to provide a second operand input to the ALU. The definition of the CIN0-9 is defined by the register address bits A0-2. The CIN0-9 data is loaded to the addressed register through the use of the CS# and LD# inputs.
DOUT0-19	Output data bus. This 20-bit output port is used to provide the convolution result. The result is the sum of products of the input data samples and their corresponding coefficients. The cascade inputs CASI0-15 may also be added to the result by selecting the appropriate cascade mode in the initialization register.

CASI0-15 Cascade input bus. This bus is used for cascading multiple devices to allow convolution with larger kernels or row sizes. It may also be used to interface to external row buffers. The function of this bus is determined by the Cascade Mode bit (bit 0) of the initialization register. When this bit is set to a '0', the value on CASI0-15 is left shifted and added to DOUT0-19. The amount of the shift is determined by bits 7-8 of the initialization register. While this mode is intended primarily for cascading, it may also be used to add an offset value, such as to increase the brightness of the convolved image.
When the cascade mode bit is set to a '1', this bus is used for interfacing to external row buffers. In this mode the bus is divided into two 8-bit buses (CASI0-7 and CASI8-15), thus allowing two additional pixel data inputs. The cascade data is sent directly to the internal multiplier array which allows for larger row sizes without using multiple devices.

CASO0-7 Cascade output bus. This bus is used primarily during cascading to handle larger frames or kernel sizes. This output data is the data on DIN0-7 delayed by twice the programmed internal row buffer length.

FRAME# Frame # is an asynchronous new frame or vertical sync input. A low on this input resets all internal circuitry except for the coefficient, ALU, AMC, EOR and INT register. Thus, after a Frame# reset has occurred, a new frame of pixels may be convolved without reloading these registers.

EALU Enable ALU input. This control line gates the clock to the ALU register. When it is high, the data on CIN0-7 is loaded on the next rising clock edge. When EALU is low, the last value loaded remains in the ALU register.

HOLD The hold input is used to gate the clock from all of the internal circuitry of the device. This signal is synchronous and is sampled on the rising edge of CLK and takes effect on the following cycle. While this signal is active (high), the clock will have no effect on the device and internal data will remain undisturbed.

RESET# Reset is an asynchronous signal which resets all internal circuitry of the device. All outputs are forced low in the reset state.

OE# Output enable. The OE# input controls the state of the output data bus (DOUT0-19). A low on this control line enables the port for output. When OE# is high, the output drivers are in the high impedance state. Processing is not interrupted by this pin.

A0-2 Control register address. These lines are decoded to determine which register in the control logic is the destination for the data on the CIN0-9 inputs. Register loading is controlled by the A0-2, LD#, and CS# inputs.

LD# Load strobe. LD# is used for loading the internal registers of the device. When CS# and LD# are active, the rising edge of LD# will latch the CIN0-7 data into the register specified by A0-2.

CS# Chip select. The chip select input enable loading of the internal registers. When CS# is low, the A0-2 address lined are decoded to determine the meaning of the data on the CIN0-7 bus. The rising edge of LD# will then load the addressed register.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.