Value Series Flash Memory Card 2, 4, 8, 16 MEGABYTE (Intel/Sharp based)

General Description

The WEDC Value Series (FV) Flash memory cards offers a low cost linear Flash solid state storage solution for code and data storage, high performance disk emulation, mobile PC and embedded applications.

The WEDC Value series is based on Intel/Sharp Flash memories. Cards are based on the 28F008SA (8Mb), 28F008S5 (8Mb) or 28F016S5 (16Mb) devices whose device codes are A2H, A6H and AAH respectively. Systems should be able to recognize all three codes. The symmetrically blocked architecture and single 5V operation provides a cost effective, high performance, nonvolatile storage solution. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

The Value series is designed as a simple x16 linear array of Flash devices. Two Flash devices in parallel provide the lower and upper bytes for the 16 bit access. The Value series does not provide access of the ODD byte (D8 - D15) on the even byte data path (D0 - D7).

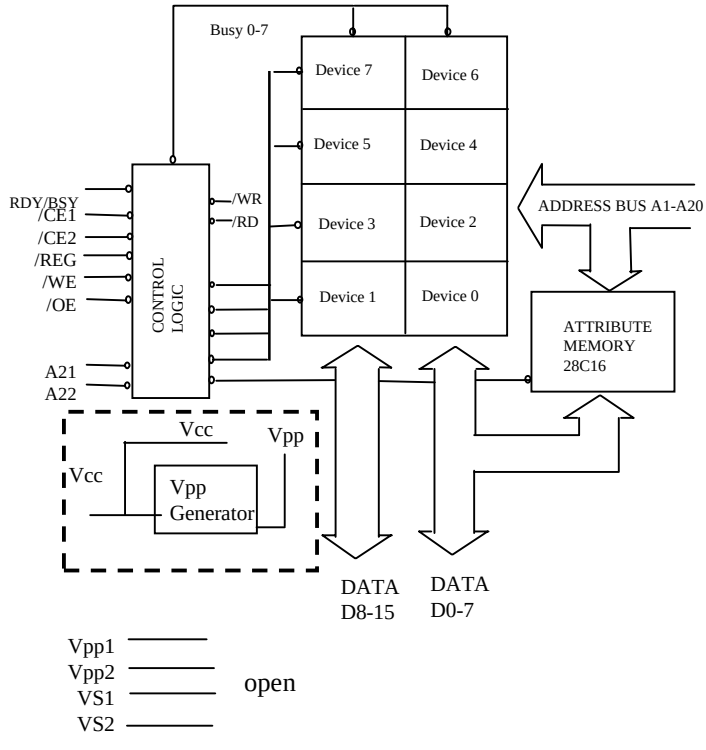
WEDC's standard Value Series Flash Card is shipped with no attribute memory or CIS (Card Information Structure) information. An option for 2KB of attribute memory with CIS information is available. The CIS for the WEDC Value series may also be stored in Block 0 (even bytes, D0 - D7 only) of the Flash memory, this option is available by request only.

WEDC's standard cards are shipped with WEDC's Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

Features

- Low cost Linear Flash Card
- Single 5 Volt Supply
- Based on FlashFile™ Components
- Fast Read Performance
  - 100ns or 150ns Maximum Access Time
- x16 Data Interface
  - Odd byte not accessible on Even byte
- High Performance Random Writes
  - 10µs Typical Word Write Time
- Automated Write and Erase Algorithms
  - Intel Command Set
- 50µA Typical Deep Power-Down
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

Block Diagram



Note: VPP Generator only required for cards using 28F008SA devices configuration above for 8MB card using 8Mbit components.

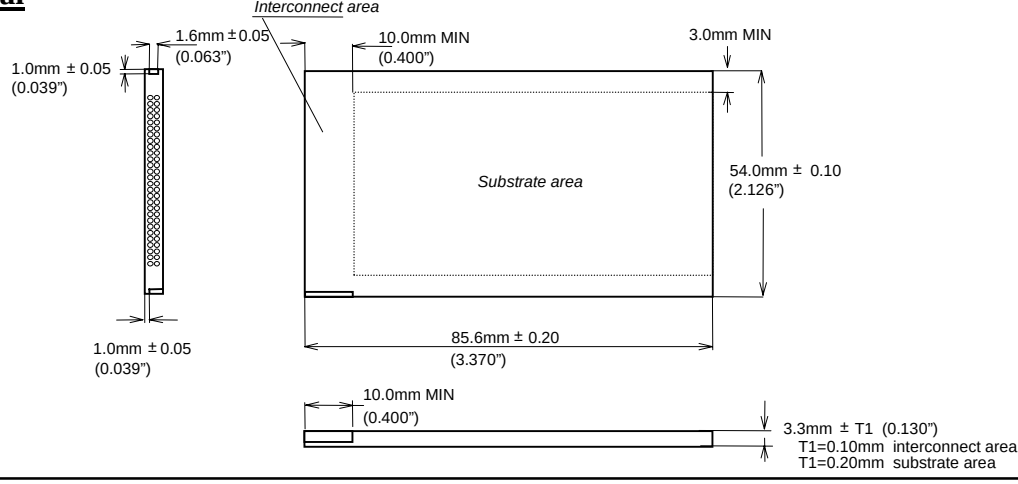
Pinout

Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	N.C.
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	2MB(2)
50	A21	I	Address bit 21	4MB(2)
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	8MB(2)
54	A23	I	Address bit 23	16MB(2)
55	A24	I	Address bit 24	N.C.
56	A25	I	Address bit 25	N.C.
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH
59	Wait#	O	Extended Bus cycle	LOW
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	
63	BVD1	O	Bat. Volt. Detect 1	
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:
1. RDY/BSY signal is a full CMOS output, pull-up resistors are not required.
2. Shows density for which specified address bit is MSB. Higher order address bits are no connects (ie 4MB A21 is MSB A22 - A25 are NC).

Mechanical



Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not decoded since the card is x16 only. The memory will wrap at the card density boundary. The system should not try to access memory beyond the card density. The upper addresses are not connected.
DQ0 - DQ15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ0 - DQ7 constitute the lower (even) byte and DQ8 - DQ15 the upper (odd) byte. DQ15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Odd byte (DQ8 - DQ15) can not be accessed on DQ0 - DQ7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal enabling read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses.
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins.
WP	OUTPUT	**WRITE PROTECT:** This signal is pulled low internally. This signifies write protect = "off " for all cases.
VPP1, VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Not connected for 5V only card.
VCC		**CARD POWER SUPPLY:** 5.0V for all internal circuitry.
GND		**GROUND:** for all internal circuitry.
REG#	INPUT	**ATTRIBUTE MEMORY SELECT :** only used with cards built with optional attribute memory.
RST	INPUT	**RESET:** Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down signal for the memory array.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V, 16 bit card has been inserted.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

Functional Truth Table

READ function

					Common Memory			***Attribute Memory***		
Function Mode	/CE2	/CE1	/OE	/WE	/REG	D15-D8	D7-D0	/REG	D15-D8	D7-D0
Standby Mode	**H**	**H**	**X**	**X**	**X**	High-Z	High-Z	**X**	High-Z	High-Z
Low Byte Access	**H**	**L**	**L**	**H**	**H**	High-Z	Even-Byte	**L**	High-Z	Even-Byte
Word Access (16 bits)	**L**	**L**	**L**	**H**	**H**	Odd-Byte	Even-Byte	**L**	Not Valid	Even-Byte
Odd-Byte Only Access	**L**	**H**	**L**	**H**	**H**	Odd-Byte	High-Z	**L**	Not Valid	High-Z

WRITE function

Standby Mode	**H**	**H**	**X**	**X**	**X**	X	X	**X**	X	X
Low Byte Access	**H**	**L**	**H**	**L**	**H**	X	Even-Byte	**L**	X	Even-Byte
Word Access (16 bits)	**L**	**L**	**H**	**L**	**H**	Odd-Byte	Even-Byte	**L**	X	Even-Byte
Odd-Byte Only Access	**L**	**H**	**H**	**L**	**H**	Odd-Byte	X	**L**	X	X

Absolute Maximum Ratings (2)

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Storage Temperature	-55°C to +110 °C
Voltage on any pin relative to VSS	-0.5V to VCC+0.5V (1)
VCC supply Voltage relative to VSS	-0.5V to +7.0V

Notes:
(1) During transitions, inputs may undershoot to -2.0V or overshoot to VCC +2.0V for periods less than 20ns.
(2) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics (1)

Symbol	Parameter	Density (Mbytes)	Notes	Typ(3)	Max	Units	Test Conditions
ICCR	VCC Read Current	2,4,8,16			75	mA	VCC = 5.25V tcycle = 100ns
ICCW	VCC Program Current	2,4,8,16			100	mA	
ICCE	VCC Erase Current	2,4,8,16			100	mA	
ICCSL	VCC Sleep Current	2,4,8	2	50	160	µA	VCC = 5.25V Control Signals = VCC Reset = VIH
ICCSL	VCC Sleep Current	16	2	90	240	µA	VCC = 5.25V Control Signals = VCC Reset = VIH
ICCS	VCC Standby Current	2,4,8,16	2	3	10	mA	VCC = 5.25V Control Signals = VCC

CMOS Test Conditions: VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

Notes:
1. All currents are for x16 mode and are RMS values unless otherwise specified.
2. Control Signals: CE_1#, CE_2#, OE#, WE#, REG#.
3. Typical: VCC = 5V, T = +25C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
ILI	Input Leakage Current	1,2		±20	µA	VCC = VCCMAX Vin =VCC or VSS
ILO	Output Leakage Current	1		±20	µA	VCC = VCCMAX Vout =VCC or VSS
VIL	Input Low Voltage	1	0	0.8	V	
VIH	Input High Voltage	1	3.85	VCC+0.5	V	
VOL	Output Low Voltage	1		0.4	V	IOL = 3.2mA
VOH	Output High Voltage	1	VCC-0.4	VCC	V	IOH = -2.0mA
VLKO	VCC Erase/Program Lock Voltage	1	2.0		V	

Notes:
1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when VIN = GND due to internal pull-up resistors. Leakage currents on RST will be <150µA when VIN=VCC due to internal pull-down resistor.

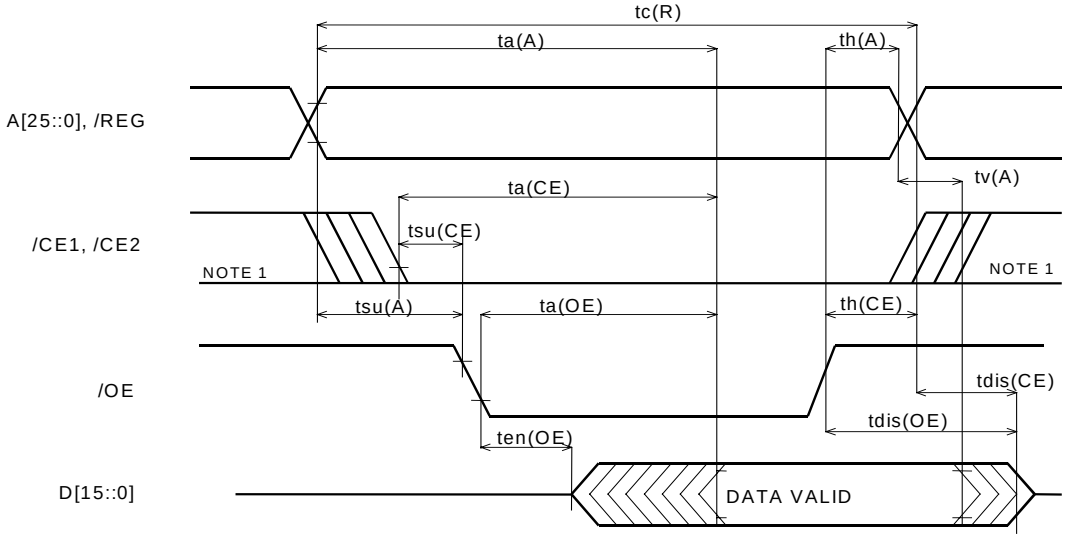
AC Characteristics

Read Timing Parameters (1)

		100ns (2)		150ns		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_C(R)	Read Cycle Time	100		150		ns
t_a(A)	Address Access Time		100		150	ns
t_a(CE)	Card Enable Access Time		100		150	ns
t_a(OE)	Output Enable Access Time		50		75	ns
t_{su}(A)	Address Setup Time		10		20	ns
t_{su}(CE)	Card Enable Setup Time		0		0	ns
t_h(A)	Address Hold Time		15		20	ns
t_h(CE)	Card Enable Hold Time		15		20	ns
t_v(A)	Output Hold from Address Change		0		0	ns
t_{dis}(CE)	Output Disable Time from CE#		50		75	ns
t_{dis}(OE)	Output Disable Time from OE#		50		75	ns
t_{en}(CE)	Output Enable Time from CE#	5		5		ns
t_{en}(OE)	Output Enable Time from OE#	5		5		ns
t_{rec}(RST)	Power Down recovery to Output Delay. VCC = 5V		500		500	ns

Notes:
1. AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.
2. Valid for cards using 8Mb components (28F008SA or 28F008S5)only. Cards based on 16Mb (28F016) are available as 150ns cards only.

Read Timing Diagram



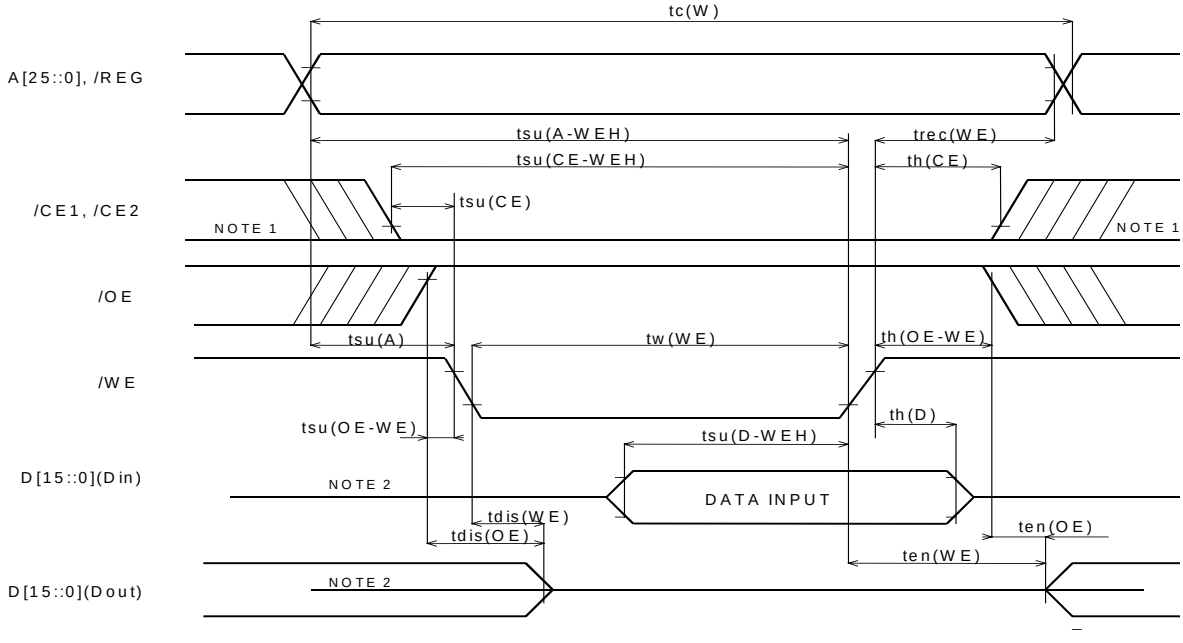
Note: Signal may be high or low in this area.

Write Timing Parameters (1)

		100ns (2)		150ns		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{CW}	Write Cycle Time	100		150		ns
t_{w}(WE)	Write Pulse Width	60		80		ns
t_{su}(A)	Address Setup Time	10		20		ns
t_{su}(A-WEH)	Address Setup Time for WE#	70		100		ns
t_{su}(CE-WEH)	Card Enable Setup Time for WE#	70		100		ns
t_{su}(D-WEH)	Data Setup Time for WE#	40		50		ns
t_{h}(D)	Data Hold Time	15		20		ns
t_{rec}(WE)	Write Recover Time	15		20		ns
t_{dis}(WE)	Output Disable Time from WE#		50		75	ns
t_{dis}(OE)	Output Disable Time from OE#		50		75	ns
t_{en}(WE)	Output Enable Time from WE#	5		5		ns
t_{en}(OE)	Output Enable Time from OE#	5		5		ns
t_{su}(OE-WE)	Output Enable Setup from WE#	10		10		ns
t_{h}(OE-WE)	Output Enable Hold from WE#	10		10		ns
t_{su}(CE)	Card Enable Setup Time from OE#	0		0		ns
t_{h}(CE)	Card Enable Hold Time	15		20		ns

Notes:
1. AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.
2. Valid for cards using 8Mb components (28F008SA or 28F008S5)only. Cards based on 16Mb (28F016) are available as 150ns cards only.

Write Timing Diagram



Notes:
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

Data Write and Erase Performance (1,3)

28F008SA Based Flash Cards

VCC = 5V ± 5%, T_A = 0C to + 60C

SYM	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	2,4		8µs	3ms		
t_{WHQV2} t_{EHQV2}	Block Program Time	2		0.4	2.1	sec	Word Program Mode
	Block Erase Time	2		0.6	10	sec	
	Full Chip Erase Time	2, 5		38.4		sec	

Notes:
1. Typical: Nominal voltages and T_A = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal or component status register should be polled.
5. Chip erase time based on 8 Mbit Flash components (28F008SA).

28F008S5 and 28F016S5 Based Flash Cards

VCC = 5V ± 5%, T_A = 0C to + 60C

SYM	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	2,4		8µs	3ms		
t_{WHQV2} t_{EHQV2}	Block Program Time	2		0.5	TBD	sec	Word Program Mode
	Block Erase Time	2		1.1	TBD	sec	
	Full Chip Erase Time	2, 5		38.4		sec	

Notes:
1. Typical: Nominal voltages and T_A = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal or component status register should be polled.
5. Chip erase time based on 8 Mbit Flash components (28F008S5).

PRODUCT MARKING

WED 7P016FVA0600C15 C995 9915

- **EDI** — Company Name
- **7P016FVA0600C15** — Part number
- **C995** — Lot code / trace number
- **9915** — Date code

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING

7 P 016 FVA06 00 C 15

Card access time

15	150ns
25	250ns

Temperature range

C	Commercial	0°C to +70°C
I	Industrial	-40°C to +85°C

Packaging option

00	Standard, type 1

Card family and version

- See Card Family and Version Info. for details (next page)

Card capacity

016	16MB

PC card

P	Standard PCMCIA
R	Ruggedized PCMCIA

Card technology

7	FLASH
8	SRAM

Ordering Information

7P XXX FVA YY SS T ZZ

where

XXX:	**002**	**2MB**
	004	**4MB**
	008	**8MB**
	016	**16MB (uses 28F016S5 only)**
YY:	**01**	**28F008SA base**
	02	**28F008SA w/attribute memory**
	03	**28F008S5 base**
	04	**28F008S5 w/attribute memory**
	05	**28F016S5 base**
	06	**28F016S5 w/attribute memory**
SS:	**00**	**WEDC Silkscreen**
	01	**Blank Housing, Type I**
	02	**Blank Housing, Type I Recessed**
T:	**C**	**Commercial**
	I	**Industrial**
ZZ:	**10**	**100ns**
	15	**150ns**

Part Number Table - Common Options

WEDC Part Number	Density	Speed	Flash Component	Attribute Memory
Intel/Sharp Based Cards				
EDI7P002FVA0100C10	2MB	100ns	28F008SA	NO
EDI7P002FVA0100C15	2MB	150ns	28F008SA	NO
EDI7P002FVA0300C10	2MB	100ns	28F008S5	NO
EDI7P002FVA0300C15	2MB	150ns	28F008S5	NO
EDI7P002FVA0200C10	2MB	100ns	28F008SA	2K EEPROM
EDI7P002FVA0200C15	2MB	150ns	28F008SA	2K EEPROM
EDI7P002FVA0400C10	2MB	100ns	28F008S5	2K EEPROM
EDI7P002FVA0400C15	2MB	150ns	28F008S5	2K EEPROM
EDI7P004FVA0300C15	4MB	150ns	28F016S5	NO
EDI7P004FVA0400C15	4MB	150ns	28F016S5	2K EEPROM
EDI7P008FVA0300C15	8MB	150ns	28F016S5	NO
EDI7P008FVA0400C15	8MB	150ns	28F016S5	2K EEPROM
EDI7P016FVA0500C15	16MB	150ns	28F016S5	NO
EDI7P016FVA0600C15	16MB	150ns	28F016S5	2K EEPROM

Notes:
1. Cards built with 16Mb devices are not available in 100ns speed grade.
2. Other options, including density, architecture and speed are available, please contact your WEDC sales representative with your request.

CIS Data - Cards Based on 28F008SA Components with Attribute Memory

Address	Value	Description
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**54H**	FLASH = 100ns (device writable)
	53H	FLASH = 150ns (device writable)
06H	**06H**	CARD SIZE: 2MB
	0EH	4MB
	1EH	8MB
08H	**FFH**	END OF DEVICE
0AH	**18H**	**CISTPL_JEDEC_A**
0CH	**02H**	TPL_LINK
0EH	**89H**	INTEL - ID
10H	**A2H**	INTEL 28F008SA - ID
12H	**17H**	**CISTPL_DEVICE_A**
14H	**03H**	TPL_LINK
16H	**42H**	EEPROM - 200ns
18H	**01H**	Device Size = 2KBytes
1AH	**FFH**	END OF TUPLE
1CH	**1EH**	**CISTPL_DEVICEGEO**
1EH	**06H**	TPL_LINK
20H	**02H**	DGTPL_BUS
22H	**11H**	DGTPL_EBS
24H	**01H**	DGTPL_RBS
26H	**01H**	DGTPL_WBS
28H	**01H**	DGTPL_PART
2AH	**01H**	FLASH DEVICE NON-INTERLEAVED
2CH	**20H**	**CISTPL_MANFID**
2EH	**04H**	TPL_LINK(04H)
30H	**F6H**	**EDI** TPLMID_MANF: LSB
32H	**01H**	**EDI** TPLMID_MANF: MSB
34H	**00H**	*LSB: Number Not Assigned*
36H	**00H**	*MSB: Number Not Assigned*
38H	**15H**	**CISTPL_VERS1**
3AH	**4AH**	TPL_LINK
3CH	**05H**	TPLLV1_MAJOR
3EH	**00H**	TPLLV1_MINOR
40H	**45H**	E
42H	**44H**	D
44H	**49H**	I
46H	**37H**	7
48H	**50H**	P
4AH	**30H**	0
4CH	**30H**	0
4EH		*x*
50H	**46H**	F
52H	**56H**	V
54H	**41H**	A
56H	**30H**	0
58H	**32H**	2
5AH	**2DH**	-
5CH	**2DH**	-
5EH	**2DH**	-
60H		*y*
62H		*y*

Address	Value	Description
64H	**20H**	SPACE
66H	**00H**	END TEXT
68H	**43H**	C
6AH	**4FH**	O
6CH	**50H**	P
6EH	**59H**	Y
70H	**52H**	R
72H	**49H**	I
74H	**47H**	G
76H	**48H**	H
78H	**54H**	T
7AH	**20H**	SPACE
7CH	**45H**	E
7EH	**4CH**	L
80H	**45E**	E
82H	**43H**	C
84H	**54H**	T
86H	**52H**	R
88H	**4FH**	O
8AH	**4EH**	N
8CH	**49H**	I
8EH	**43H**	C
90H	**20H**	SPACE
92H	**44H**	D
94H	**45H**	E
96H	**53H**	S
98H	**49H**	I
9AH	**47H**	G
9CH	**4EH**	N
9EH	**53H**	S
A0H	**20H**	SPACE
A2H	**49H**	I
A4H	**4EH**	N
A6H	**43H**	C
A8H	**4FH**	O
AAH	**52H**	R
ACH	**50H**	P
AEH	**4FH**	O
B0H	**52H**	R
B2H	**41H**	A
B4H	**54H**	T
B6H	**45H**	E
B8H	**44H**	D
BAH	**20H**	SPACE
BCH	**00H**	END TEXT
BEH	**31H**	1
C0H	**39H**	9
C2H	**39H**	9
C4H	**37H**	7
C6H	**00H**	END TEXT
C8H	**FFH**	END OF LIST
CAH	**FFH**	**CISTPL_END**
CCH	**00H**	INVALID ADDRESS

Note: In the part number, value *x* will be substituted with the proper capacity and value *yy* with the proper card speed.

CIS Data - Cards Based on 28F008S5 Components with Attribute Memory

Address	Value	Description
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**54H**	FLASH = 100ns (device writable)
	53H	FLASH = 150ns (device writable)
06H	**06H**	CARD SIZE: 2MB
	0EH	4MB
	1EH	8MB
08H	**FFH**	END OF DEVICE
0AH	**18H**	**CISTPL_JEDEC_C**
0CH	**02H**	TPL_LINK
0EH	**89H**	INTEL - ID
10H	**A6H**	INTEL 28F008S5 - ID
12H	**17H**	**CISTPL_DEVICE_A**
14H	**03H**	TPL_LINK
16H	**42H**	EEPROM - 200ns
18H	**01H**	Device Size = 2KBytes
1AH	**FFH**	END OF TUPLE
1CH	**1EH**	**CISTPL_DEVICEGEO**
1EH	**06H**	TPL_LINK
20H	**02H**	DGTPL_BUS
22H	**11H**	DGTPL_EBS
24H	**01H**	DGTPL_RBS
26H	**01H**	DGTPL_WBS
28H	**01H**	DGTPL_PART
2AH	**01H**	FLASH DEVICE NON-INTERLEAVED
2CH	**20H**	**CISTPL_MANFID**
2EH	**04H**	TPL_LINK(04H)
30H	**F6H**	**EDI** TPLMID_MANF: LSB
32H	**01H**	**EDI** TPLMID_MANF: MSB
34H	**00H**	*LSB: Number Not Assigned*
36H	**00H**	*MSB: Number Not Assigned*
38H	**15H**	**CISTPL_VERS1**
3AH	**47H**	TPL_LINK
3CH	**05H**	TPLLV1_MAJOR
3EH	**00H**	TPLLV1_MINOR
40H	**45H**	E
42H	**44H**	D
44H	**49H**	I
46H	**37H**	7
48H	**50H**	P
4AH	**30H**	0
4CH	**30H**	0
4EH		*x*
50H	**46H**	F
52H	**56H**	V
54H	**41H**	A
56H	**30H**	0
58H	**34H**	4
5AH	**2DH**	-
5CH	**2DH**	-
5EH	**2DH**	-
60H		*y*
62H		*y*

Address	Value	Description
64H	**20H**	SPACE
66H	**00H**	END TEXT
68H	**43H**	C
6AH	**4FH**	O
6CH	**50H**	P
6EH	**59H**	Y
70H	**52H**	R
72H	**49H**	I
74H	**47H**	G
76H	**48H**	H
78H	**54H**	T
7AH	**20H**	SPACE
7CH	**45H**	E
7EH	**4CH**	L
80H	**45E**	E
82H	**43H**	C
84H	**54H**	T
86H	**52H**	R
88H	**4FH**	O
8AH	**4EH**	N
8CH	**49H**	I
8EH	**43H**	C
90H	**20H**	SPACE
92H	**44H**	D
94H	**45H**	E
96H	**53H**	S
98H	**49H**	I
9AH	**47H**	G
9CH	**4EH**	N
9EH	**53H**	S
A0H	**20H**	SPACE
A2H	**49H**	I
A4H	**4EH**	N
A6H	**43H**	C
A8H	**4FH**	O
AAH	**52H**	R
ACH	**50H**	P
AEH	**4FH**	O
B0H	**52H**	R
B2H	**41H**	A
B4H	**54H**	T
B6H	**45H**	E
B8H	**44H**	D
BAH	**20H**	SPACE
BCH	**00H**	END TEXT
BEH	**31H**	1
C0H	**39H**	9
C2H	**39H**	9
C4H	**37H**	7
C6H	**00H**	END TEXT
C8H	**FFH**	END OF LIST
CAH	**FFH**	**CISTPL_END**
CCH	**00H**	INVALID ADDRESS

Note: In the part number, value *x* will be substituted with the proper capacity and value *yy* with the proper card speed.

CIS Data - Cards Based on 28F016S5 Components with Attribute Memory

Address	Value	Description
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**53H**	FLASH = 150ns (device writable)
06H	**0EH**	CARD SIZE: 4MB
	1EH	8MB
	3EH	16MB
08H	**FFH**	END OF DEVICE
0AH	**18H**	**CISTPL_JEDEC_C**
0CH	**02H**	TPL_LINK
0EH	**89H**	INTEL - ID
10H	**AAH**	28F016S5 - ID
12H	**17H**	**CISTPL_DEVICE_A**
14H	**03H**	TPL_LINK
16H	**42H**	EEPROM - 200ns
18H	**01H**	Device Size = 2KBytes
1AH	**FFH**	END OF TUPLE
1CH	**1EH**	**CISTPL_DEVICEGEO**
1EH	**06H**	TPL_LINK
20H	**02H**	DGTPL_BUS
22H	**11H**	DGTPL_EBS
24H	**01H**	DGTPL_RBS
26H	**01H**	DGTPL_WBS
28H	**01H**	DGTPL_PART
2AH	**01H**	FLASH DEVICE NON-INTERLEAVED
2CH	**20H**	**CISTPL_MANFID**
2EH	**04H**	TPL_LINK(04H)
30H	**F6H**	**EDI** TPLMID_MANF: LSB
32H	**01H**	**EDI** TPLMID_MANF: MSB
34H	**00H**	*LSB: Number Not Assigned*
36H	**00H**	*MSB: Number Not Assigned*
38H	**15H**	**CISTPL_VERS1**
3AH	**47H**	TPL_LINK
3CH	**05H**	TPLLV1_MAJOR
3EH	**00H**	TPLLV1_MINOR
40H	**45H**	E
42H	**44H**	D
44H	**49H**	I
46H	**37H**	7
48H	**50H**	P
4AH	**30H**	0
4CH	**30H**	0
4EH		*x*
50H	**46H**	F
52H	**56H**	V
54H	**41H**	A
56H	**30H**	0
58H	**36H**	6
5AH	**2DH**	-
5CH	**2DH**	-
5EH	**2DH**	-
60H		*y*
62H		*y*

Address	Value	Description
64H	**20H**	SPACE
66H	**00H**	END TEXT
68H	**43H**	C
6AH	**4FH**	O
6CH	**50H**	P
6EH	**59H**	Y
70H	**52H**	R
72H	**49H**	I
74H	**47H**	G
76H	**48H**	H
78H	**54H**	T
7AH	**20H**	SPACE
7CH	**45H**	E
7EH	**4CH**	L
80H	**45E**	E
82H	**43H**	C
84H	**54H**	T
86H	**52H**	R
88H	**4FH**	O
8AH	**4EH**	N
8CH	**49H**	I
8EH	**43H**	C
90H	**20H**	SPACE
92H	**44H**	D
94H	**45H**	E
96H	**53H**	S
98H	**49H**	I
9AH	**47H**	G
9CH	**4EH**	N
9EH	**53H**	S
A0H	**20H**	SPACE
A2H	**49H**	I
A4H	**4EH**	N
A6H	**43H**	C
A8H	**4FH**	O
AAH	**52H**	R
ACH	**50H**	P
AEH	**4FH**	O
B0H	**52H**	R
B2H	**41H**	A
B4H	**54H**	T
B6H	**45H**	E
B8H	**44H**	D
BAH	**20H**	SPACE
BCH	**00H**	END TEXT
BEH	**31H**	1
C0H	**39H**	9
C2H	**39H**	9
C4H	**37H**	7
C6H	**00H**	END TEXT
C8H	**FFH**	END OF LIST
CAH	**FFH**	**CISTPL_END**
CCH	**00H**	INVALID ADDRESS

Note: In the part number, value *x* will be substituted with the proper capacity and value *yy* with the proper card speed.

Revision History

revision	rev date	description
0	Jan-98	initial release
1	Jun-99	logo/name change
2	May-00	added pg. 8
3	Aug-00	changed pg. 5&6

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