3.3 V SDRAM Modules

144-pin SO-DIMM SDRAM Modules
PC100/PC133
32 MB & 64 MB Density

- 144-pin Eight Byte Small Outline Dual-In-Line Synchronous DRAM Modules for PC 100 and PC133 notebook applications
- One bank 4M × 64, two bank 8M × 64 non-parity module organization
- Single + 3.3 V (± 0.3 V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- Performance:
- All inputs and outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Uses 4M × 16 SDRAM components
- 4096 refresh cycles every 64 ms
- Gold contact pad
- This module family is fully compliant with the latest INTEL SO-DIMM layout specification

		-7.5	-8	Unit
		PC133 3-3-3	PC100 2-2-2	
f_{CK}	Clock Frequency (max.)	133	100	MHz
t_{AC}	Clock Access Time $\overline{\text{CAS}}$ latency = 2 & 3	5.4	6	ns

This Infineon module family are industry standard 144-pin 8-byte Synchronous DRAM (SDRAM) Small Outline Dual In-line Memory Modules (SO-DIMM) which are organized as x64 high speed memory arrays designed for use in non-parity applications. These SO-DIMMs use SDRAMs in TSOPII packages. Decoupling capacitors are mounted on the board.

The DIMMs use serial presence detects implemented via a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All Infineon 144-pin SO-DIMMs provide a high performance, flexible 8-byte interface in a 67.5 mm long footprint.

Product Sprectrum

Organi-zation	Partnumber	SDRAMs Used	Row Addr.	Bank Select	Column Addr.	Refresh	Period
4M × 64	HYS 64V4200GDL-7.5	4 4M × 16	12	BA0, BA1	8	4k	64 ms
4M × 64	HYS 64V4200GDL-8	4 4M × 16	12	BA0, BA1	8	4k	64 ms
8M × 64	HYS 64V8220GDL-7.5	8 4M × 16	12	BA0, BA1	8	4k	64 ms
8M × 64	HYS 64V8220GDL-8	8 4M × 16	12	BA0, BA1	8	4k	64 ms

Note: All part numbers end with a place code (not shown), designating the die revision. Consult factory for current revision. Example: HYS 64V8220GDL-8-B, indicating Rev.B dies are used for SDRAM components.

Card Dimensions

Organization	PCB-Board	L × H × T [mm]
4M × 64	Intel Rev. 1.0	67.60 × 25.40 × 3.80
8M × 64	Intel Rev. 1.0	67.60 × 31.75 × 3.80

Pin Definitions and Functions

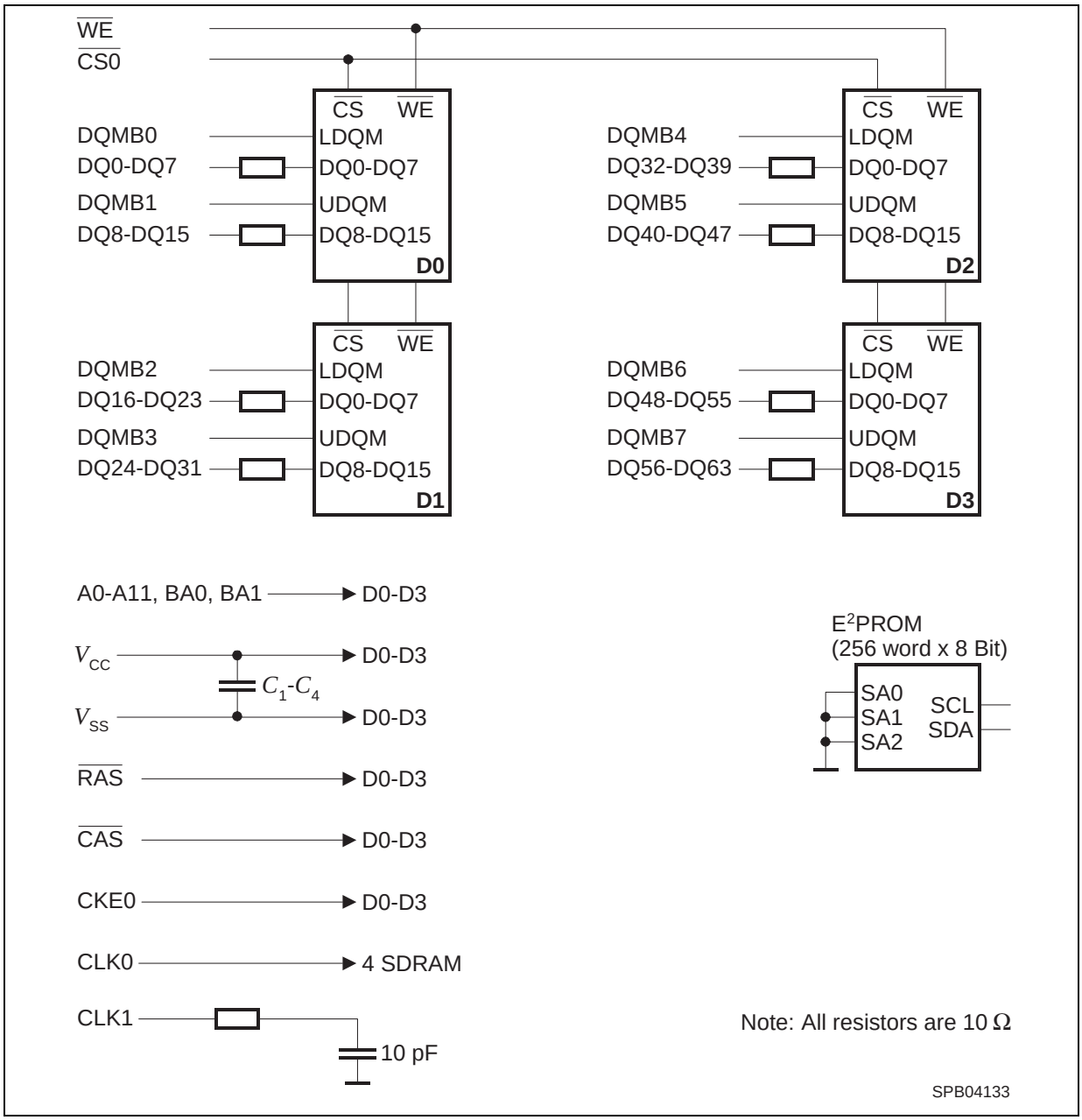
A0 - A11	Address Inputs for 4M × 64 & 8M × 64 modules	DQMB0 - DQMB7	Data Mask
BA0, BA1	Bank Selects for 4M × 64, 8M × 64 & 16M × 64 modules	$\overline{CS0}$ - $\overline{CS3}$	Chip Select
DQ0 - DQ63	Data Input/Output	V_{DD}	Power (+ 3.3 Volt)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read/Write Input	SDA	Serial Data Out for Presence Detect
CKE0	Clock Enable	N.C.	No Connection
CLK0	Clock Input	–	–

Pin Configuration

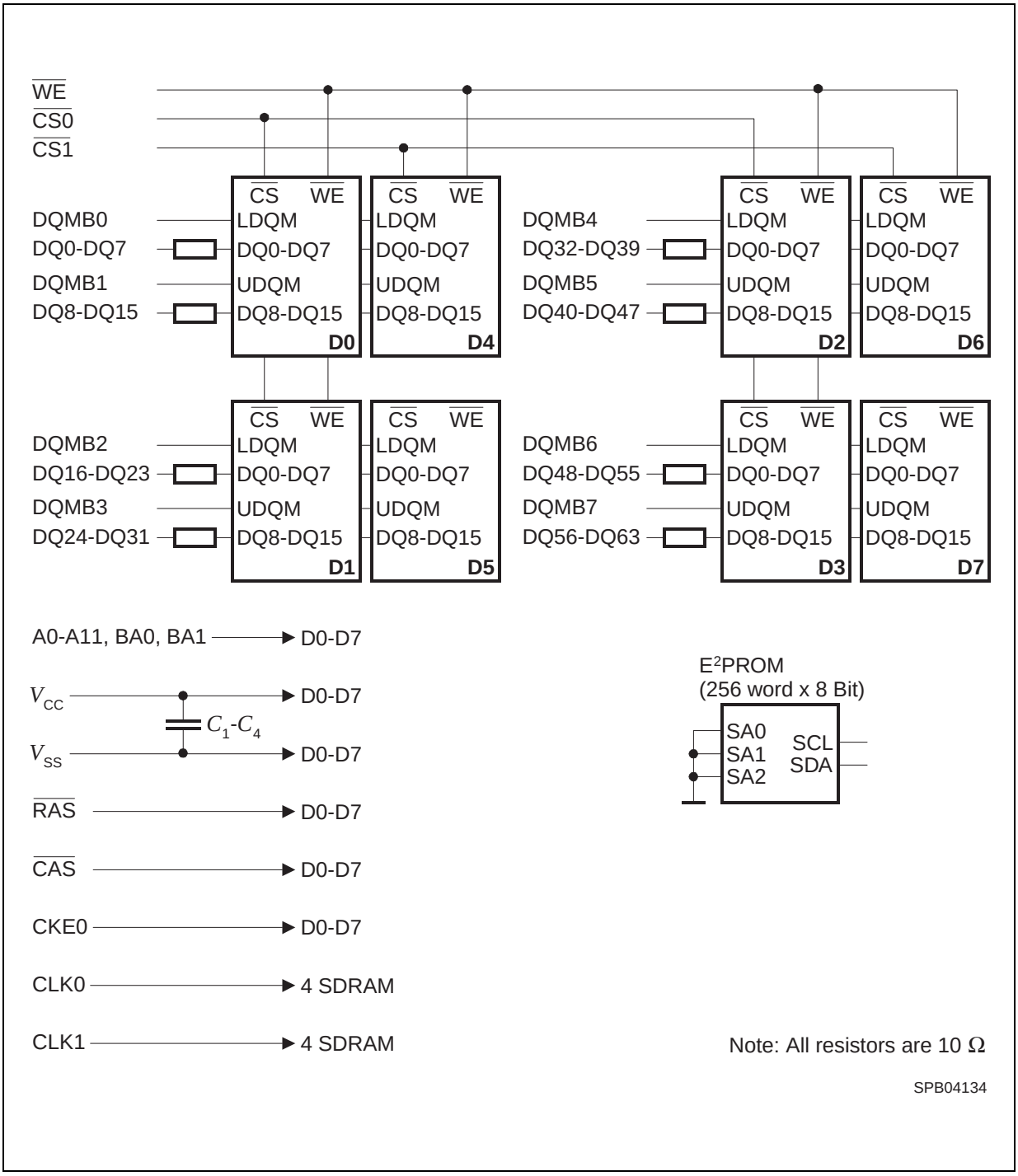
PIN#	Front Side	PIN#	Back Side	PIN#	Front Side	PIN#	Back Side
1	V_{SS}	2	V_{SS}	73	N.C.	74	CLK1
3	DQ0	4	DQ32	75	V_{SS}	76	V_{SS}
5	DQ1	6	DQ33	77	N.C.	78	N.C.
7	DQ2	8	DQ34	79	N.C.	80	N.C.
9	DQ3	10	DQ35	81	V_{DD}	82	V_{DD}
11	V_{DD}	12	V_{DD}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V_{SS}	92	V_{SS}
21	V_{SS}	22	V_{SS}	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	V_{DD}	28	V_{DD}	99	DQ23	100	DQ55
29	A0	30	A3	101	V_{DD}	102	V_{DD}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	V_{SS}	36	V_{SS}	107	V_{SS}	108	V_{SS}
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	V_{DD}	114	V_{DD}
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	V_{DD}	46	V_{DD}	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	V_{SS}	120	V_{SS}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	V_{SS}	56	V_{SS}	127	DQ27	128	DQ59
57	N.C.	58	N.C.	129	V_{DD}	130	V_{DD}
59	N.C.	60	N.C.	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	V_{DD}	64	V_{DD}	135	DQ30	136	DQ62
65	$\overline{RAS}$	66	$\overline{CAS}$	137	DQ31	138	DQ63

Pin Configuration (cont'd)

PIN#	Front Side	PIN#	Back Side	PIN#	Front Side	PIN#	Back Side
67	$\overline{WE}$	68	CKE1	139	V_{SS}	140	V_{SS}
69	$\overline{CS0}$	70	(A12)	141	SDA	142	SCL
71	$\overline{CS1}$	72	(A13)	143	V_{DD}	144	V_{DD}



Block Diagram: 4M × 64 SDRAM DIMM Module



Block Diagram: Two Bank 8M × 64 SDRAM DIMM Module

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5	0.8	V
Output High Voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V
Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 20	20	µA
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 20	20	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		4M × 64 max.	8M × 64 max.	
Input Capacitance (A0 to A11, BA0, BA1)	C_{I1}	28	52	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0)	C_{I2}	25	46	pF
Input Capacitance (CLK0, CLK1)	C_{I3}	35	35	pF
Input Capacitance ($\overline{CS0}$)	C_{I4}	25	30	pF
Input Capacitance (DQMB0 - DQMB7)	C_{I5}	10	15	pF
Input/Output Capacitance (DQ0 - DQ63)	C_{IO}	12	18	pF
Input Capacitance (SCL, SA0 - 2)	C_{SC}	8	8	pF
Input/Output Capacitance	C_{SD}	10	8	pF

Operating Currents per Memory Bank
T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.3 V
(Recommended Operating Conditions unless otherwise noted)

Parameter	Test Condition	Symbol	-7.5	-8	Unit	Note
Operating current $t_{RC} = t_{RC(MIN.)}$, $t_{CK} = t_{CK(MIN.)}$ Outputs open, Burst Length = 4, CL = 3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	–	I_{CC1}	560	520	mA	1)
Precharge stand-by current in Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, CKE ≤ $V_{IL(MAX.)}$	t_{CK} = min.	I_{CC2P}	8	8	mA	1)
	t_{CK} = infinity	I_{CC2PS}	4	4	mA	1)
Precharge Stand-by Current in Non-Power Down Mode $\overline{CS} = V_{IH\ (MIN.)}$, CKE ≥ $V_{IH(MIN.)}$	t_{CK} = min.	I_{CC2N}	160	140	mA	1)
	t_{CK} = infinity	I_{CC2NS}	20	20	mA	1)
No operating current t_{CK} = min., $\overline{CS} = V_{IH(MIN.)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	200	180	mA	1)
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}	32	32	mA	1)
Burst operating current t_{CK} = min., Read command cycling	–	I_{CC4}	440	400	mA	1), 2)
Auto refresh current t_{CK} = min., Auto Refresh command cycling	–	I_{CC5}	560	520	mA	1)
Self refresh current Self Refresh Mode, CKE = 0.2 V	L-version	I_{CC6}	2	2	mA	1)

Notes

1. These parameters depend on the cycle rate. These values are measured at 133 MHz for -7.5 parts, 100 MHz for -8 parts, and at 66 MHz for -10 parts. Input signals are changed once during t_{CK}, excepts for I_{CC6} and for standby currents when t_{CK} = infinity.
2. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 are assumed and the V_{DDQ} current is excluded.

AC Characteristics [1), 2)]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

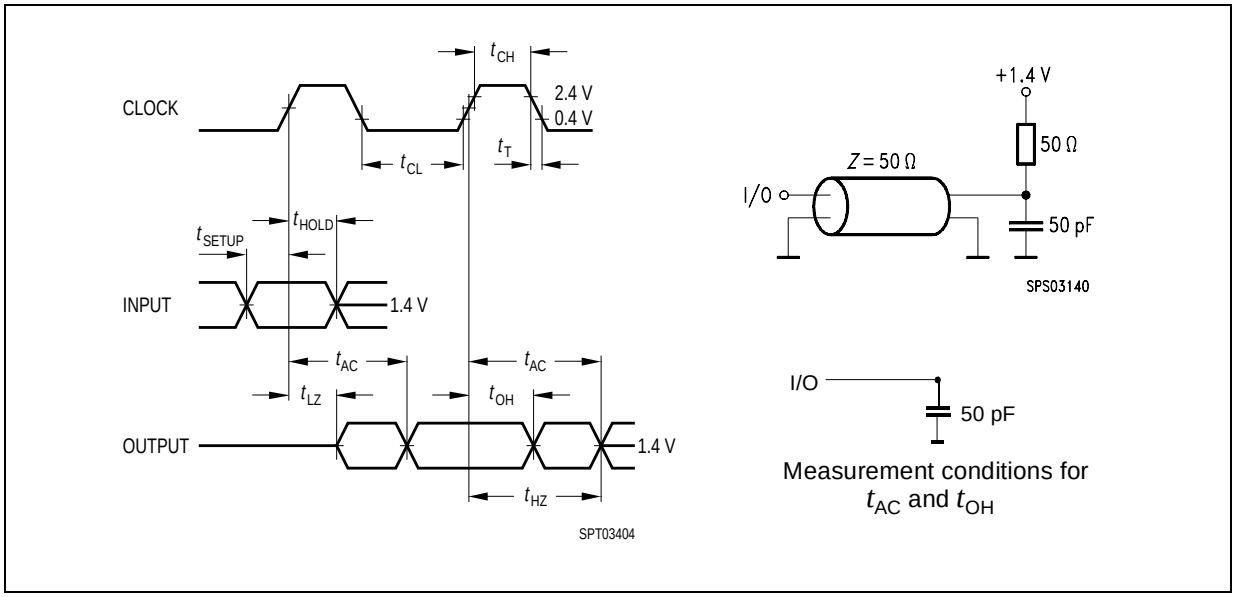
Parameter	Symbol	Limit Values				Unit	Note
		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.		
Clock and Clock Enable							
Clock Cycle Time	t_{CK}						–
$\overline{CAS}$ Latency = 3		7.5	–	10	–	ns	
$\overline{CAS}$ Latency = 2		10	–	10	–	ns	
Clock Frequency	f_{CK}						–
$\overline{CAS}$ Latency = 3		–	133	–	100	MHz	
$\overline{CAS}$ Latency = 2		–	100	–	100	MHz	
Access Time from Clock	t_{AC}						2), 3)
$\overline{CAS}$ Latency = 3		–	5.4	–	6	ns	
$\overline{CAS}$ Latency = 2		–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	3	–	ns	–
Clock Low Pulse Width	t_{CL}	2.5	–	3	–	ns	–
Transition Time	t_T	0.3	1.2	0.5	10	ns	–
Setup and Hold Times							
Input Setup Time	t_{IS}	1.5	–	2	–	ns	4)
Input Hold Time	t_{IH}	0.8	–	1	–	ns	4)
Power Down Mode Entry Time	t_{SB}	–	1	–	1	CLK	4)
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	CLK	4)
Mode Register Set-up Time	t_{RSC}	2	–	2	–	CLK	–
Common Parameters							
Row to Column Delay Time	t_{RCD}	20	–	20	–	ns	5)
Row Precharge Time	t_{RP}	20	–	20	–	ns	5)
Row Active Time	t_{RAS}	45	100k	50	100k	ns	5)
Row Cycle Time	t_{RC}	67	–	70	–	ns	5)
Activate (a) to Activate (b) Command Period	t_{RRD}	14	–	16	–	ns	5)
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period	t_{CCD}	1	–	1	–	CLK	–

AC Characteristics (cont'd) [1), 2)]
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.		
Refresh Cycle							
Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	ms	–
Self Refresh Exit Time	t_{SREX}	1	–	1	–	CLK	6)
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	–
Data Out to Low Impedance Time	t_{LZ}	1	–	0	–	ns	–
Data Out to High Impedance Time	t_{HZ}	3	7	3	8	ns	7)
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	CLK	–
Write Cycle							
Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	–

Notes

1. An initial pause of 100 µs is required after power-up. Then, a Precharge All Banks command must be given, followed by eight Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.
3. If clock rising time is longer than 1 ns, a time (t_T – 0.5) ns must be added to this parameter.
4. If t_T is longer than 1 ns, a time (t_T – 1) ns must be added to this parameter.
5. Whenever the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to “wake-up” the device.
6. Self Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied after the Self Refresh Exit command is registered.
7. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.



A serial presence detect storage device - E^{2}PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^{2}PROM device during module production using a serial presence detect protocol (I^{2}C synchronous 2-wire bus).

SPD-Table

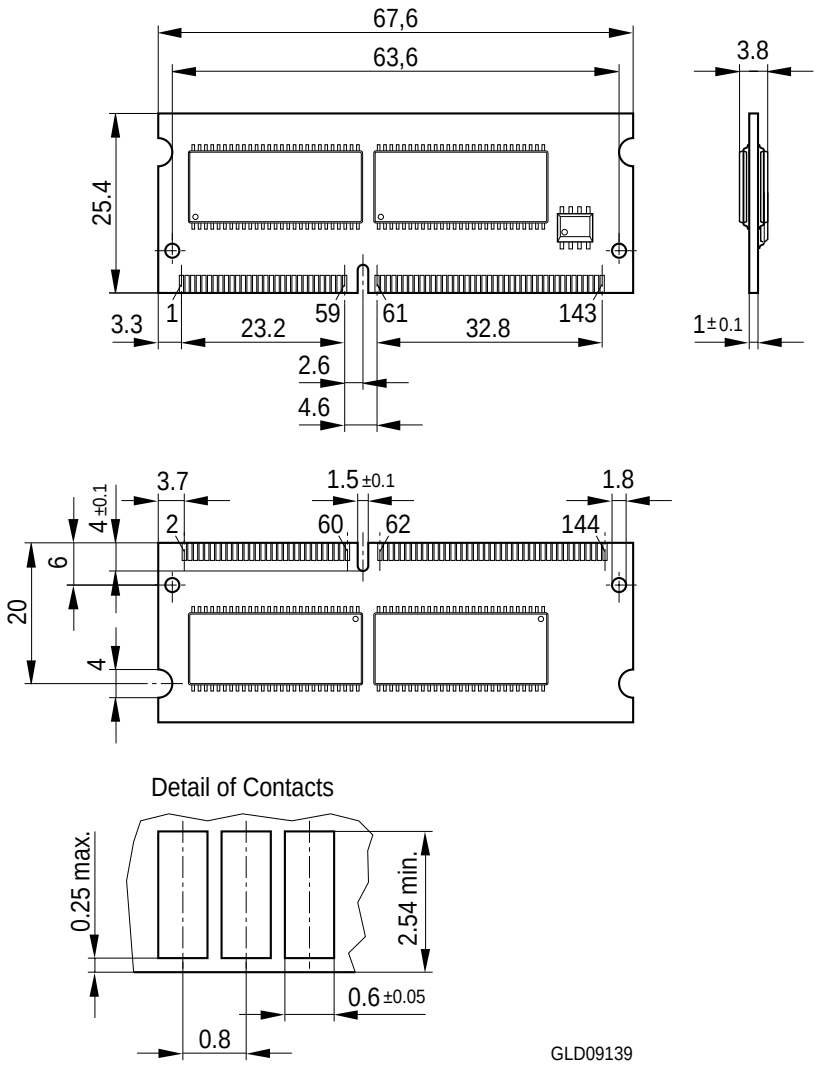
Byte#	Description	SPD Entry Value	Hex			
			4M × 64 -7.5	8M × 64 -10	4M × 64 -8	8M × 64 -8
0	Number of SPD Bytes	128	80			
1	Total Bytes in Serial PD	256	08			
2	Memory Type	SDRAM	04			
3	Number of Row Addresses (without BS)	–	0C			
4	Number of Column Addresses	–	08			
5	Number of DIMM Banks	1	01	02	01	02
6	Module Data Width	64	40			
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	LVTTL	01			
9	SDRAM Cycle Time at CL = 3	7.5/10.0 ns	75	75	A0	A0
10	SDRAM Access Time from Clock at CL = 3	5.4/6.0 ns	54	54	60	60
11	DIMM Config (Error Det/Corr.)	none	00			
12	Refresh Rate/Type	Self-Refresh, 15.6 µs	80			
13	SDRAM Width, Primary	–	10			
14	Error Checking SDRAM Data Width	n/a/x8	00			
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01			
16	Burst Length Supported	1, 2, 4, 8 & full page	8F			
17	Number of SDRAM Banks	2	04			
18	Supported $\overline{CAS}$ Latencies	2 & 3	06			
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01			
20	$\overline{WE}$ Latencies	Write latency = 0	01			
21	SDRAM DIMM Module Attributes	non buffered/non reg.	00			
22	SDRAM Device Attributes: General	V_{DD} tol +/– 10%	0E			
23	SDRAM Cycle Time at CL = 2	10.0 ns	A0	A0	A0	A0
24	SDRAM Access Time from Clock at CL = 2	6.0 ns	60	60	60	60
25	SDRAM Cycle Time at CL = 1	not supported	FF			
26	SDRAM Access Time from Clock at CL = 1	not supported	FF			
27	Minimum Row Precharge Time	20 ns	14			
28	Minimum Row Active to Row Active Delay	14/16 ns	0F	0F	10	10
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	20 ns	14			
30	Minimum $\overline{RAS}$ Pulse Width	45 ns	2D			
31	Module Bank Density (per bank)	32 MB	08			
32	SDRAM Input Setup Time	1.5/2 ns	15	15	20	20
33	SDRAM Input Hold Time	0.8/1 ns	08	08	10	10

SPD-Table (cont'd)

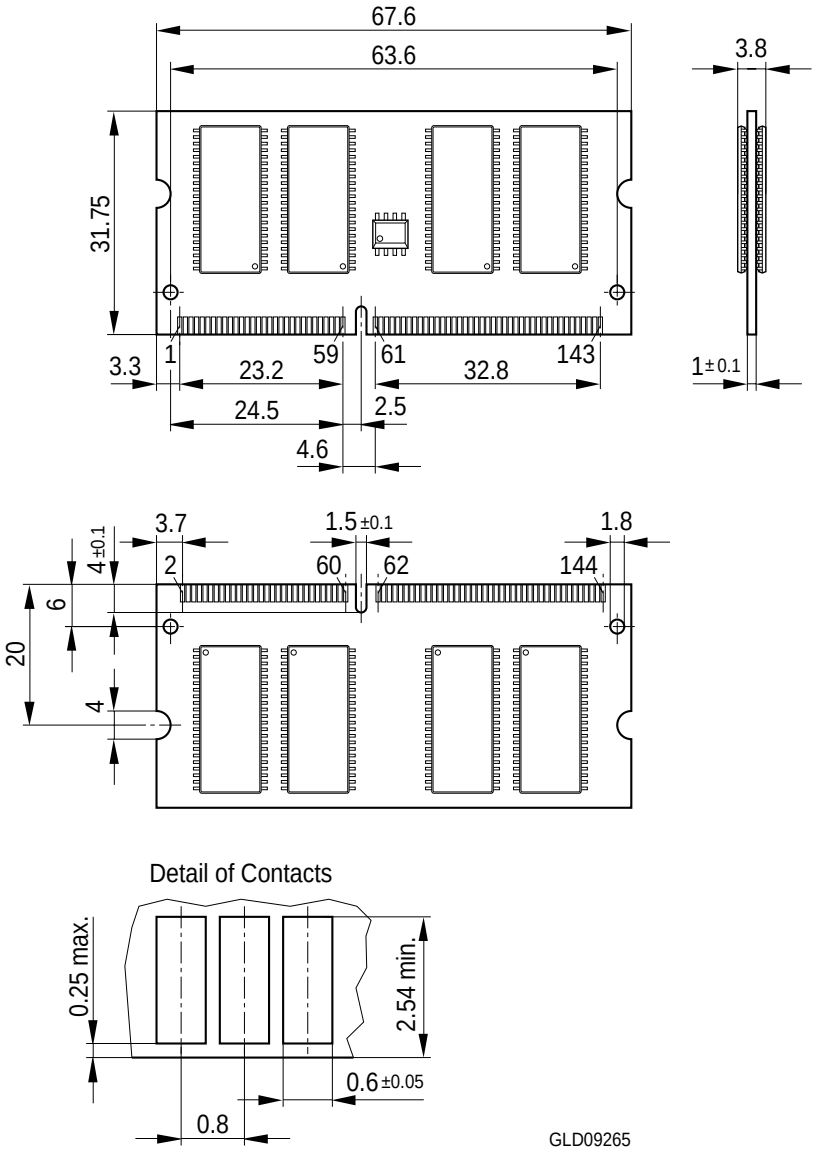
Byte#	Description	SPD Entry Value	Hex			
			4M × 64 -7.5	8M × 64 -10	4M × 64 -8	8M × 64 -8
34	SDRAM Data Input Setup Time	1.5/2 ns	15	15	20	20
35	SDRAM Data Input Hold Time	0.8/1 ns	08	08	10	10
36-61	Superset Information	–	FF			
62	SPD Revision	Revision 1.2	12			
63	Checksum for Bytes 0 - 62	–	81	82	DF	E0
64-125	Manufactures's Information (optional)	–	FF			
126	Frequency Specification		64	64	64	64
127	Details	–	87	C7	87	C7
128+	Unused Storage Locations	–	FF			

Package Outlines

32 MByte SO-DIMM Module Package
(144-pin, Dual Read-out, Single In-line Memory Module)



64 MByte SO-DIMM Module Package
(144-pin, Dual Read-out, Single In-line Memory Module)



Update Information:

5.8.99	Input/Output Capacitance values adjusted according to latest measurements
8.9.99	Templeate from R&L
3.12.99	PC133 timing parameters changed according to INTEL'S PC133 specification