LSI LOGIC CORPORATION

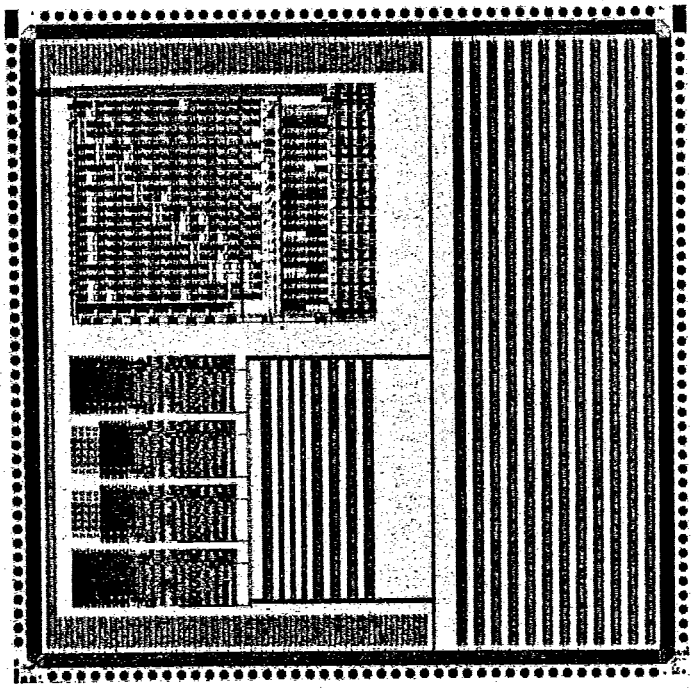
LSA2011 Two Micron HCMOS Structured Array™

General Description

The LSA2011 is a member of the 2-micron drawn, (1.4-micron effective) HCMOS family of Structured Arrays offered by LSI Logic Corporation. These very high performance, Application Specific Integrated Circuits (ASICs) combine special purpose silicon structures, optimized for performance with general purpose logic arrays on a single chip. Structured Arrays provide a high density of logic functionality while maintaining the flexibility of design and fast turn-around of metal mask programmable logic-arrays. The use of dual layer metal interconnect technology provides high speed, high packing density, ease of layout and the ability to configure megacell architectures at the interconnect level.

Contains The Following Structures:

- 5700 gate LL 7000 Series type 2-micron drawn (1.4-micron effective) gate length HCMOS logic array
- 16 x 16-bit Multiplier-Accumulator (MAC)
  - Performs function $\overline{Z} = \overline{X} * \overline{Y} + \overline{C} + \overline{D} + \overline{SUB}$
  - Supports two's complement, unsigned and mixed mode inputs
  - Provides two separate, metal configurable accumulator/adder inputs ($\overline{C}$ and $\overline{D}$)
  - Full 36-bit accumulator and product register
  - Supports both positive and negative product accumulation
  - HOLD input on product register disables clock
  - Built-in scan/signature analysis testability
  - Programmable output buffers
- Four 2901 bit slice microprocessor/ALUs.
  - Available as four individual four bit slices
  - Each slice contains 16 or 32 general purpose registers
  - Shift pins available for cascading slices
  - Full built-in scan testing
  - Programmable output buffers

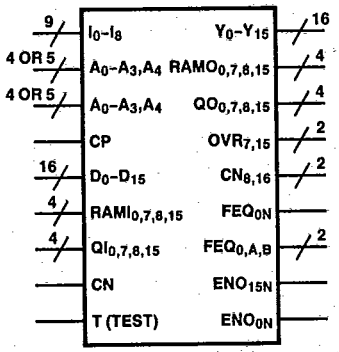


LSA2011 Pad Statistics

Max Pads[1]		Max I/O Pads[1]		Max Package Pins[2]	
Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic
172	228	156	212	178	224

Notes:
1. The difference between the maximum number of pads and I/Os is the number of dedicated V_{DD} or V_{SS} pads. It may be necessary to configure additional I/O pads for V_{DD}/V_{SS}, depending on the number and drive of the output buffers.
2. LSI Logic recommends that all LSA2011 designs be configured for use in plastic packages, thus permitting upward compatibility to ceramic packages, where required. Does not apply to military designs.

16-Pin 2901 Functional Pinout



16 x 16 MAC AC Switching Characteristics

Parameter	Description	Typ
t_{MA}	Any input to CK1	64ns
t_{OD}	CK1 to $P_{0:35}$	12ns

Typ or typical specifications are stated for operation at 25°C, 5V, nominal processing.

Available Packages

Ceramic Pin Grid Array—64, 68, 84, 100, 120, 132, 144, 180, 224 pins
Plastic Pin Grid Array—68, 84, 100, 120, 132, 144, 180 pins
Ceramic Chip Carrier (Leaded and Leadless)—68, 84, 100, 132 pins
Plastic Chip Carrier (J-bend)—68, 84 pins

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May 1986
Order No. 002011

16 x 16-Bit Multiplier-Accumulator (MAC)

Description

The LSA2011 contains a 16 x 16-bit parallel multiplier-accumulator (MAC). This MAC performs the function:

$$\overline{Z}_{35:0} = \overline{X}_{15:0} * \overline{Y}_{15:0} + \overline{C}_{19:0} + \overline{D}_{35:0} + \overline{SUB}$$

where $\overline{X}$ and $\overline{Y}$ are the multiplier inputs, $\overline{C}$ and $\overline{D}$ are two metal configurable accumulator/adder inputs and $\overline{SUB}$ allows an inverted $\overline{C}$ or $\overline{D}$ input to be interpreted as a two's complement negative number by adding a '1' to the final result.

The $\overline{C}$ and $\overline{D}$ inputs may optionally be tied to the output of the product register to perform a multiply-accumulate function. Otherwise, the user may provide $\overline{C}$ and $\overline{D}$ input data from any point within the array. If both $\overline{C}$ and $\overline{D}$ are '0', the megacell performs a multiply only function. $\overline{C}$ and $\overline{D}$ may also be used as rounding inputs by setting the appropriate bit(s) to round the output at the desired places.

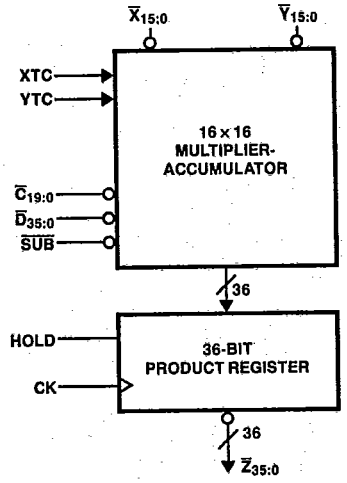
Two independent input format controls (XTC and YTC) determine whether the $\overline{X}$ and $\overline{Y}$ inputs are interpreted as two's complement or unsigned numbers.

A HOLD input is provided on the 36-bit product register which acts as a register enable. When HOLD is HIGH, the product clock (CK) is disabled.

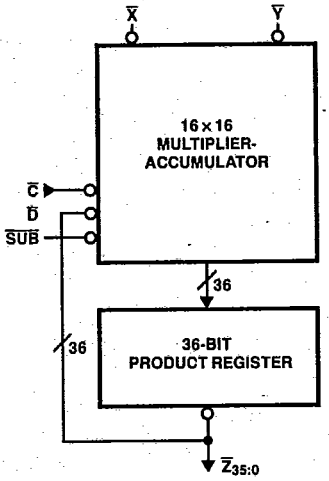
A test input places the MAC into a scan test/signature analysis mode. The product register becomes a 36-bit serial shift register with a scan input (SI), scan output (SO), hold (THOLD) and clock (TCK). Test data is serially shifted into the product register. This data is fed back into the MAC through a signature analysis loop. After an appropriate number of cycles, the test data is serially shifted out and compared versus the expected result.

16 x 16-Bit MAC Functional Block Diagram

Normal Operation (TEST = LOW)

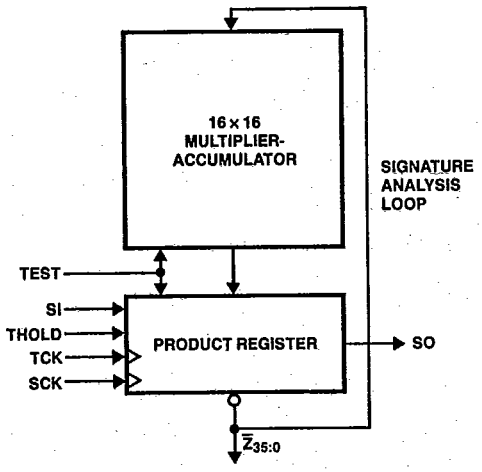


Example of setup for product accumulation

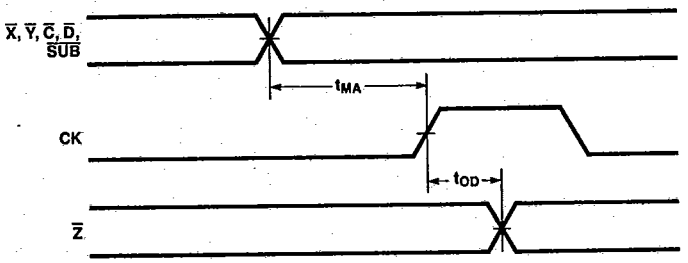


16 x 16-Bit MAC Functional Block Diagram

Test Operation (TEST = HIGH)



AC Timing Waveform



2901 Architecture

Description

The 2901 is a 4-bit slice consisting of a register file (16 × 4 or 32 × 4 dual port RAM), the ALU, the Q register and the necessary control logic. It is expandable in 4-bit increments.

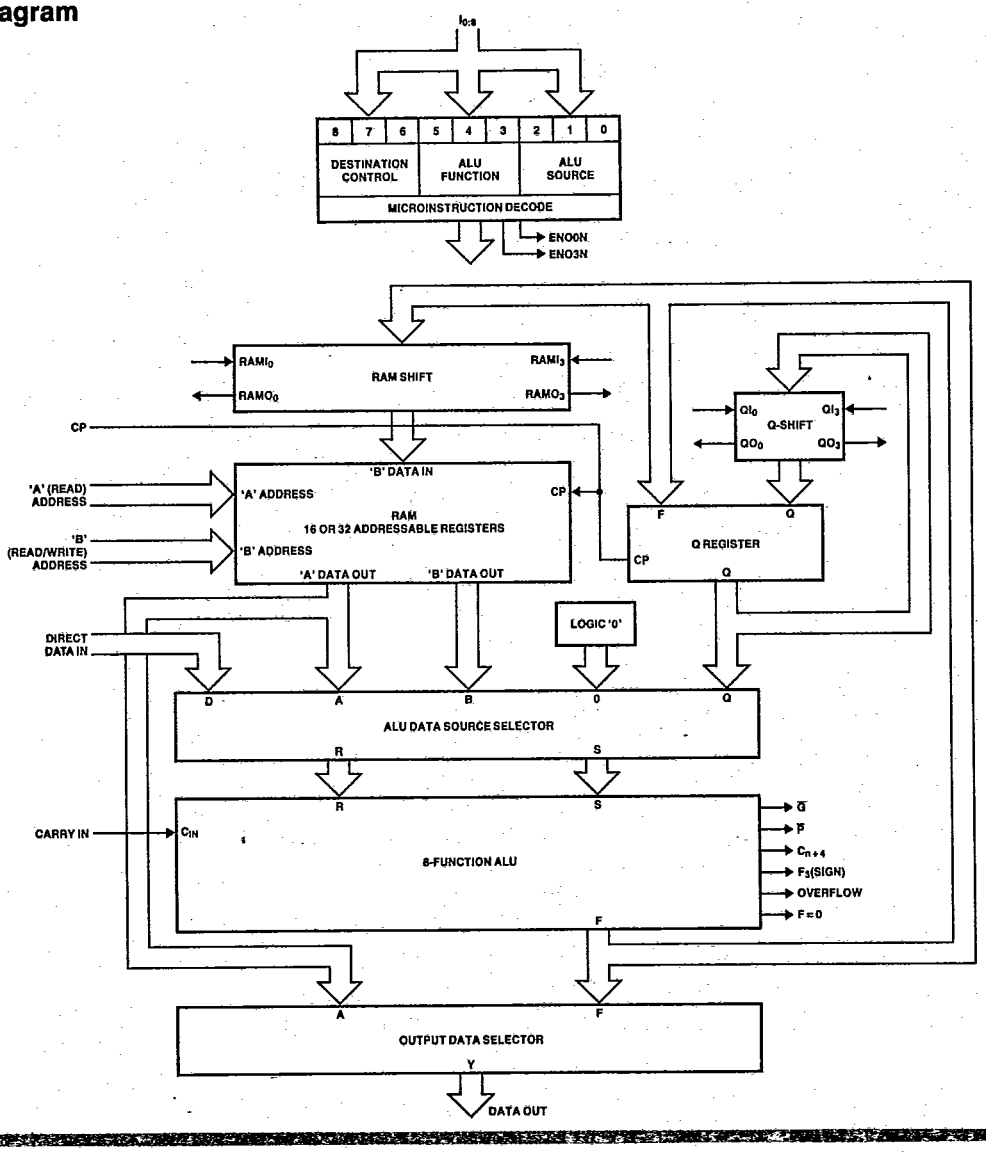
The RAM is addressed by two four or five bit address fields that cause the data to appear at the A or B (internal) ports. Four address bits (A_0–A_3, B_0–B_3) are used for a 16 deep RAM. Five address bits (A_0–A_4, B_0–B_4) are used for a 32 deep RAM. In either case, if the A and B addresses are the same, the data at the A and B ports will be identical.

The ALU can perform three arithmetic and five logical operations on two 4-bit input words, R and S. The R inputs are driven from a four bit 2 to 1 multiplexer whose inputs are from either the RAM A-port or the external data (D) inputs. The S inputs are driven from a 4-bit 3 to 1 multiplexer whose inputs are from the A-port, the B-port, or the Q register. Both multiplexers are controlled by the $I_{0,1,2}$ inputs. This configuration of multiplexers on the ALU R and S inputs enables the user to select eight pairs of combinations of A,B,D,Q and "0" inputs as 4-bit operands to the ALU. The ALU has a carry-in (CN) input, and carry-propagate (PN), carry-generate (GN) , carry-out (CN4) and overflow (OVR) outputs to enable the user to speed up arithmetic operations by implementing carry look-ahead logic and determine if an arithmetic overflow has occurred. An output, FEQ0, is provided that is HIGH when $F_0 = F_1 = F_2 = F_3 = 0$ so that the user can determine when the ALU output is zero.

Testing

LSI Logic provides a single test pin (T) which places the 2901s into a test mode. This pin is required to be accessible on the package level. LSI Logic can then gain direct access into the 2901 through a series of shared inputs and outputs. A set of predefined test patterns are then run on the 2901s to ensure full functionality independent of any other vectors run on the LSA2011.

2901 4-Bit Block Diagram



16-bit 2901 AC Characteristics — nominal conditions — 16 word register

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	58ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	44MHz
Minimum Clock LOW Time	20ns
Minimum Clock HIGH Time	20ns
Minimum Clock Period	58ns

Notes:
1. 16-bit 2901 and 16 deep RAM
2. Nominal case
3. Based on 2 gate array loads on each output

B. Maximum Combinational Propagation Delay.

From Input \ To Output	Y	F15	CN16	CN8	GN	PN	FEQ0N	FEQ0B	FEQ0A	OVR15	OVR7	RAMO15	RAMO7	RAMO0	QO15:0	ENO0N	ENO15N
A, B Address	56.0	52.5	38.7	38.6	31.9	28.8	57.6	51.3	39.2	51.6	48.6	52.5	49.5	36.3	—	—	—
D	43.9	40.4	25.8	26.5	19.3	17.4	44.9	39.7	26.6	39.5	37.0	40.4	37.9	25.3	—		
CN	30.8	27.3	8.1	13.4	—	—	32.4	26.0	19.7	26.4	22.8	27.3	24.2	17.7	—	—	—
I012	51.2	47.7	33.2	33.8	27.0	23.9	52.8	46.5	34.3	46.8	43.8	47.7	44.7	31.5	—	—	—
I345	50.2	46.7	32.2	32.8	26.0	22.9	51.8	45.4	32.4	45.8	42.7	46.7	43.6	27.4	—	—	—
I678	17.9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	12.4	11
A Bypass ALU (I = 2XX)	20.4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CP ⎍	48.2	44.7	30.9	30.8	24.1	21.0	49.8	44.2	31.4	43.8	41.5	44.7	42.4	28.5	11.3	—	—

C. Set-up and Hold Times Relative to Clock (CP).

From Input	CP: Set-up Time Before H→L	Hold Time After H→L	Set-up Time Before L→H	Hold Time After L→H
A, B Address	13	0	57.4	0
B Destination Address	7	Do Not Change		0
D	—	—	44.6	0
CN	—	—	31.5	0
I012	—	—	51.9	0
I345	—	—	50.9	0
I678	8.6	Do Not Change		0
RAMI/QI0:15	—	—	11.1	0

Timing Diagram Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.
5. All timing listed above assumes a fanout of two, estimated wirelength and minimum drive configuration for the programmable output buffers.

Functionality Notes:
1. The 2901 megacell does not contain three-state outputs, therefore there is no $\overline{OE}$ signal.
2. Each of the bidirectional pins (RAM0, RAM15, Q0, Q15) is replaced by three pins, one input, one output and an output enable. There are only two output enable signals. ENO0N controls both RAMO0N and QO0N while ENO15N controls both RAMO15N and QO15N.
3. FEQ0N is the F = 0 output for the full 16-bit 2901. FEQ0A is the F = 0 output for the first four bits. FEQ0B is the F = 0 output for the next four bits.

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Printed in U.S.A. 930/586/30K/IM/J