13 I/O PORTS

OVERVIEW

The S5N8946 has 18 programmable I/O ports. You can configure each I/O port to input mode, output mode, or special function mode. To do this, you write the appropriate settings to the IOPMOD and IOPCON registers. User can set filtering for the input ports using IOPCON register.

The modes of the ports from port0 to port7 are determined only by the IOPMOD register. But port[11:8] can be used as xINTREQ[3:0], port[13:12] as nXDREQ[1:0], port[15:14] as nXDACK[1:0], port[16] as TOUT0, or port[17] as TOUT1 depending on the settings in IOPCON register.

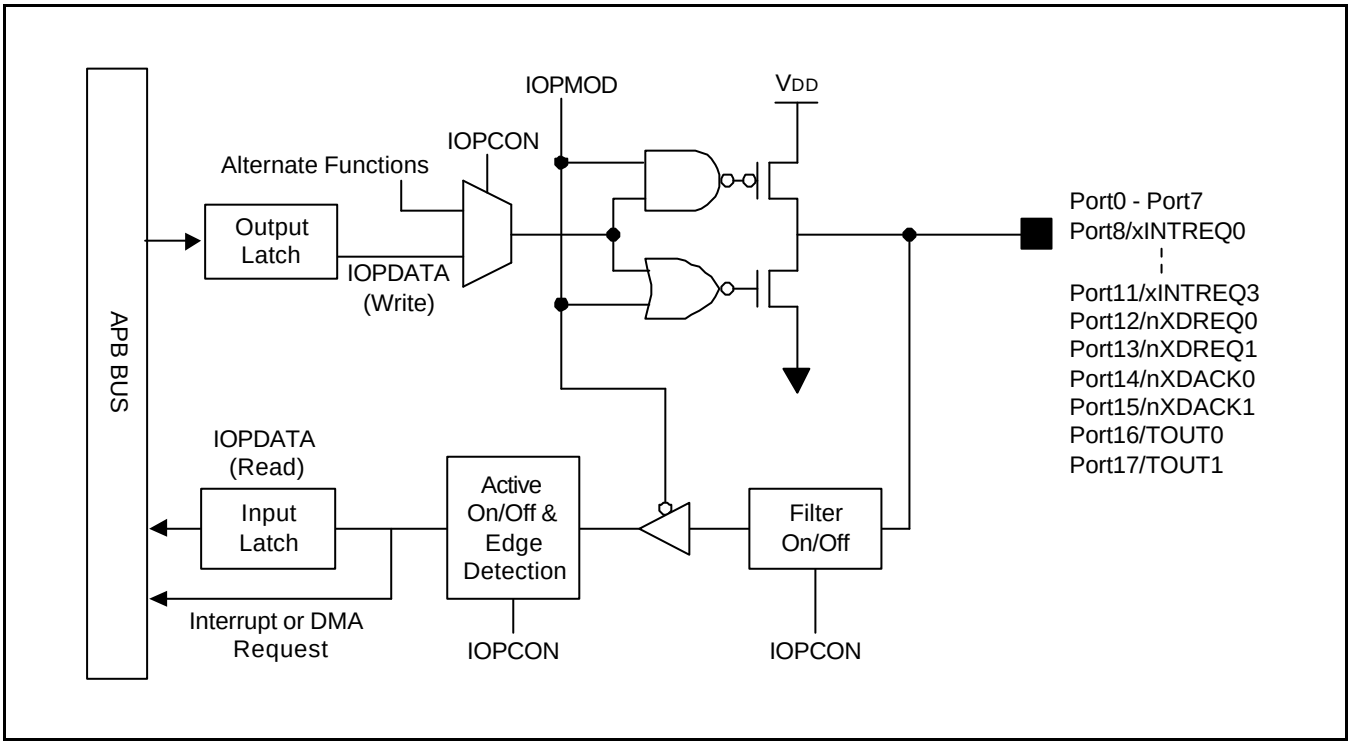


Figure 13-1. I/O Port Function Diagram

I/O PORT SPECIAL REGISTERS

Three registers control the I/O port configuration: IOPMOD, IOPCON, and IOPDATA. These registers are described in detail below.

I/O PORT MODE REGISTER (IOPMOD)

The I/O port mode register, IOPMOD, is used to configure the port pins, P17–P0.

NOTE

If the port is used for a special function such as an external interrupt request, an external DMA request, or acknowledge signal and timer outputs, its mode is determined by the IOPCON register, not by IOPMOD.

Table 13-1. IOPMOD Register

Register	Offset Address	R/W	Description	Reset Value
IOPMOD	0x5000	R/W	I/O port mode register	0x00000000

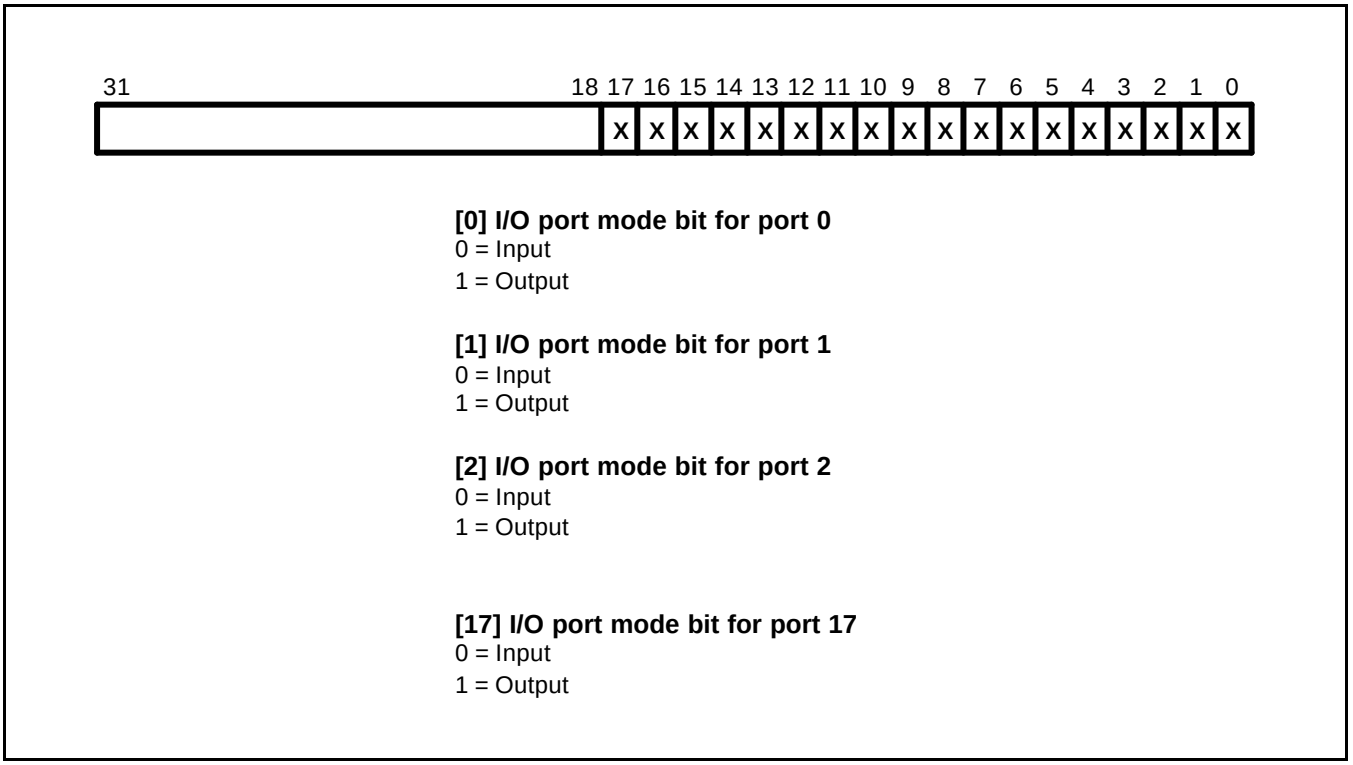


Figure 13-2. I/O Port Mode Register (IOPMOD)

I/O PORT CONTROL REGISTER (IOPCON)

The I/O port control register, IOPCON, is used to configure the port pins, P17–P8.

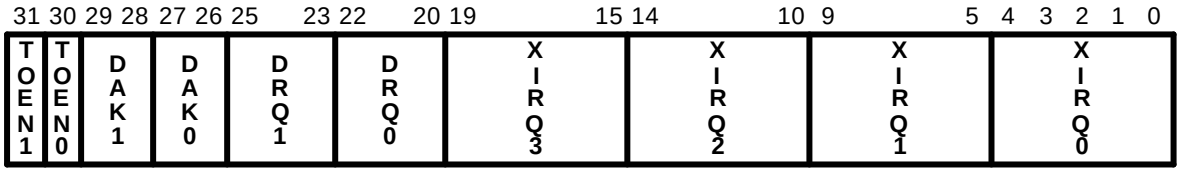
NOTE

If the port is used for a special function such as an external interrupt request, an external DMA request, or acknowledge signal and timer outputs, its mode is determined by the IOPCON register, not by IOPMOD.

For the special input ports, S5N8946 provides 3-tap filtering. If the input signal levels are same for the three system clock periods, that level is taken as input for dedicated signals such as external interrupt requests and external DMA requests.

Table 13-2. IOPCON Register

Register	Offset Address	R/W	Description	Reset Value
IOPCON	0x5004	R/W	I/O port control register	0x00000000



[4:0] Control external interrupt request 0 input for port 8 (xIRQ0)

[4] Port 8 for xINTREQ0
0 = Disable 1 = Enable
[3] 0 = Active Low 1 = Active High
[2] 0 = Filtering off 1 = Filtering on
[1:0] 00 = Level detection 01 = Rising edge detection
10 = Falling edge detection 11 = Both edge detection

[9:5] Control external interrupt request 1 input for port 9 (xIRQ1)

(See control external interrupt request 1.)

[14:10] Control external interrupt request 2 input for port 10 (xIRQ2)

(See control external interrupt request 2.)

[19:15] Control external interrupt request 3 input for port 11 (xIRQ3)

(See control external interrupt request 3.)

[22:20] Control external DMA request 0 input for port 12 (DRQ0)

[22] Port 12 for nXDREQ0
0 = Disable 1 = Enable
[21] 0 = Filtering off 1 = Filtering on
[20] 0 = Active Low 1 = Active High

[25:23] Control external DMA request 1 input for port 13 (DRQ1)

[25] Port 13 for nXDREQ1
0 = Disable 1 = Enable
[24] 0 = Filtering off 1 = Filtering on
[23] 0 = Active Low 1 = Active High

[27:26] Control external DMA acknowledge 0 output for port 14 (DAK0)

[27] Port 14 for nXDACK0
0 = Disable 1 = Enable
[26] 0 = Active Low 1 = Active High

[29:28] Control external DMA acknowledge 1 output for port 15 (DAK1)

[29] Port 15 for nXDACK1
0 = Disable 1 = Enable
[28] 0 = Active Low 1 = Active High

[30] Control Timeout 0 for port 16 (TOEN0)

0 = Disable 1 = Enable

[31] Control Timeout 1 for port 17 (TOEN1)

0 = Disable 1 = Enable

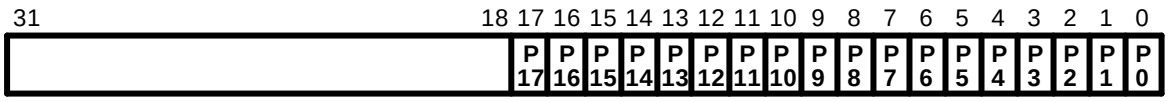
Figure 13-3. I/O Port Control Register (IOPCON)

I/O PORT DATA REGISTER (IOPDATA)

The I/O port data register, IOPDATA, contains one-bit read values for I/O ports that are configured to input mode and one-bit write values for ports that are configured to output mode. Bits[17:0] of the 18-bit I/O port register value correspond directly to the 18 port pins, P17–P0.

Table 13-3. IOPDATA Register

Register	Offset Address	R/W	Description	Reset Value
IOPDATA	0x5008	R/W	I/O port data register	Undefined



[17:0] I/O port read/write values for ports 17 - 0 (P0 - P17)

NOTE: The values in the I/O port data register reflect the signal level on the respective I/O port pins. When the ports are configured to output mode, the bit reflects the ports write value. When the port is configured to input mode, the bit reflects the ports read value.

Figure 13-4. I/O Port Data Register (IOPDATA)

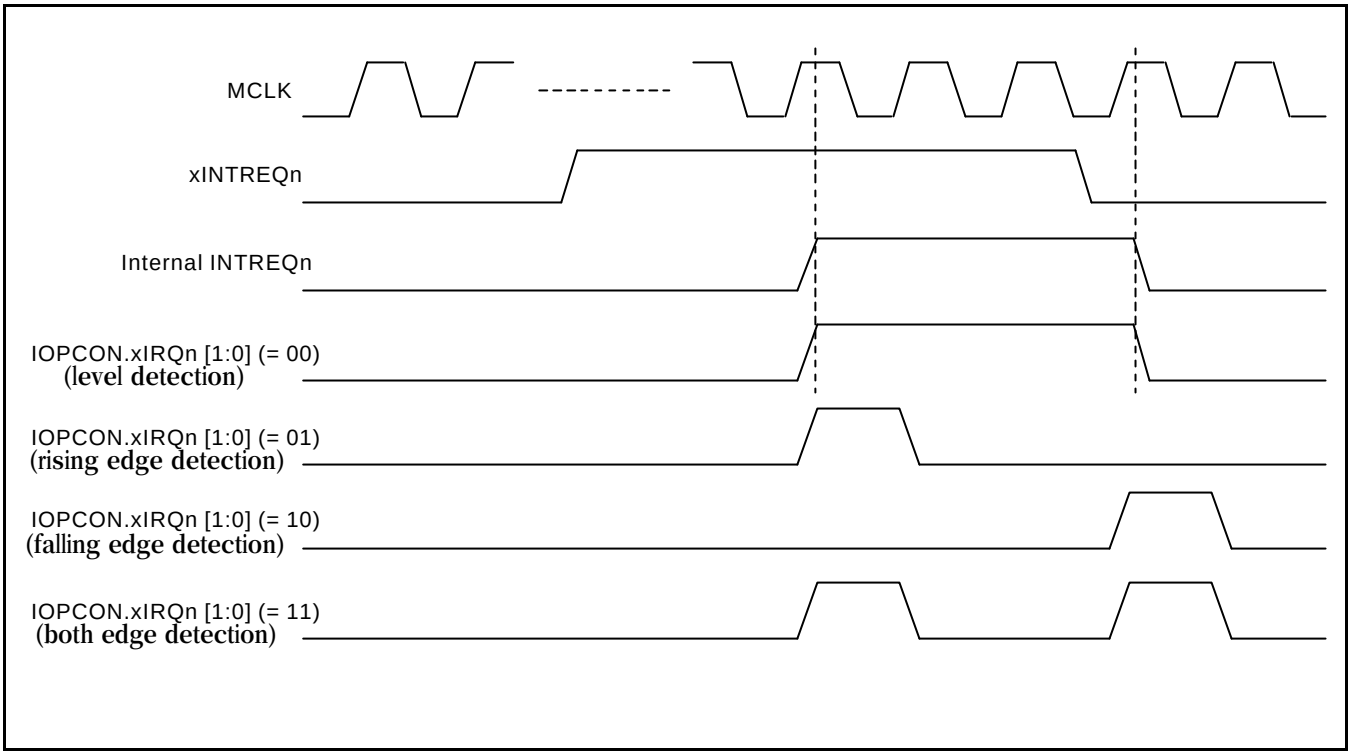


Figure 13-5. External Interrupt Request Timing (Active High)

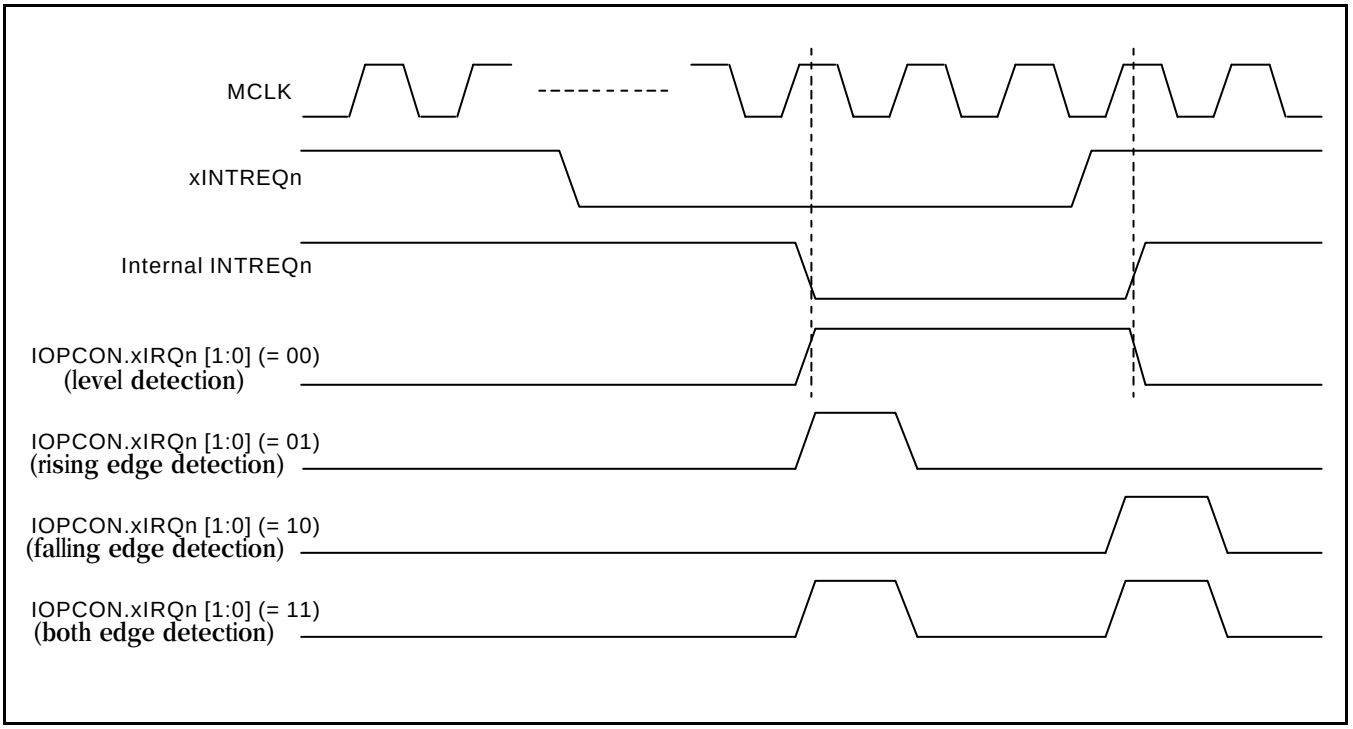


Figure 13-5. External Interrupt Request Timing (Active Low)