MOTOROLA

Quad Bus Driver

ELECTRICALLY TESTED PER:
MPG 10592

The 10592 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable ($\overline{E}$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector.

Outputs can drive higher values of load resistance, provided that the combination of I_R drop and load return voltage V_{LR} does not cause an output collector to go more negative than -2.4 V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC}.

When the $\overline{E}$ input is high, both output transistors of a driver are nonconducting. When not used, the $\overline{E}$ inputs, as well as the D inputs, may be left open.

- Open Collector Outputs Drive Terminated Lines or Transformers
- 50 kΩ Input Pull-down Resistors on All Inputs (Unused Inputs May be left Open)
- 805 mW typ/pkg (No Load)
- Propagation Delay = 3.5 ns typ ($\overline{E}$-Output)
  = 3.0 ns typ (D-Output)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
Z_2	1	5	2	GND
$\overline{Z_2}$	2	6	3	GND
Z_1	3	7	4	GND
$\overline{Z_1}$	4	8	5	GND
D_1	5	9	7	OPEN
D_2	6	10	8	OPEN
$\overline{E_1}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{E_2}$	9	13	12	OPEN
D_3	10	14	13	OPEN
D_4	11	15	14	OPEN
$\overline{Z_4}$	12	16	15	GND
Z_4	13	1	17	GND
$\overline{Z_3}$	14	2	18	GND
Z_3	15	3	19	GND
V_{CC}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

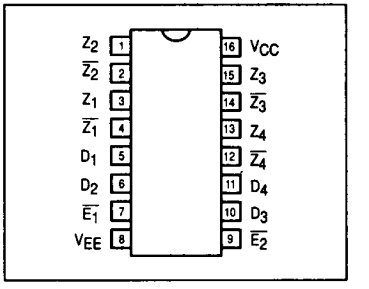
Military 10592

AVAILABLE AS

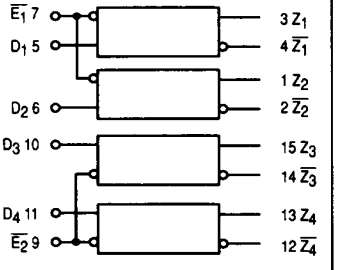
1) JAN: N/A
2) SMD: N/A
3) 883: 10592/BXAJC
X = CASE OUTLINE AS FOLLOWS:

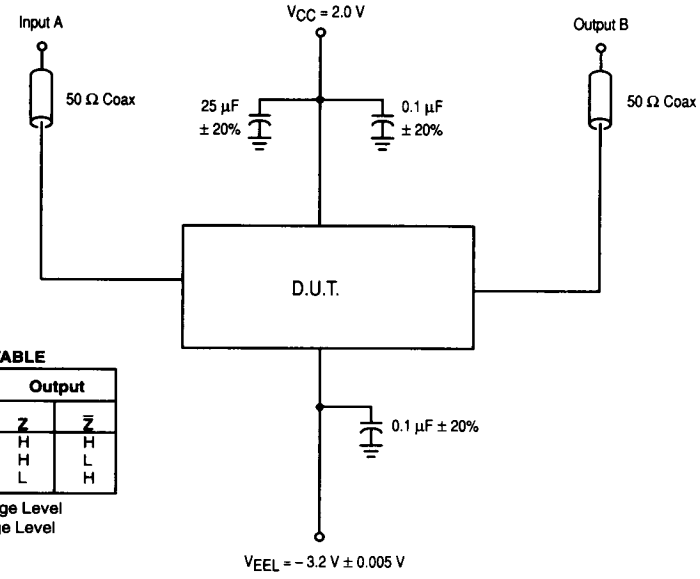
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM

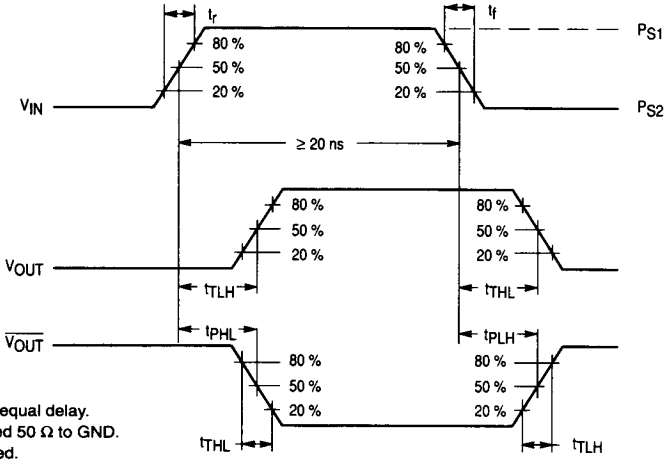




TRUTH TABLE

Inputs		Output	
$\overline{E}$	D	Z	$\overline{Z}$
H	X	H	H
L	H	H	L
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



NOTES
1. L1 = L2: Matched for equal delay.
2. All other outputs loaded 50 Ω to GND.
3. 2:1 divider may be used.
4. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 1. Switching Test Circuit and Waveforms

10592
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE} (MIN)	V_{EE} (MAX)	V_{EE} (Nom)	B_{VO}	V_{LK}	V_{OLS}
T_A = 25 °C	- 0.780	- 1.85	- 1.105	- 1.475	- 0.89	- 1.69	- 5.72	- 4.68	- 5.2	+ 5.095	- 1.850	- 2.4
T_A = 125 °C	- 0.630	- 1.82	- 1.000	- 1.400	- 0.78	- 1.655	- 5.72	- 4.68	- 5.2	+ 4.960	- 1.825	- 2.4
T_A = - 55 °C	- 0.880	- 1.92	- 1.255	- 1.510	- 0.97	- 1.715	- 5.72	- 4.68	- 5.2	+ 4.960	- 1.89	- 2.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = GND, Output Load = 50 Ω to GND, V_{LR} = 270 Ω to + 5.5 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{LR}	V_{OLS}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.10	+ 0.10	- 0.10	+ 0.10	- 0.15	+ 0.05	V	5, 6, 10, 11	5, 6, 10, 11					8	16	1 - 4, 12 - 15
V_{OL}	Low Output Voltage	- 0.90	- 0.70	- 0.95	- 0.70	- 0.85	- 0.60	V	5, 6, 10, 11	5, 6, 10, 11					8	16	1 - 4, 12 - 15
V_{OLC}	Low Output Voltage	- 0.90	- 0.70	- 0.95	- 0.70	- 0.85	- 0.60	V			5, 6, 10, 11	5, 6, 10, 11			8	16	1 - 4, 12 - 15
V_{OHC}	High Output Voltage	- 0.10	+ 0.10	- 0.10	- 0.10	- 0.15	+ 0.05	V			5, 6, 10, 11	5, 6, 10, 11			8	16	1 - 4, 12 - 15
I_{IH1}	Input Current High		220		350		350	µA	5 - 7, 9 - 11						8	16	5 - 7, 9 - 11
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 9 - 11					8	16	5 - 7, 9 - 11
I_{OV}	Short Circuit Current (No Output Voltage)		104.4		102.2		102.2	mA	7, 9				1 - 4, 12 - 15		8	16	1 - 4, 12 - 15
I_{OS}	Output Short Circuit Current	34.1		34.7		- 34.7		mA		5, 6, 10, 11				1 - 4, 12 - 15	8	16	1 - 4, 12 - 15
I_{QOFF}	Open Collector Input Current		500		500		500	µA		2, 7, 9, 14, 15					8	16	2, 7, 9, 14, 15
I_{EE}	Power Supply Drain Current	- 140		- 154		- 154		mA							8	16	8

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to Gnd.

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QUIESCENT LIMIT TABLE *

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	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE} (MIN)	V_{EE} (MAX)	V_{EE} (Nom)	B_{VO}	V_{LK}	V_{OLS}
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	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = GND, Output Load = 50 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	0.5	3.3	0.5	4.7	0.5	3.8	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t_{THL}	Fall Time	0.5	3.3	0.5	4.7	0.5	3.8	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t_{PLH} t_{PHL}	Propagation Delay Data	1.5	4.5	1.5	5.6	1.5	5.3	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t_{PLH} t_{PHL}	Propagation Delay Enable	2.0	6.0	1.0	9.0	1.0	6.0	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15

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