REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15																		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-03-15

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, PROGRAMMABLE, OFF-LINE, PULSE WIDTH MODULATOR CONTROLLER, MONOLITHIC SILICON

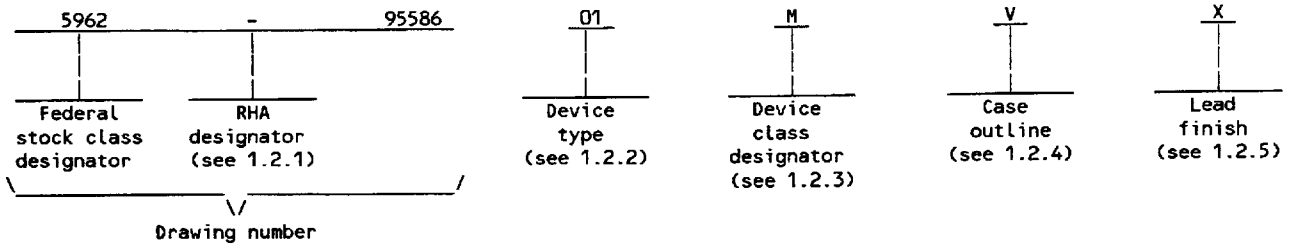
SIZE	CAGE CODE	5962-95586
A	67268	

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UC1851	Programmable, off-line, pulse width modulator controller

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage ($+V_{IN}$)	
Voltage driven	+32 V
Current driven, 100 mA maximum	Self-limiting
PWM output voltage	40 V
PWM output current, steady state	400 mA
PWM output peak energy discharge	20 µJ
Driver bias current	-200 mA
Reference output current	-50 mA
Slow start sink current	20 mA
V_{IN} sense current	10 mA
Current limit inputs	-0.5 V to +5.5 V
Stop input	-0.3 V to +5.5 V
Comparator inputs	Internally clamped at 12 V
Power dissipation (P_D) at T_A < +25°C	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA})	110°C/W

1.4 Recommended operating conditions.

Supply voltage ($+V_{IN}$)	20.0 V
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Power inputs section							
Start-up current	I_{SU}	V_{IN} = 30 V, START/UV pin = 2.5 V	1,2,3	01		6	mA
Operating current	I_S	V_{IN} = 30 V, START/UV pin = 3.5 V	1,2,3	01		21	mA
Supply over-voltage (OV) clamp voltage	V_S	V_{IN} = 20 mA	1,2,3	01	33	45	V
Reference section							
Reference voltage	V_{REF}	T_A = +25°C	1	01	4.95	5.05	V
Line regulation	V_{LN}	V_{IN} = 8 V to 30 V	1,2,3	01		15	mV
Load regulation	V_{LD}	I_L = 0 mA to 10 mA	1,2,3	01		20	mV
Total reference variation	V_{TR}		1,2,3	01	4.90	5.10	V
Short circuit current	I_{OS}	T_A = +25°C, V_{REF} = 0 V	1	01		-100	mA
Oscillator section							
Nominal frequency	f_N	T_A = +25°C	4	01	47	53	kHz
Voltage stability	V_{ST}	V_{IN} = 8 V to 30 V	4,5,6	01		1	%
Total reference variation	TRV		4,5,6	01	45	55	kHz
Maximum frequency	f_{MAX}	R_T = 2kΩ, C_T = 330 pF	4,5,6	01	500		kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Ramp generator section							
Minimum ramp current	I_{RMN}	I_{SENSE} = -10 µA	1,2,3	01		-14	µA
Maximum ramp current	I_{RMX}	I_{SENSE} = 1.0 mA	1,2,3	01	-0.9		mA
Ramp valley voltage	V_{RV}		1,2,3	01	0.3	0.6	V
Ramp peak voltage	V_{RP}	Clamping level	1,2,3	01	3.9	4.5	V
Error amplifier section							
Input offset voltage	V_{IO}	V_{CM} = 5.0 V	1,2,3	01		5	mV
Input bias current	I_{IB}		1,2,3	01		2	µA
Input offset current	I_{IO}		1,2,3	01		0.5	µA
Open loop gain	OLG	ΔV_{OUT} = 1 V to 3 V	4,5,6	01	60		dB
Output swing (max output ≤ ramp peak - 100 mV)	V_{OSW}	T_A = +25°C, minimum total range	1	01	0.3	3.5	V
Common mode rejection ratio	CMRR	V_{CM} = 1.5 V to 5.5 V	4,5,6	01	70		dB
Power supply rejection ratio	PSRR	V_{IN} = 8 V to 30 V	4,5,6	01	70		dB
Short circuit current	I_{SC}	V_{COMP} = 0 V	1,2,3	01		-10	mA
Gain bandwidth	GBW	T_A = +25°, A_{VOL} = 0 dB 3/	4	01	1		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Pulse width modulator section							
Continuous duty cycle range (other than zero)	CDCR	Minimum total continous range ramp peak < 4.2 V	4,5,6	01	2	46	%
Output high level voltage	V_{DIN}	I_{SOURCE} = 20 mA	1,2,3	01	18		V
		I_{SOURCE} = 200 mA			17		
Rise time	t_R	C_L = 1 nF, T_A = +25°C 3/	9	01		150	ns
Fall time	t_F	C_L = 1 nF, T_A = +25°C 3/	9	01		150	ns
Output saturation voltage	V_{SAT}	I_{OUT} = 20 mA	1,2,3	01		0.4	V
		I_{OUT} = 200 mA				2.2	
Comparator delay		SLOW START pin to PWM OUT pin, R_L = 1 kΩ, T_A = +25°C 3/	9	01		500	ns
Sequencing functions section							
Comparator thresholds voltage	V_{CT}	START/UV pin, OV SENSE pin, RESET pin	1,2,3	01	2.8	3.2	V
Input bias current	I_{IB}	OV SENSE pin and RESET pin at 0 V	1,2,3	01		-4.0	µA
Input leakage current	I_{IL}	OV SENSE pin and RESET pin at 10 V	1,2,3	01		2.0	µA
Start/UV hysteresis current	I_{SUVH}	START/UV pin at 2.5 V	1,2,3	01	170	220	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Sequencing functions section - continued.							
External stop threshold voltage	V_{EST}	STOP pin	1,2,3	01	0.6	2.4	V
Error latch activate current	I_{ELA}	STOP pin at 0 V, OV SENSE pin at > 3 V	1,2,3	01		-200	µA
Driver bias saturation voltage (V_{IN} - V_{OH})	V_{DBS}	I_B = -50 mA	1,2,3	01		3	V
Driver bias leakage current	I_{DBL}	V_B = 0 V	1,2,3	01		-10	µA
Slow start saturation voltage	V_{SSS}	I_S = 10 mA	1,2,3	01		0.5	V
Slow start leakage current	I_{SSL}	V_S = 4.5 V	1,2,3	01		2.0	µA
Current control section							
Current limit offset voltage	V_{CLO}		1,2,3	01		5	mV
Current shutdown offset voltage	V_{CSO}		1,2,3	01		430	mV
Input bias current	I_{IB}	CURRENT SENSE pin at 0 V	1,2,3	01		-5	µA
Common mode range voltage	V_{CMR}	3/	1,2,3	01	-0.4	3.0	V
Current limit delay time	t_{CLD}	CURRENT SENSE pin to PWM OUT pin, R_L = 1 kΩ, T_A = +25°C	9	01		400	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Unless otherwise specified, V_{IN} = 20 V, timing resistance (R_T) = 20 kΩ, timing capacitance (C_T) = .001 mF, ramp resistance (R_R) = 10 kΩ, and ramp capacitance (C_R) = .001 mF. Current limit threshold voltage = 200 mV.

2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

3/ If not tested, shall be guaranteed to the limits specified in table I herein.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

Device type	01	
Case outlines	V	2
Terminal number	Terminal symbol	
1	COMPENSATION (COMP)	COMPENSATION (COMP)
2	START/UNDER VOLTAGE (UV)	START/UNDER VOLTAGE (UV)
3	OVER VOLTAGE (OV)/SENSE	OVER VOLTAGE (OV)/SENSE
4	STOP	STOP
5	RESET	RESET
6	CURRENT THRESHOLD	NC
7	CURRENT SENSE	CURRENT THRESHOLD
8	SLOW START	CURRENT SENSE
9	TIMING RESISTANCE (R_T)/ TIMING CAPACITANCE (C_T)	SLOW START
10	RAMP	TIMING RESISTANCE (R_T)/ TIMING CAPACITANCE (C_T)
11	INPUT VOLTAGE SENSE (V_{IN} SENSE)	RAMP
12	PULSE WIDTH MODULATOR OUTPUT (PWM OUT)	INPUT VOLTAGE SENSE (V_{IN} SENSE)
13	GROUND	PULSE WIDTH MODULATOR OUTPUT (PWM OUT)
14	DRIVE BIAS	GROUND
15	+INPUT VOLTAGE (+V_{IN})	DRIVE BIAS
16	5.0 V REFERENCE	NC
17	INVERSE INPUT	+INPUT VOLTAGE (+V_{IN})
18	NON-INVERSE INPUT	5.0 V REFERENCE
19	---	INVERSE INPUT
20	---	NON-INVERSE INPUT

NC = No connection

FIGURE 1. Terminal connections.

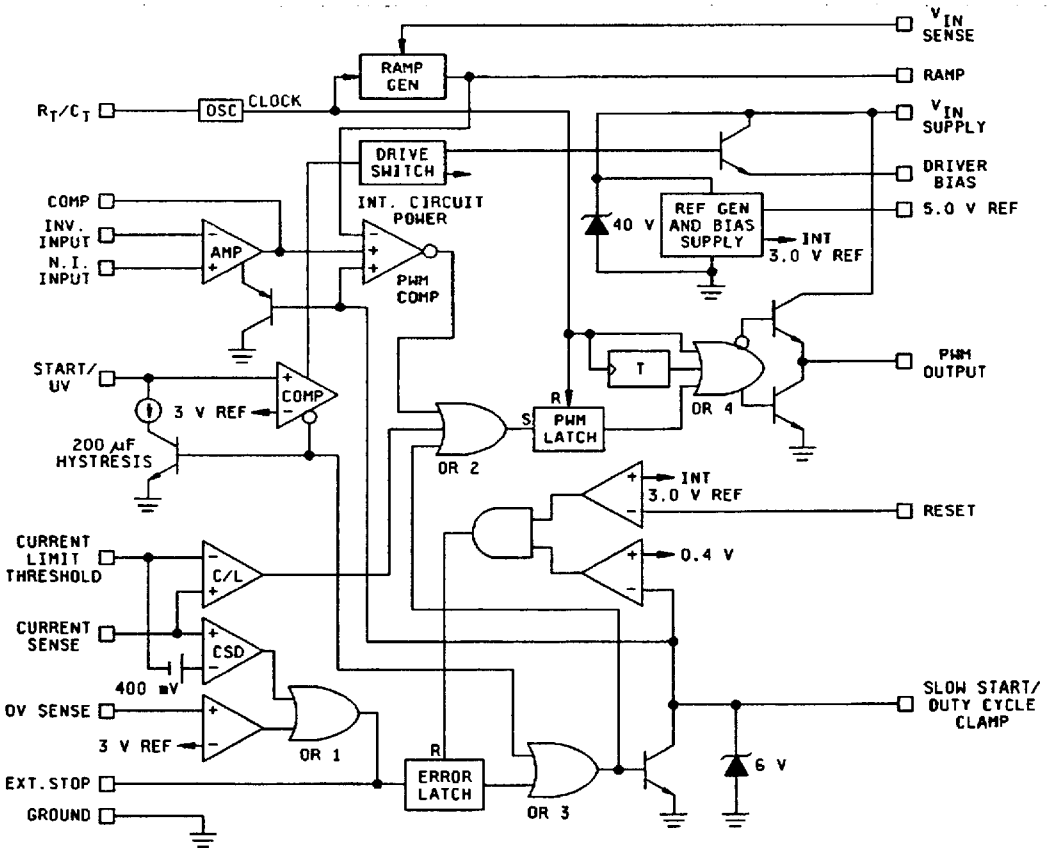


FIGURE 2. Logic diagram.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,4, 5,6,9 1/	1,2,3,4, 5,6,9 1/	1,2,3,4, 5,6,9 1/
Group A test requirements (see 4.4)	1,2,3,4,5,6,9	1,2,3,4,5,6,9	1,2,3,4, 5,6,9
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions.

OSCILLATOR	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $K_C/(R_T \times C_T)$ where K_C is a first-order correction factor = 0.3 log $(C_T \times 10^{12})$.
RAMP GENERATOR	Develops linear ramp with slope defined externally by dV/dT = sense voltage/$(R_R \times C_R)$. C_R is normally selected ≤ C_T and its value will have some effect upon valley duty cycle. Limiting the minimum value for I_{SENSE} into V_{IN} SENSE pin will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
ERROR AMPLIFIER	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity gain stable. The output is held low by the SLOW START voltage at turn on in order to minimize overshoot.
REFERENCE GENERATOR	Precision 5.0 V for internal and external usage to 50 mA. Tracking 3.0 V reference for internal usage only with nominal accuracy of ±2%. 40 V clamp zener for chip overvoltage (OV) protection, 100 mA maximum current.
PWM COMPARATOR	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
PWM LATCH	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse comparator, or the error latch. Resets with each internal clock pulse.
PWM OUTPUT SWITCH	Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "ON" state is high.
START/ UV SENSE	With an increasing voltage, this comparator generates a turn-on signal and releases the SLOW START clamp at a signal threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200 μA hysteresis current.
DRIVE SWITCH	Disables most of the chip to hold internal current consumption low, and DRIVER BIAS pin off, until input voltage reaches start threshold.
DRIVE BIAS	Supplies drive to external circuitry upon start-up.
SLOW START	Clamps low to hold PWM off. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
ERROR LATCH	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to ERROR LATCH are: a. OV SENSE > 3.2 V (typically 3.0 V) b. STOP > 2.4 V (typically 1.6 V). c. CURRENT SENSE at 400 mV over threshold (typically). ERROR LATCH resets when SLOW START voltage falls to 0.4 V if RESET pin < 2.8 V. With RESET pin > 3.2 V, ERROR LATCH will remain set.
CURRENT LIMITING	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400 mV (typically) above threshold, a shutdown signal is sent to ERROR LATCH.
EXTERNAL STOP	A voltage over 2.4 will set the ERROR LATCH and hold the output off. A voltage less than 0.8 V will defeat the ERROR LATCH and prevent shutdown. A capacitor here will slow the action of the ERROR LATCH for transient protection by providing a typical delay of 13 ms/μF.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.