PowerMOS transistor TOPFET

BUK108-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	100	mΩ

FUNCTIONAL BLOCK DIAGRAM

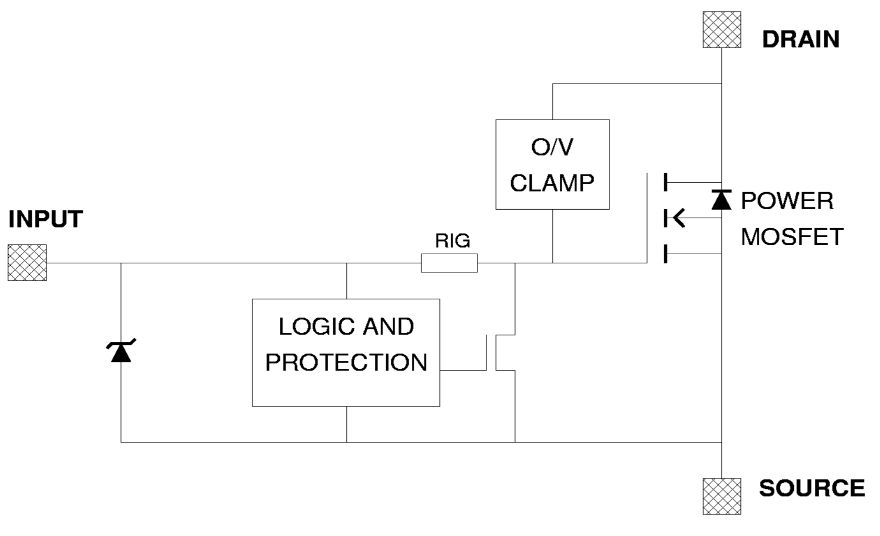
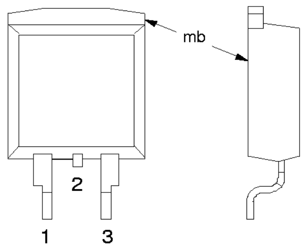


Fig.1. Elements of the TOPFET.

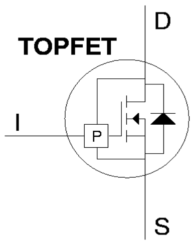
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	$V_{IS} = 0$ V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ ˚C; $V_{IS} = 10$ V	-	15	A
I_D	Continuous drain current	$T_{mb} \leq 100$ ˚C; $V_{IS} = 10$ V	-	9.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ ˚C; $V_{IS} = 10$ V	-	60	A
P_D	Total power dissipation	$T_{mb} \leq 25$ ˚C	-	40	W
T_{stg}	Storage temperature	-	-55	150	˚C
T_j	Continuous junction temperature[2]	normal operation	-	150	˚C
T_{sold}	Lead temperature	during soldering	-	250	˚C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 10$ V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	$V_{IS} = 10$ V	-	20	V
		$V_{IS} = 5$ V	-	35	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ ˚C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ ˚C; $I_{DM} = 15$ A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ ˚C; $I_{DM} = 4$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

---

[1] Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

[2] A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

[3] The input voltage for which the overload protection circuits are functional.

[4] The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 33)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \leq$ 300 µs; $\delta \leq$ 0.01	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 ˚C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 7.5 A; $t_p \leq$ 300 µs; $\delta \leq$ 0.01; V_{IS} = 10 V	-	65	100	mΩ
		V_{IS} = 5 V	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 ˚C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \geq$ 0.5 A[2]	150	-	-	˚C

---

[1] The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

[2] The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[1]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 ˚C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	1.0	2.5	5.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

TRANSFER CHARACTERISTICS

T_{mb} = 25 ˚C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
$I_{D(SC)}$	Drain current[2]	V_{DS} = 13 V; V_{IS} = 10 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 ˚C. R_I = 50 Ω . Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	4	-	µs
$t_{d\ off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	5	-	µs
$t_{d\ on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	0.5	-	µs
$t_{d\ off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ ˚C; V_{IS} = 0 V	-	15	A

---

[1] The input voltage below which the overload protection circuits will be reset.

[2] During overload before short circuit load protection operates.

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 ˚C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[1]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead solering point to source bond pad	-	7.5	-	nH

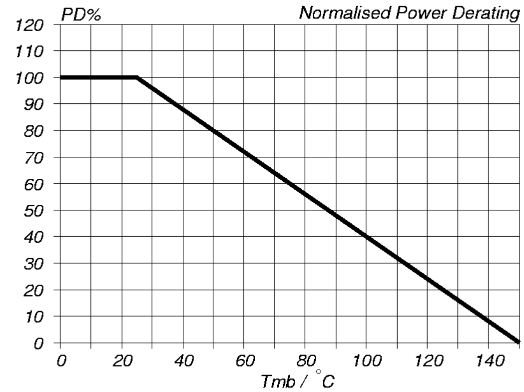


Fig.2. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ˚C) = f(T_{mb})$

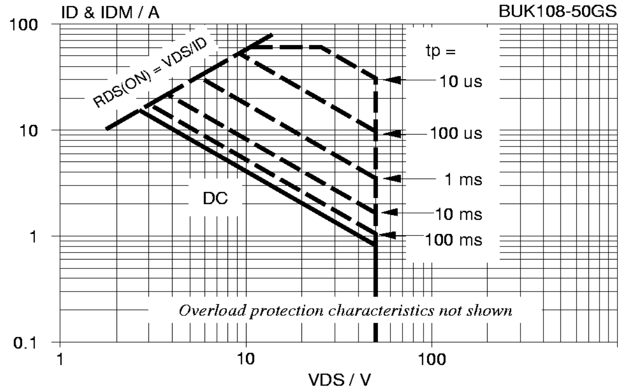


Fig.4. Safe operating area. T_{mb} = 25 ˚C I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

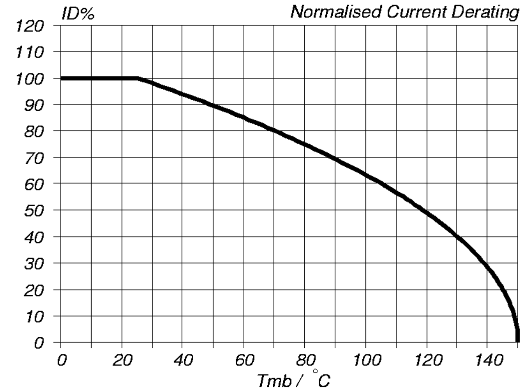


Fig.3. Normalised continuous drain current. $I_D\% = 100 \cdot I_D/I_D(25\ ˚C) = f(T_{mb})$; conditions: V_{IS} = 5 V

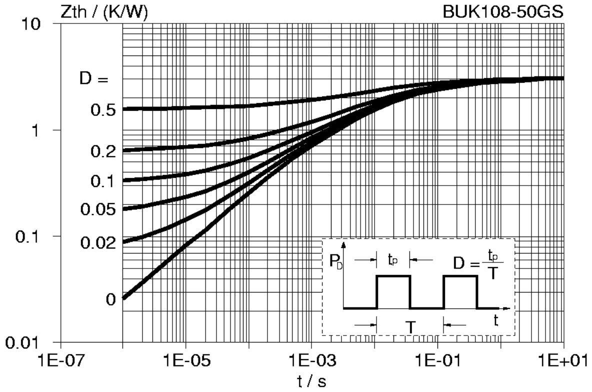


Fig.5. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

---

[1] The reverse diode of this type is not intended for applications requiring fast reverse recovery.

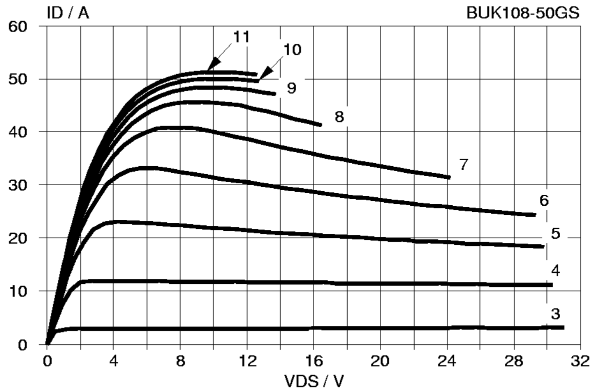


Fig.6. Typical output characteristics, $T_j = 25$ ˚C.
ID = f(V_{DS}); parameter V_{IS}; $t_p = 250$ µs & $t_p < t_{d\,sc}$

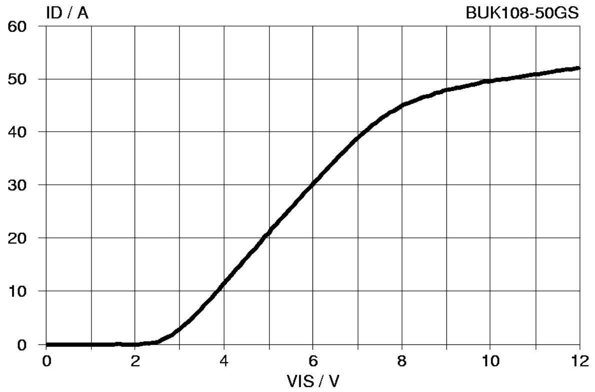


Fig.9. Typical transfer characteristics, $T_j = 25$ ˚C.
$I_D = f(V_{IS})$; conditions: $V_{DS} = 10$ V; $t_p = 250$ µs

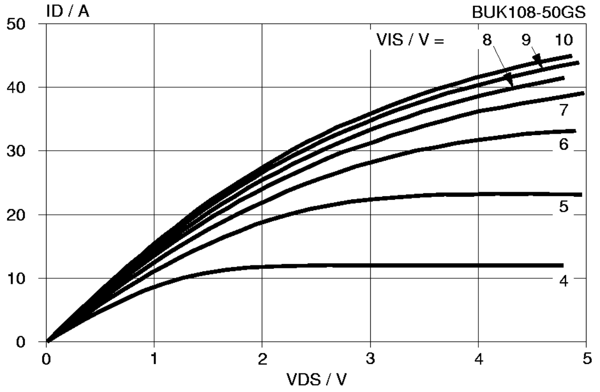


Fig.7. Typical on-state characteristics, $T_j = 25$ ˚C.
ID = f(V_{DS}); parameter V_{IS}; $t_p = 250$ µs

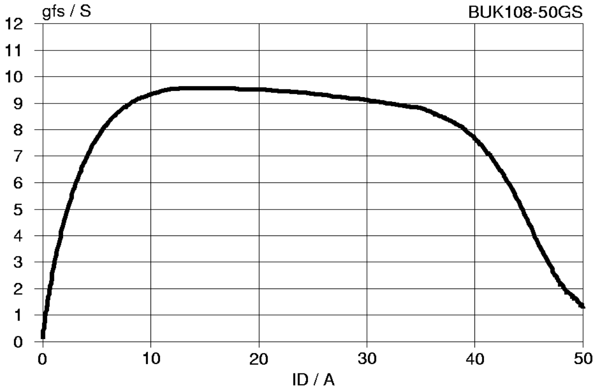


Fig.10. Typical transconductance, $T_j = 25$ ˚C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 10$ V; $t_p = 250$ µs

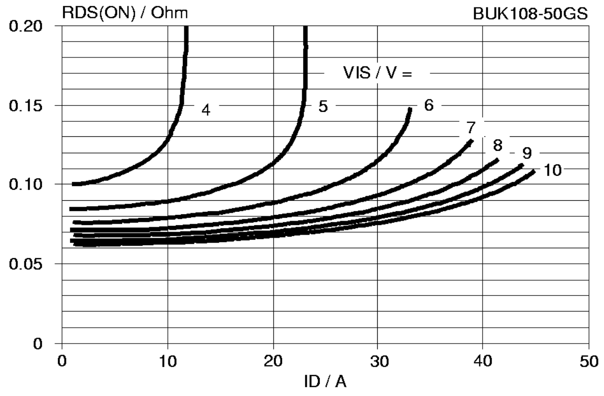


Fig.8. Typical on-state resistance, $T_j = 25$ ˚C.
$R_{DS(ON)} = f(I_D)$; parameter V_{IS}; $t_p = 250$ µs

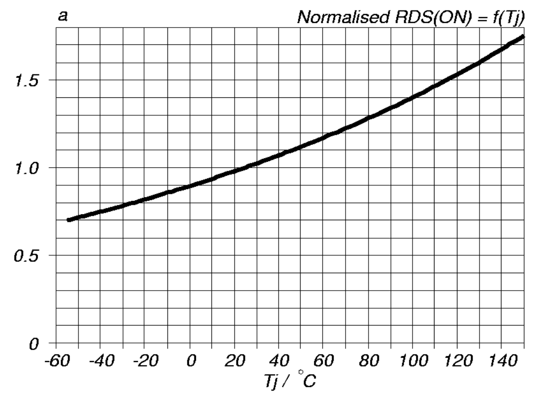


Fig.11. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C $= f(T_j)$; $I_D = 7.5$ A; $V_{IS} = 5$ V

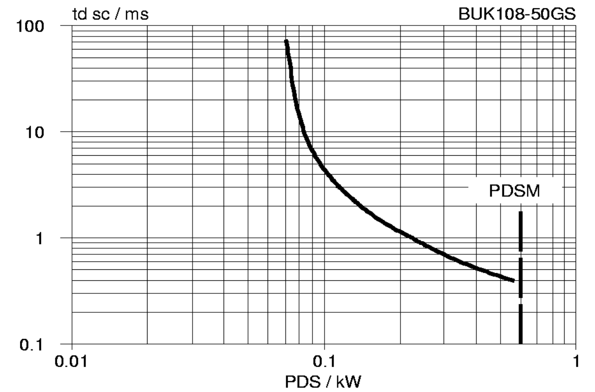


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 5$ V; $T_j = 25$ ˚C.

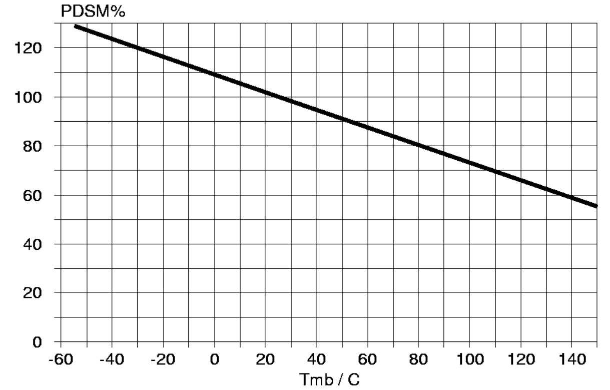


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ˚C) = f(T_{mb})$

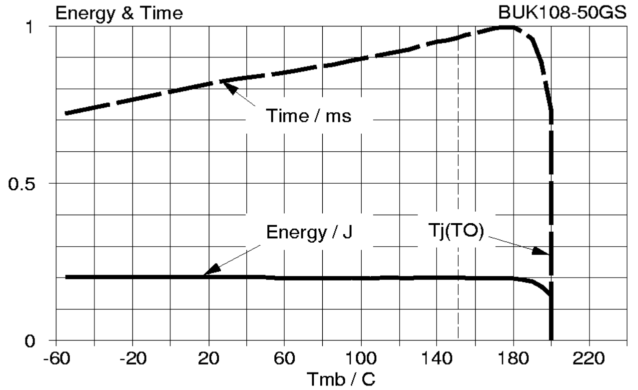


Fig.14. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{IS} = 10$ V; SC load = 30 mΩ

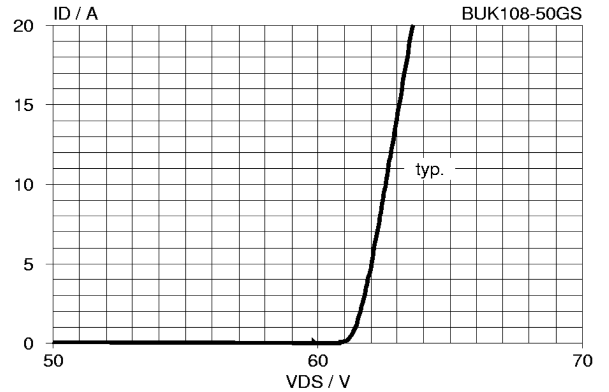


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

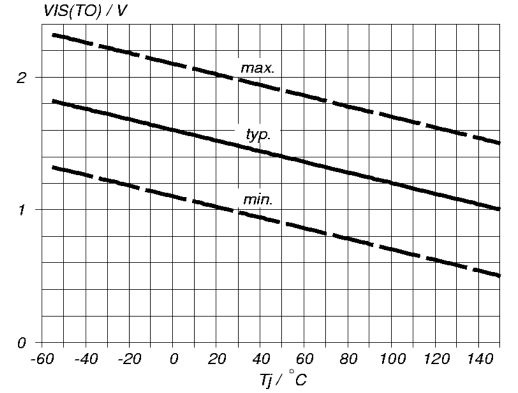


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

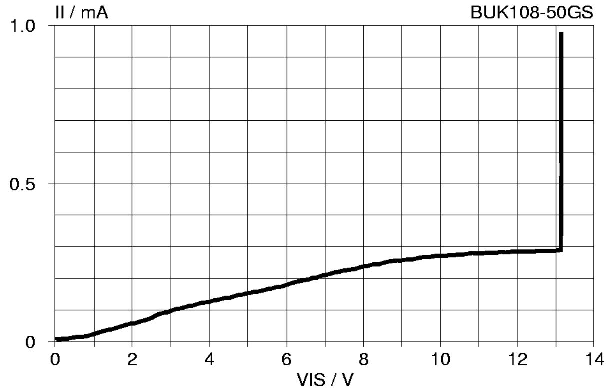


Fig.17. Typical DC input characteristics, $T_j = 25$ ˚C. $I_{IS} = f(V_{IS})$; normal operation

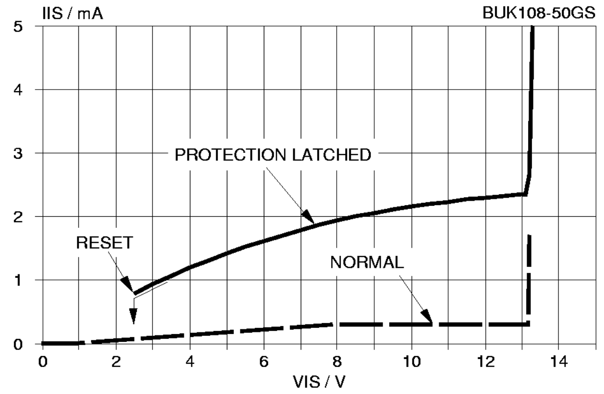


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

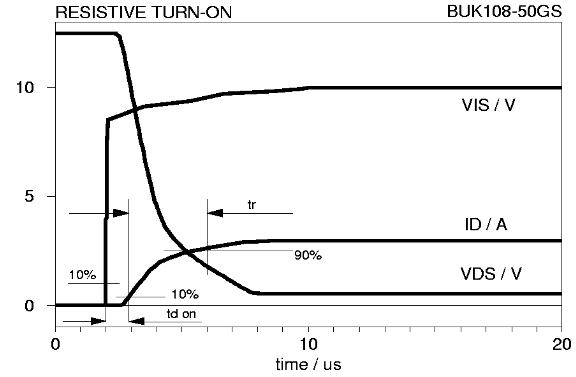


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 ˚C.

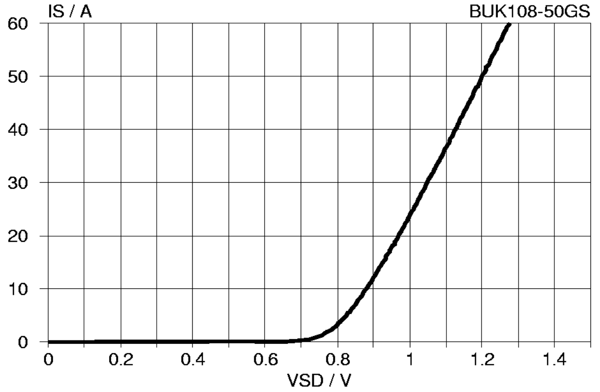


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

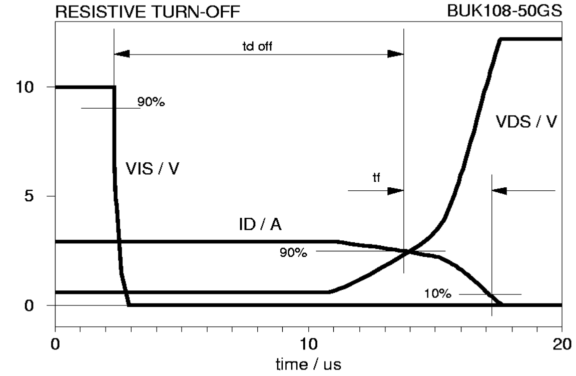


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 ˚C.

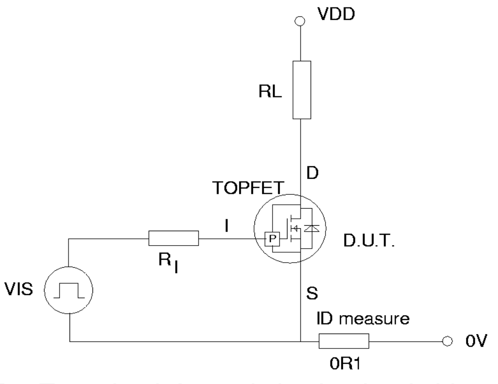


Fig.20. Test circuit for resistive load switching times.

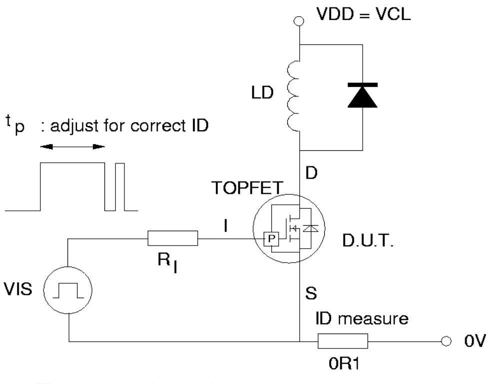


Fig.23. Test circuit for inductive load switching times.

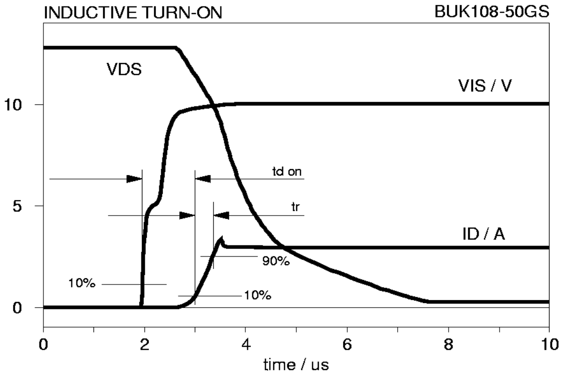


Fig.24. Typical switching waveforms, inductive load.
V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 ˚C.

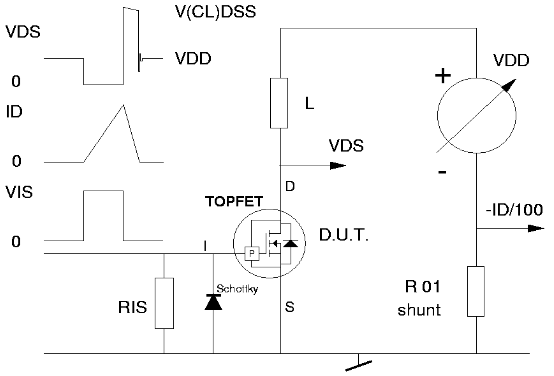


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

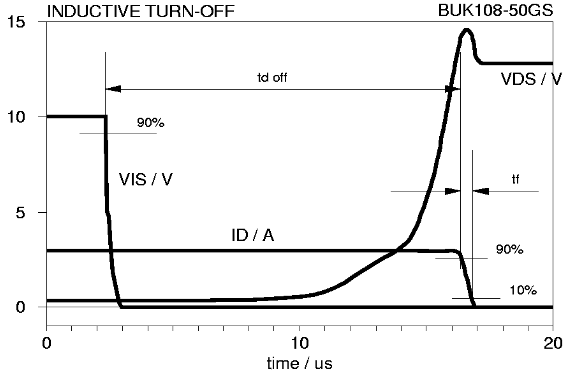


Fig.25. Typical switching waveforms, inductive load.
V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 ˚C.

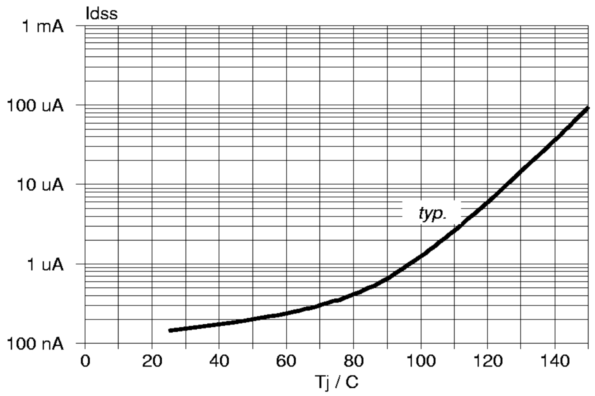


Fig.28. Typical off-state leakage current.
$I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

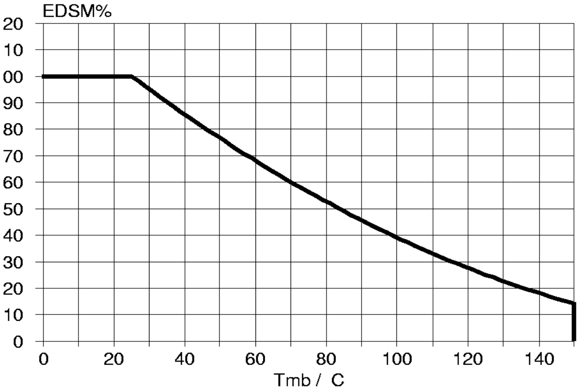


Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 10 V

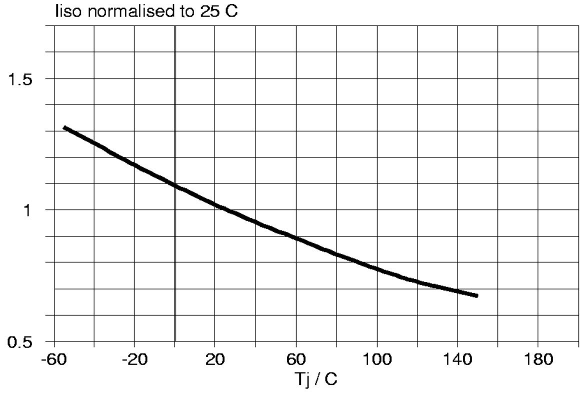


Fig.29. Normalised input current (normal operation).
$I_{IS}/I_{IS}25$ ˚C = $f(T_j)$; V_{IS} = 10 V

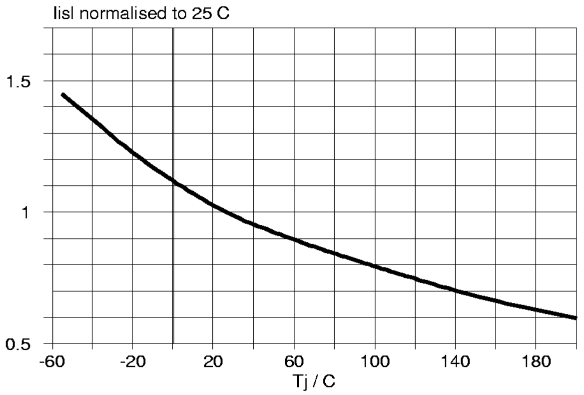


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; $V_{IS} = 10$ V

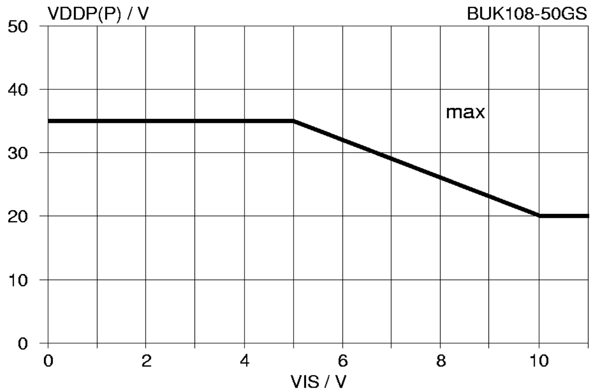


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^{\circ}C$

MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

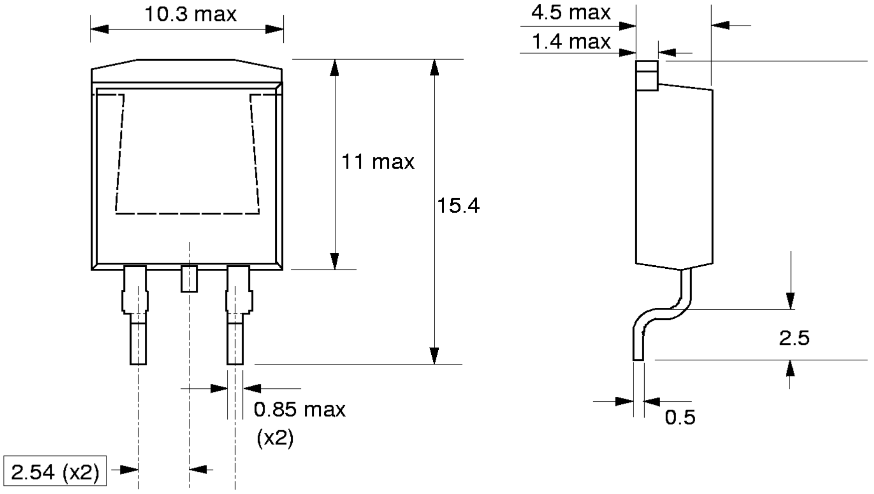


Fig.32. SOT404 : centre pin connected to mounting base.

Notes

1. Epoxy meets UL94 V0 at 1/8".

MOUNTING INSTRUCTIONS

Dimensions in mm

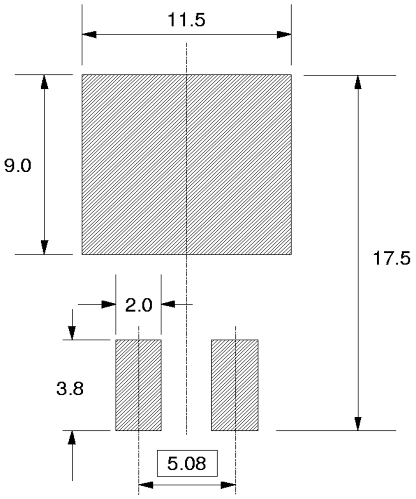


Fig.33. SOT404 : minimum pad sizes for surface mounting.

Notes

1. Plastic meets UL94 V0 at 1/8".