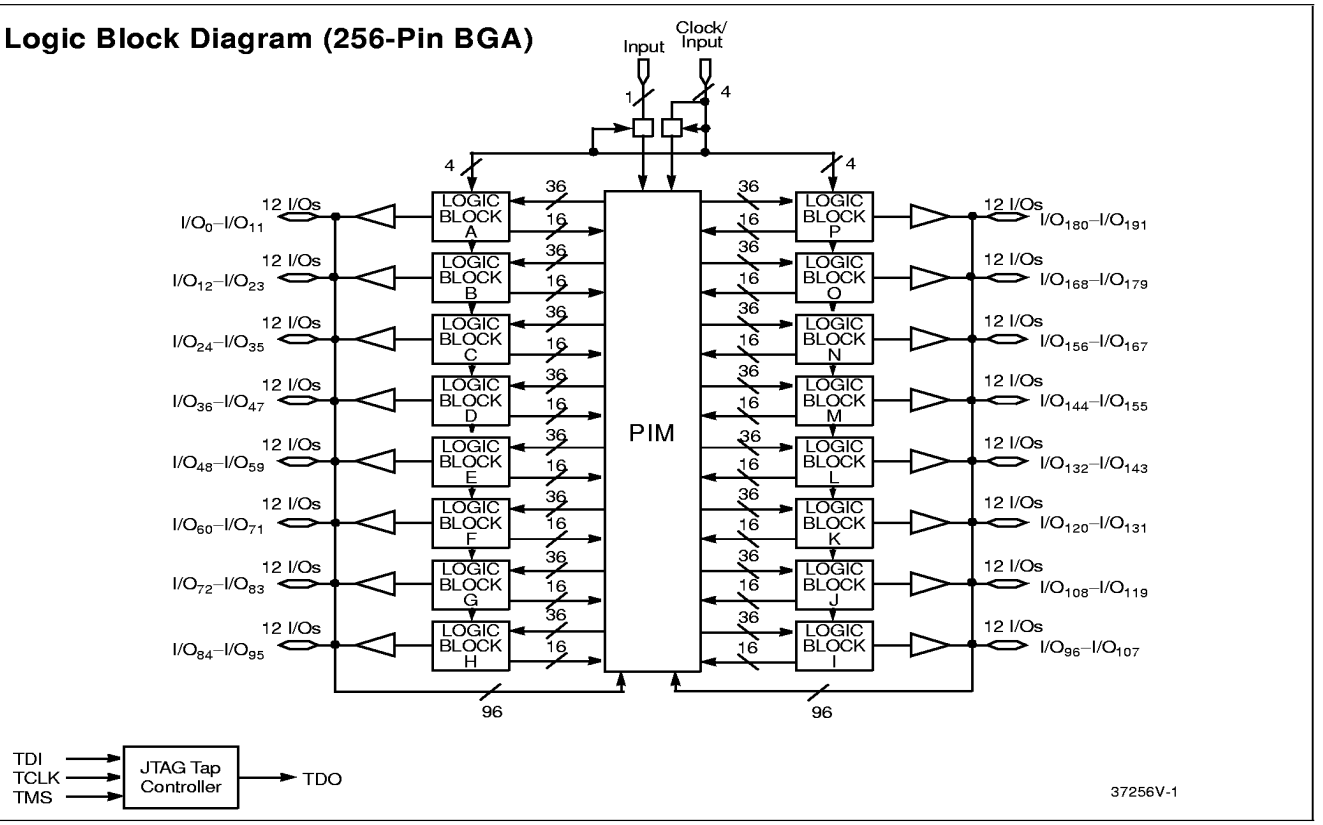
CY37256V

UltraLogic™ 3.3V 256-Macrocell ISR™ CPLD

Features

- 256 macrocells in sixteen logic blocks
- 3.3V In-System Reprogrammable™ (ISR™)
  - JTAG-compliant on-board programming
  - Design changes don't cause pinout changes
  - Design changes don't cause timing changes
- IEEE standard 3.3V operation
  - 3.3V ISR
  - 5V tolerant
- Up to 192 I/Os
  - Plus 5 dedicated inputs including 4 clock inputs
- High speed
  - t_{PD} = 12 ns
  - t_S = 7.0 ns
  - t_{CO} = 6.0 ns
- Product-term clocking
- IEEE 1149.1 JTAG boundary scan
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- User-Programmable Bus Hold capabilities on all I/Os
- Simple Timing Model
- PCI compliant[1]
- Available in 160-Pin TQFP, 208-Pin PQFP, and 256-Lead BGA packages
- Pinout compatible with the CY37256, CY37128/37128V, CY37192/37192V, CY37384/37384V, CY37512/37512V

Logic Block Diagram (256-Pin BGA)



Selection Guide

	CY37256V-100	CY37256V-66
Maximum Propagation Delay, t_{PD} (ns)	12	20
Minimum Set-Up, t_S (ns)	7	10
Maximum Clock to Output, t_{CO} (ns)	6	10
Typical Supply Current, I_{CC} (mA) in Low Power Mode	120	120

Note:
1. Due to the 5V tolerant nature of the I/Os, the I/Os are not clamped to V_{CC}, and PCI V_{IH} = 2V.

Functional Description

The CY37256V is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the CY37256V is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

# of Pins	# Buried Macrocells	# I/O Macrocells	Package Types
160	128	128	TQFP
208	96	160	PQFP
256	64	192	BGA

For a more detailed description of the architecture and features of the CY37256V see the Ultra37000 family data sheet.

Fully Routable with 100% Logic Utilization

The CY37256V is designed with a robust routing architecture which allows utilization of the entire device with a fixed pinout. This makes Ultra37000 optimal for implementing on-board design changes using ISR without changing pinouts.

Simple Timing Model

The CY37256V features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

Low-Power Operation

Each Logic Block of the CY37256V can be configured as either High-Speed (default) or Low-Power. In the Low-Power Mode, the logic block consumes approximately 50% less power and slows down by t_{LP}.

Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at 1V/ns max. There is a nominal delay for I/Os using the slow edge rate mode.

In System Reprogramming

The CY37256V can be programmed in system using IEEE 1149.1 compliant JTAG programming protocol. The CY37256V can also be programmed on a number of traditional parallel programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for UltraISR cable and software specifications, refer to the Ultra37000 ISR Programming Kit data sheet (CY3700i).

User-Programmable Bus Hold

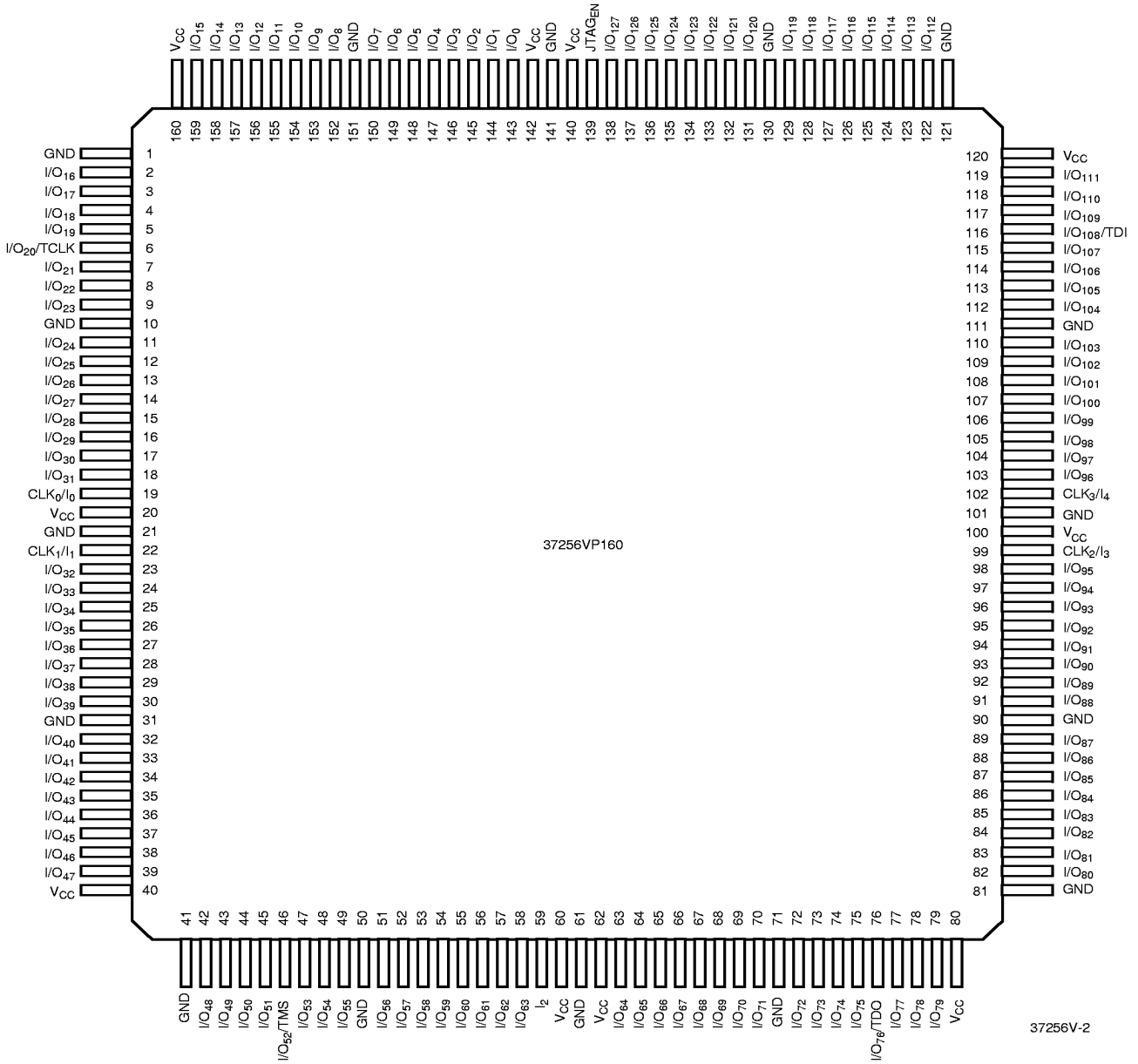
All outputs of the CY37256V can either be configured into bus hold mode or left floating. When in bus hold mode, the undriven outputs retain their last value with a weak latch. This feature allows the designer the flexibility of either eliminating or including external pull-up/pull-down resistors. Enabling this feature affects all I/Os simultaneously.

Design Tools

Development software for the CY37256V is available from Cypress's *Warp*™ or third-party bolt-in software packages as well as a number of third-party development packages. Please refer to the *Warp* or third-party tool support data sheets for further information.

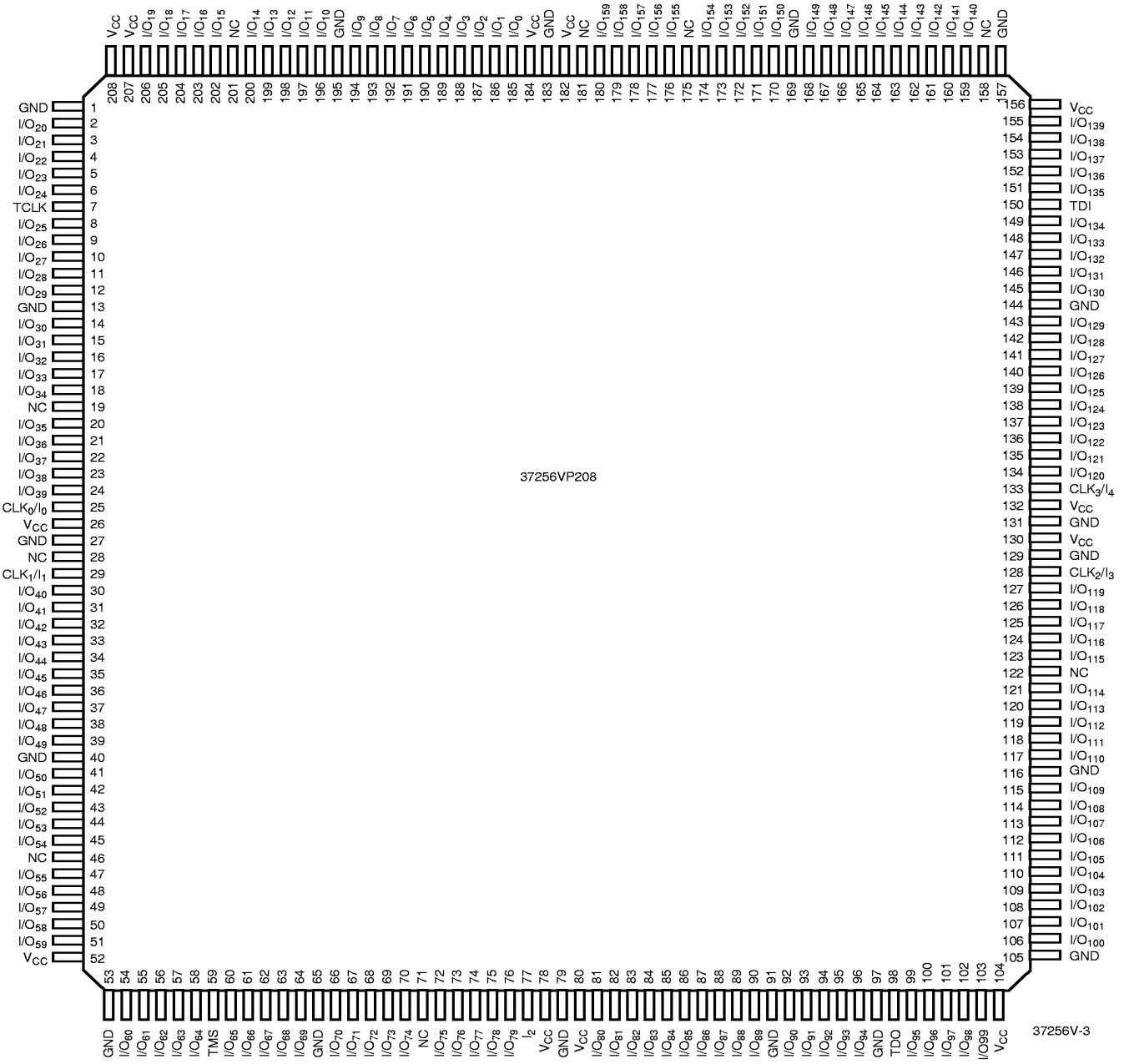
Pin Configurations

160-Pin TQFP
Top View



Pin Configurations (continued)

208-Pin PQFP
Top View



Pin Configurations (continued)

256-Ball BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O_{21}	NC	I/O_{16}	I/O_{12}	I/O_9	I/O_7	I/O_4	I/O_0	I/O_{190}	I/O_{189}	I/O_{186}	I/O_{182}	NC	I/O_{178}	I/O_{175}	NC	NC	I/O_{169}	I/O_{168}	A
B	I/O_{23}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{15}	I/O_{11}	I/O_8	I/O_5	I/O_1	I/O_{191}	I/O_{187}	I/O_{185}	I/O_{181}	NC	NC	I/O_{174}	I/O_{171}	I/O_{170}	NC	I/O_{166}	B
C	NC	NC	I/O_{22}	NC	I/O_{17}	I/O_{14}	I/O_{10}	I/O_6	I/O_2	NC	I/O_{188}	I/O_{184}	I/O_{180}	I/O_{179}	I/O_{176}	I/O_{173}	I/O_{172}	I/O_{167}	I/O_{165}	I/O_{162}	C
D	I/O_{24}	NC	NC	GND	NC	V_{CCO}	I/O_{13}	GND	I/O_3	NC	V_{CC}	I/O_{183}	GND	I/O_{177}	V_{CCO}	NC	GND	I/O_{164}	TDI	I/O_{160}	D
E	I/O_{27}	I/O_{26}	I/O_{25}	NC													I/O_{163}	I/O_{161}	I/O_{159}	I/O_{156}	E
F	I/O_{30}	TCK	I/O_{28}	V_{CCO}													V_{CCO}	I/O_{158}	NC	I/O_{154}	F
G	I/O_{33}	I/O_{32}	I/O_{31}	I/O_{29}													I/O_{157}	I/O_{155}	I/O_{153}	I/O_{152}	G
H	I/O_{35}	NC	I/O_{34}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{151}	I/O_{150}	I/O_{149}	H
J	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{36}				GND	GND	GND	GND	GND	GND				I/O_{148}	I/O_{147}	I/O_{146}	I/O_{145}	J
K	I/O_{42}	I/O_{40}	I/O_{41}	V_{CC}				GND	GND	GND	GND	GND	GND				I/O_{144}	CLK_3/I_4	NC	NC	K
L	I/O_{43}	I/O_{44}	I/O_{45}	I/O_{46}				GND	GND	GND	GND	GND	GND				V_{CC}	CLK_2/I_3	I/O_{143}	NC	L
M	I/O_{47}	CLK_0/I_0	CLK_1/I_1	I/O_{48}				GND	GND	GND	GND	GND	GND				I/O_{139}	I/O_{140}	I/O_{141}	I/O_{142}	M
N	I/O_{49}	I/O_{50}	I/O_{51}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{136}	I/O_{137}	I/O_{138}	N
P	I/O_{52}	I/O_{53}	I/O_{55}	I/O_{58}													I/O_{131}	I/O_{133}	I/O_{134}	I/O_{135}	P
R	I/O_{54}	I/O_{56}	I/O_{59}	V_{CCO}													V_{CCO}	I/O_{130}	NC	I/O_{132}	R
T	I/O_{57}	I/O_{60}	I/O_{62}	I/O_{65}													I/O_{124}	I/O_{127}	I/O_{128}	I/O_{129}	T
U	I/O_{61}	I/O_{63}	I/O_{66}	GND	I/O_{76}	V_{CCO}	I/O_{82}	GND	I/O_{91}	V_{CC}	I/O_{98}	I/O_{102}	GND	I/O_{112}	V_{CCO}	NC	GND	I/O_{123}	I/O_{122}	I/O_{126}	U
V	I/O_{64}	I/O_{67}	I/O_{69}	I/O_{75}	I/O_{78}	I/O_{81}	I/O_{85}	I/O_{88}	I/O_{92}	I_2	I/O_{97}	I/O_{101}	I/O_{105}	I/O_{109}	I/O_{113}	TDO	I/O_{114}	I/O_{117}	I/O_{121}	I/O_{125}	V
W	I/O_{68}	I/O_{70}	I/O_{72}	I/O_{74}	I/O_{79}	I/O_{83}	I/O_{86}	I/O_{89}	I/O_{93}	I/O_{95}	I/O_{96}	I/O_{100}	I/O_{104}	I/O_{107}	I/O_{110}	NC	NC	I/O_{115}	I/O_{118}	I/O_{120}	W
Y	I/O_{71}	I/O_{73}	I/O_{77}	TMS	I/O_{80}	I/O_{84}	I/O_{87}	I/O_{90}	I/O_{94}	NC	NC	I/O_{99}	I/O_{103}	I/O_{106}	I/O_{108}	I/O_{111}	NC	NC	I/O_{116}	I/O_{119}	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

***NOTE: Center pins must be connected to GND to aid thermal dissipation.**

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 3.0V to 3.6V

Current into Outputs ..... 8 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to + 90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to + 125°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

Shaded areas contain advance information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4			V
			I_{OH} = –3 mA (Mil)[4]				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]			0.5	V
			I_{OL} = 6 mA (Mil)[4]				
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[5]		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[5]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND, or V_{CC}		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled		–50		50	µA
I_{JTAG}	$JTAG_{EN}$ Leakage Current	V_I = 3.6V			120		µA
I_{OS}	Output Short Circuit Current[6, 7]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Inductance[7]

Parameter	Description	Test Conditions	160-lead TQFP	208-lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	9	11	nH

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.
3. T_A is the "instant on" case temperature.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
6. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

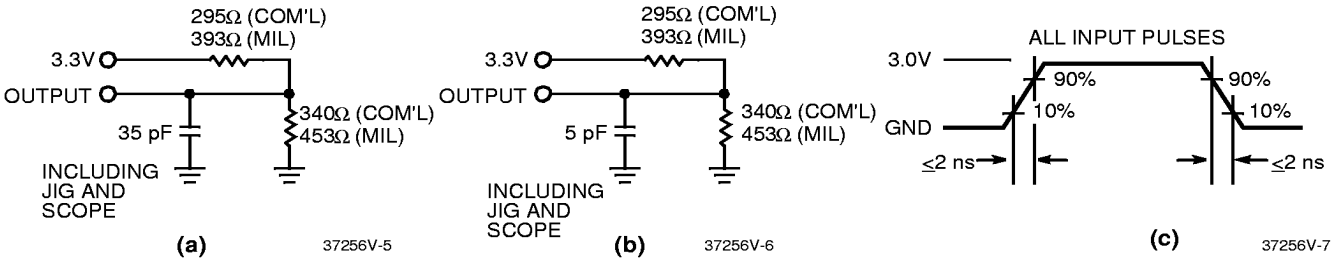
Capacitance[7]

Parameter	Description	Test Conditions	Commercial Devices	Military Devices	Unit
$C_{I/O}$	Maximum Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	8	12	pF
C_{CLK}	Maximum Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	12	pF

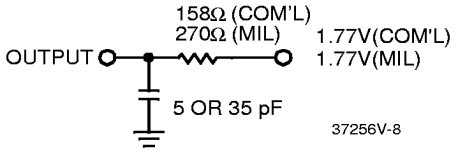
Endurance Characteristics[7]

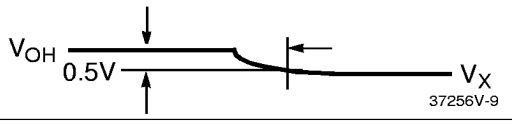
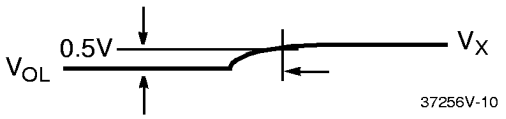
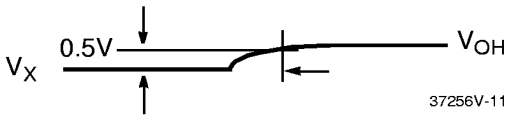
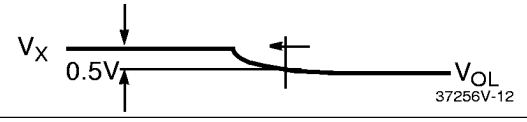
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter[8]	V_X	Output Waveform–Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Note:

8. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[9]

Parameter	Description	37256V-100		37256V-66		Unit
		Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters						
t_{PD}[10, 11]	Input to Combinatorial Output		12		20	ns
t_{PDL}[10, 11]	Input to Output Through Transparent Input or Output Latch		16.5		22	ns
t_{PDLL}[10, 11]	Input to Output Through Transparent Input and Output Latches		17		24	ns
t_{EA}[10, 11]	Input to Output Enable		16		24	ns
t_{ER}[10]	Input to Output Disable		16		24	ns
Input Register Parameters						
t_{WL}	Clock or Latch Enable Input LOW Time[7]	3		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[7]	3		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2.5		4		ns
t_{IH}	Input Register or Latch Hold Time	2.5		4		ns
t_{ICO}[10, 11]	Input Register Clock or Latch Enable to Combinatorial Output		16		24	ns
t_{ICOL}[10, 11]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		26	ns
Synchronous Clocking Parameters						
t_{CO}[11]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output		6		10	ns
t_S[10]	Set-Up Time from Input to Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	7		10		ns
t_H	Register or Latch Data Hold Time	0		0		ns
t_{CO2}[10, 11]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)		16		24	ns
t_{SCS}[10]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	10		15		ns
t_{SL}[10]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	12		15		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	0		0		ns
Product Term Clocking Parameters						
t_{COPT}[10, 11]	Product Term Clock or Latch Enable (PTCLK) to Output		13		20	ns
t_{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	3		6		ns
t_{HPT}	Register or Latch Data Hold Time	3		6		ns
t_{ISPT}[10]	Set-Up Time for Buried Register Used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)		–2		–2	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time		11		19	ns

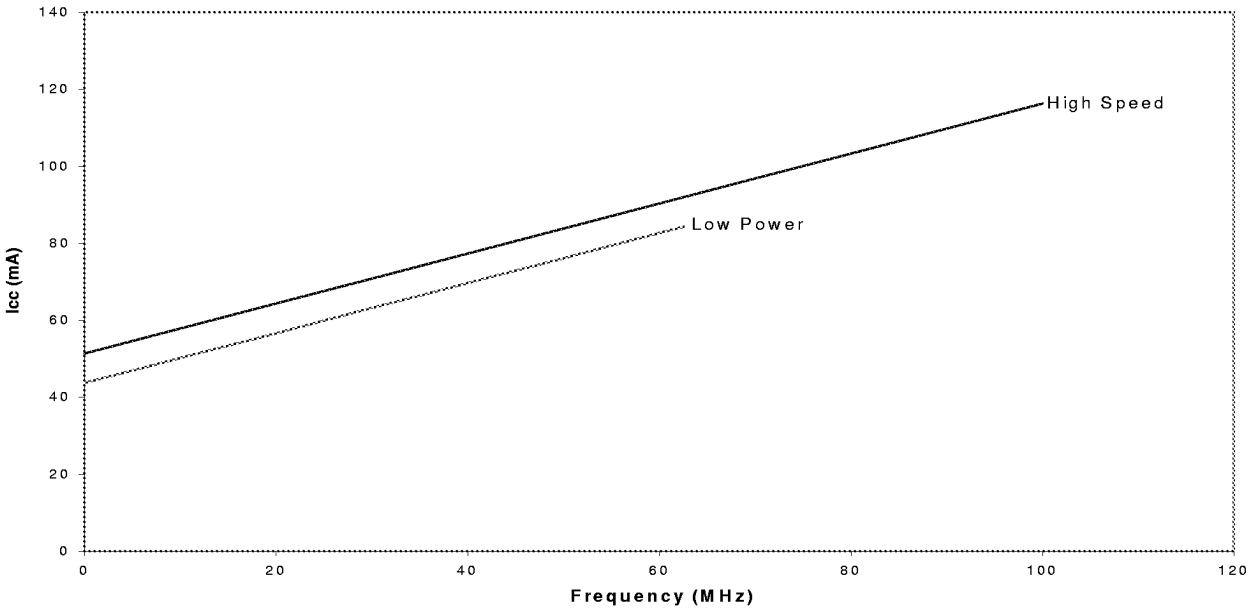
Notes:

9. All AC parameters are measured with 2 outputs switching and 35-pF AC Test Load.
10. Logic Blocks operating in low-power mode, add t_{LP} to this spec.
11. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.

Switching Characteristics Over the Operating Range[9] (continued)

Parameter	Description	37256V-100		37256V-66		Unit
		Min.	Max.	Min.	Max.	
t_{CO2PT}[10, 11]	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)		21		30	ns
Pipelined Mode Parameters						
t_{ICS}[10]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	10		15		ns
Operating Frequency Parameters						
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[7]	100		66.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[7]	143		100		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)[7]	80		50		MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[7]	100		66.7		MHz
Reset/Preset Parameters						
t_{RW}	Asynchronous Reset Width[7]	12		20		ns
t_{RR}[10]	Asynchronous Reset Recovery Time[7]	14		22		ns
t_{RO}[10, 11]	Asynchronous Reset to Output		18		26	ns
t_{PW}	Asynchronous Preset Width[7]	12		20		ns
t_{PR}[10]	Asynchronous Preset Recovery Time[7]	14		22		ns
t_{PO}[10, 11]	Asynchronous Preset to Output		18		26	ns
User Option Parameters						
t_{LP}	Low Power Adder		6		4	ns
t_{SLEW}	Slow Output Slew Rate Adder		2		2	ns
JTAG Timing Parameters						
$t_{S\ JTAG}$	Set-Up time from TDI and TMS to TCK[7]	0		0		ns
$t_{H\ JTAG}$	Hold Time on TDI and TMS[7]	20		20		ns
$t_{CO\ JTAG}$	Falling Edge of TCK to TDO[7]		20		20	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency[7]		20		20	MHz

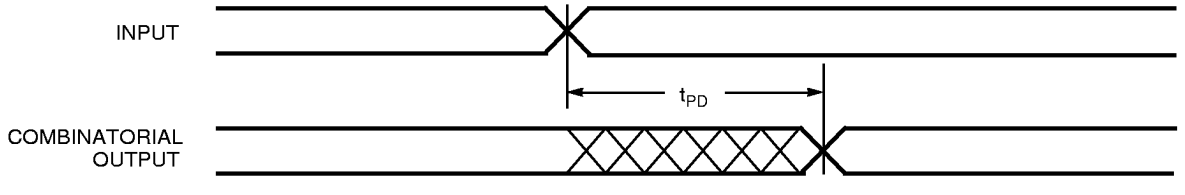
Typical I_{cc} Characteristics



The typical pattern is a 16 bit up counter, per logic block, with outputs disabled.
V_{cc} = 3.3V, T_A = Room Temperature

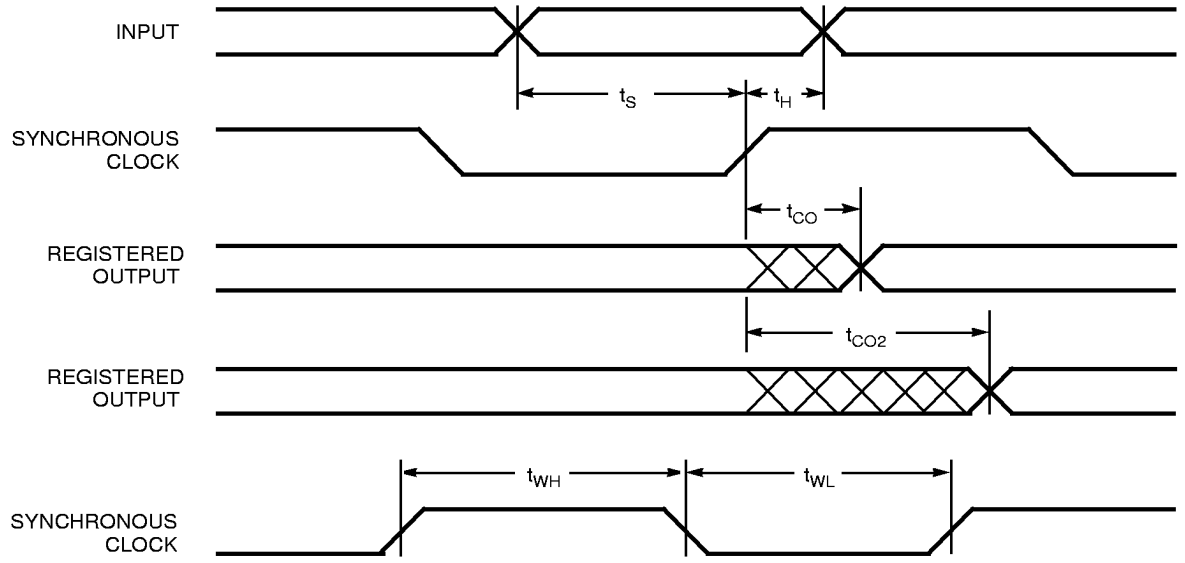
Switching Waveforms

Combinatorial Output



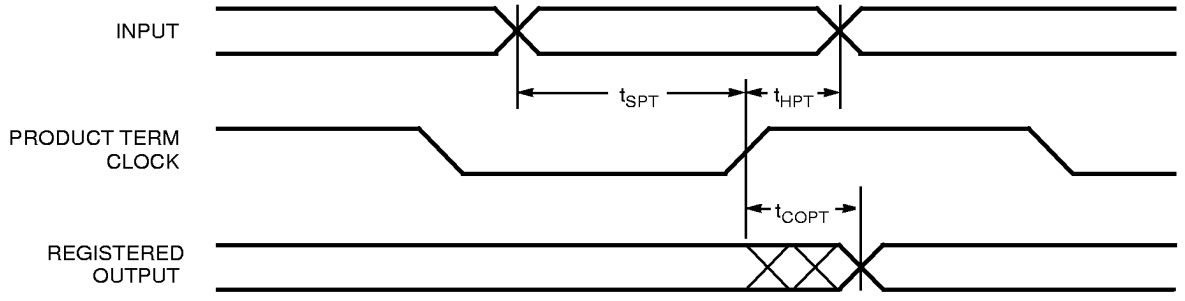
37256V-13

Registered Output with Synchronous Clocking



37256V-14

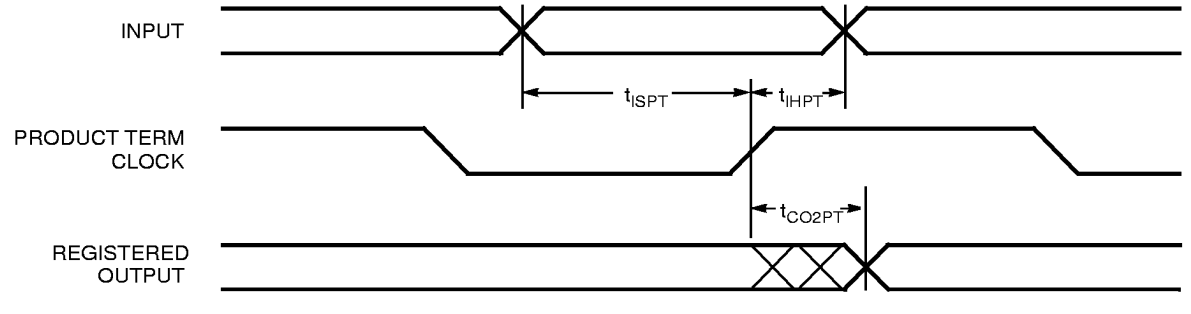
Registered Output with Product Term Clocking Input Going Through the Array



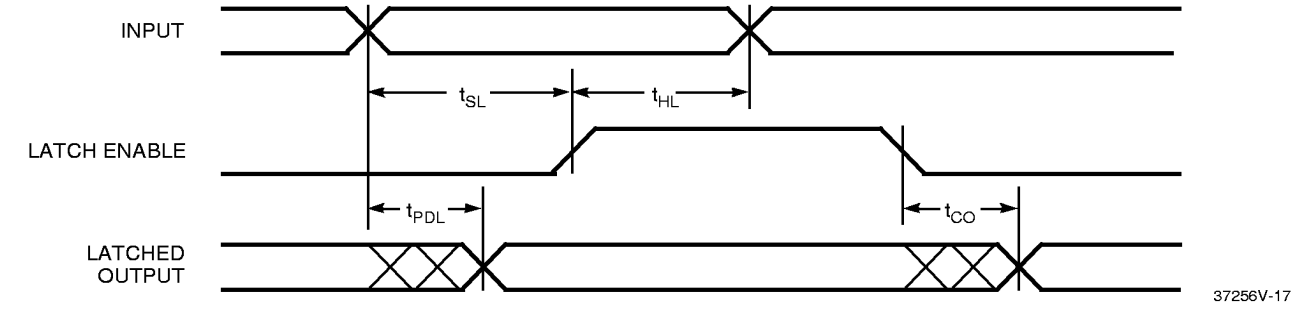
37256V-15

Switching Waveforms (continued)

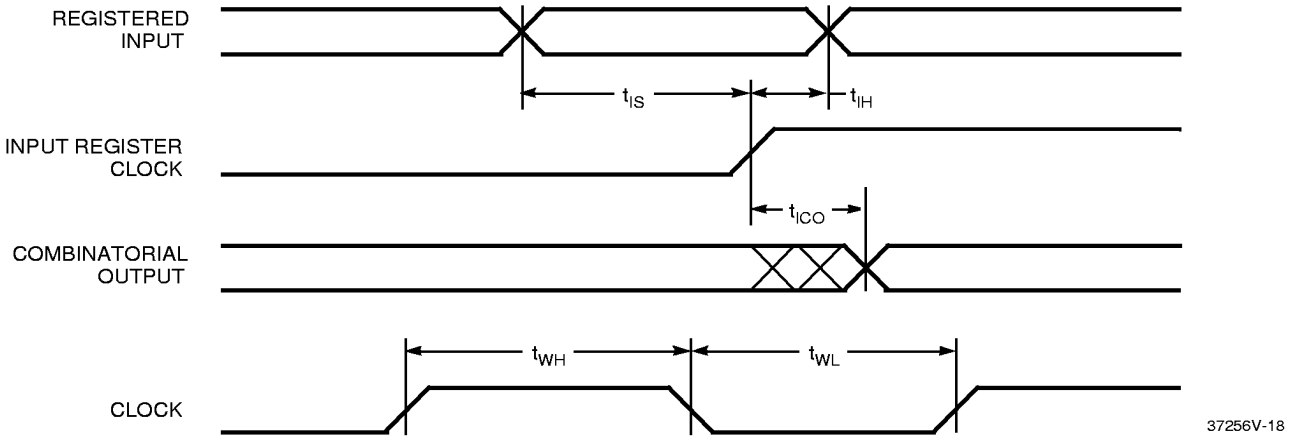
Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register



Latched Output

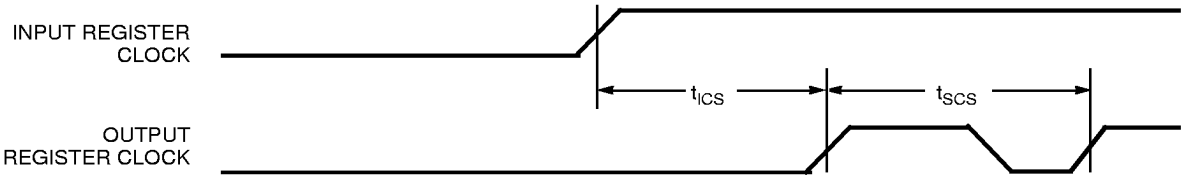


Registered Input



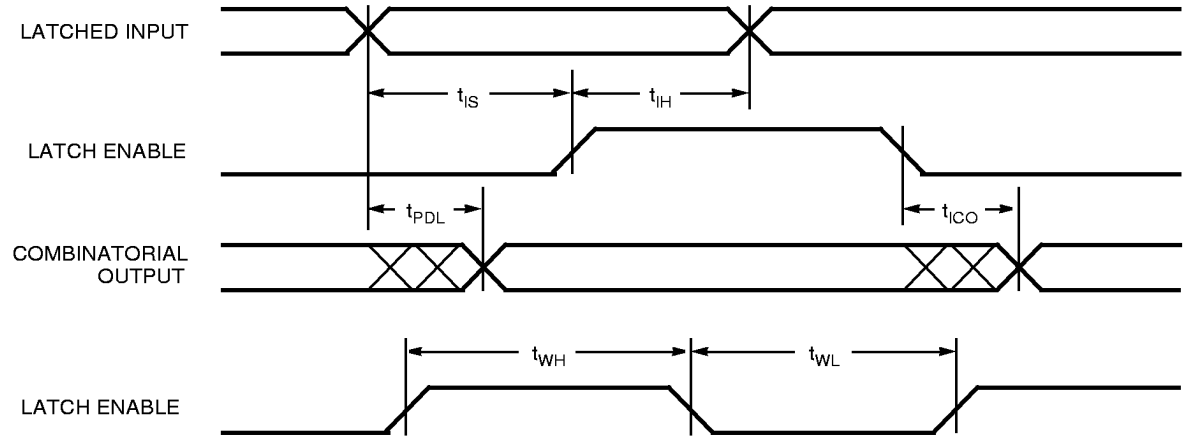
Switching Waveforms (continued)

Clock to Clock



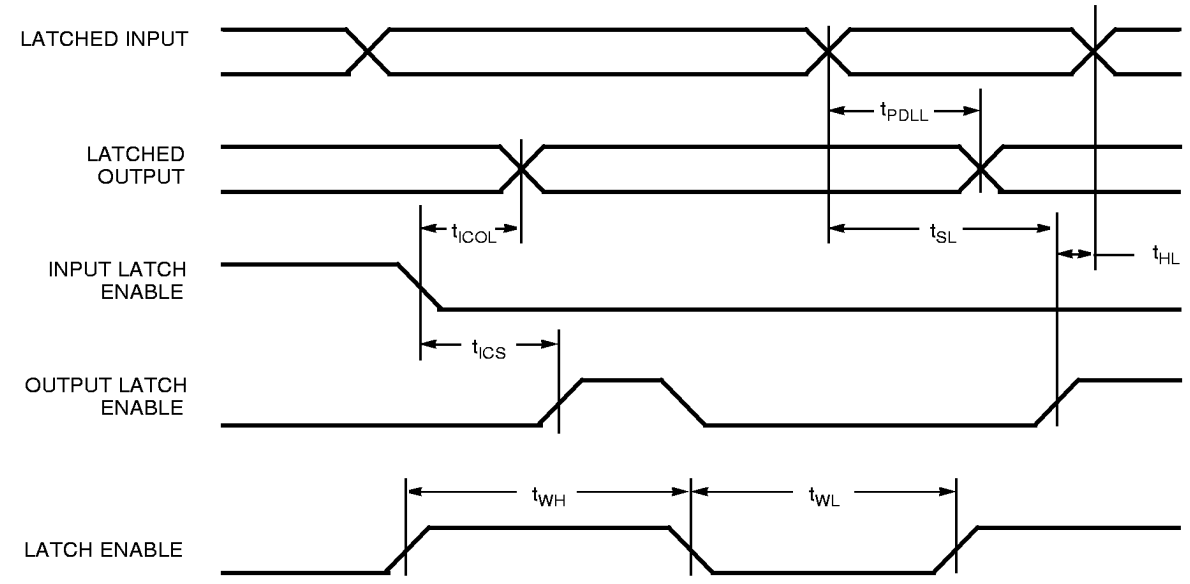
37256V-19

Latched Input



37256V-20

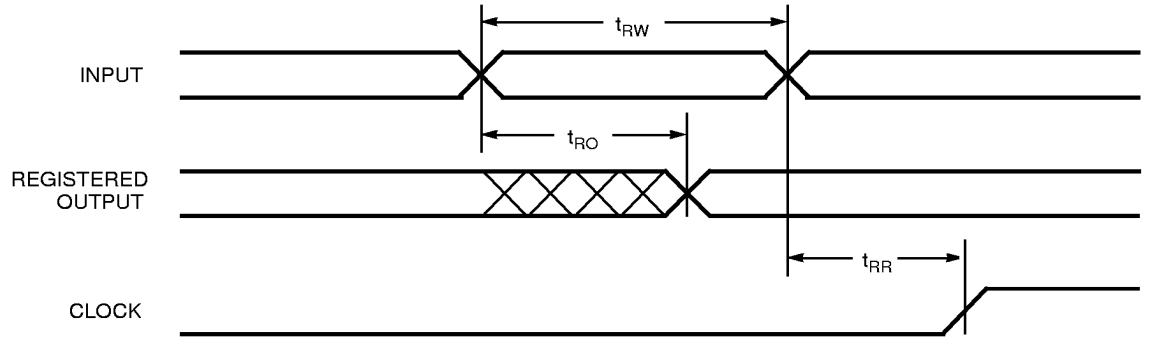
Latched Input and Output



37256V-21

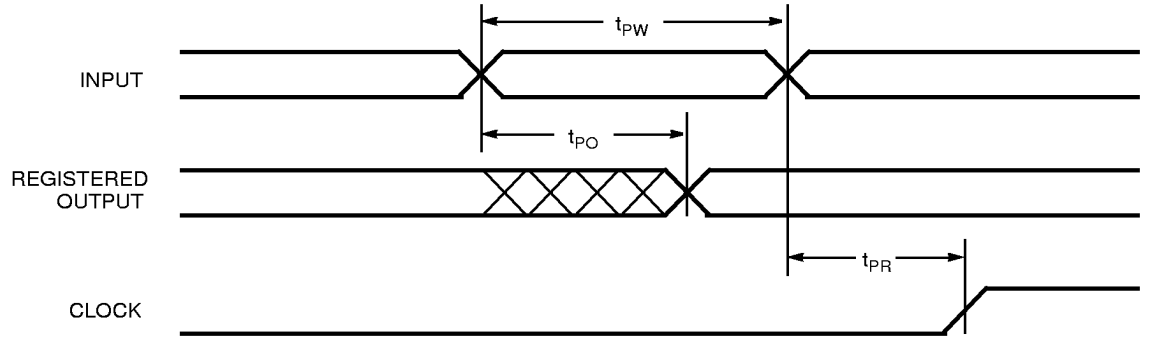
Switching Waveforms (continued)

Asynchronous Reset



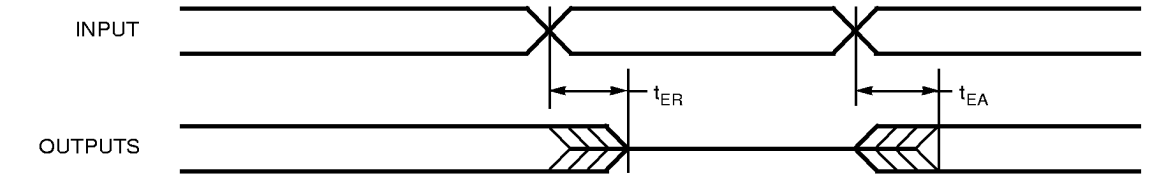
37256V-22

Asynchronous Preset



37256V-23

Output Enable/Disable



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Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY37256VP160-100AC	A160	160-Pin Thin Quad Flatpack	Commercial
	CY37256VP208-100NC	N208	208-Pin Plastic Quad Flatpack	
	CY37256VP256-100BGC	BG256	256-Pin Ball Grid Array	
66	CY37256VP160-66AC	A160	160-Pin Thin Quad Flatpack	Commercial
	CY37256VP208-66NC	N208	208-Pin Plastic Quad Flatpack	
	CY37256VP256-66BGC	BG256	256-Pin Ball Grid Array	
	CY37256VP160-66AI	A160	160-Pin Thin Quad Flatpack	Industrial
	CY37256VP208-66NI	N208	208-Pin Plastic Quad Flatpack	
	CY37256VP256-66BGI	BG256	256-Pin Ball Grid Array	
	CY37256VP160-66UMB	U162	160-Lead Ceramic Quad Flatpack	Military

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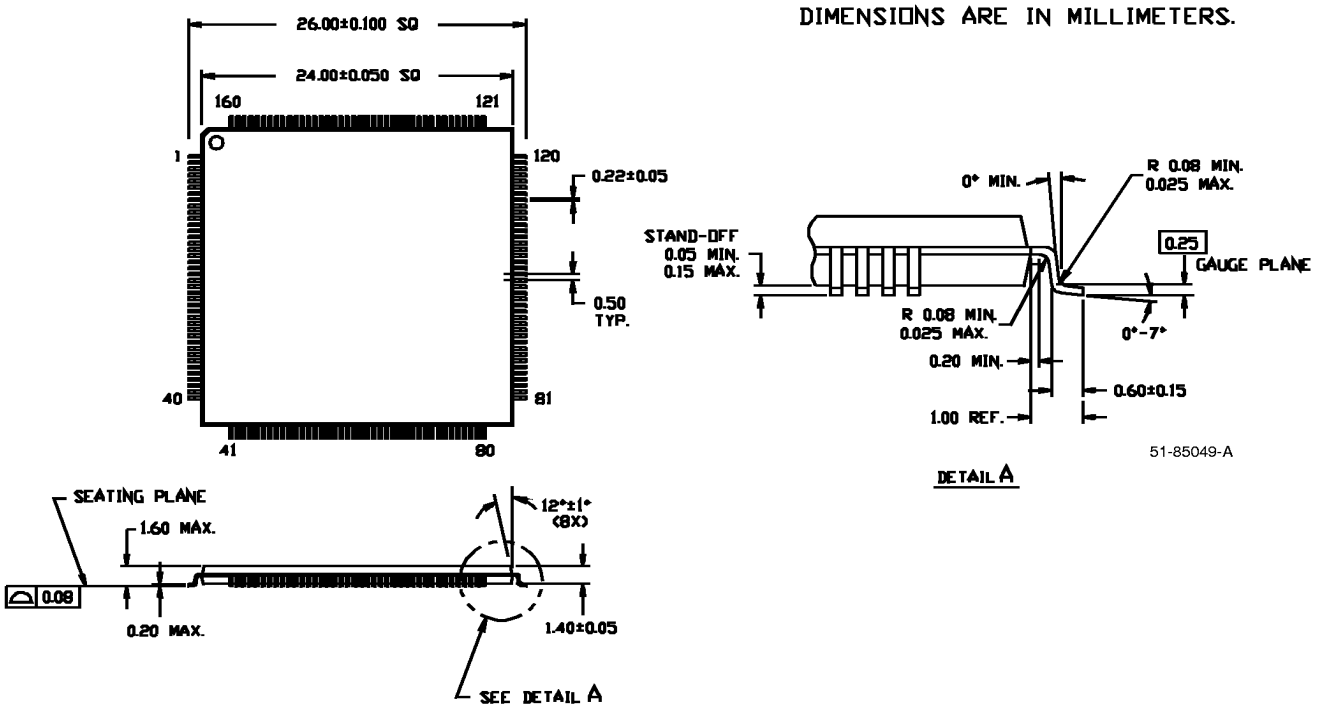
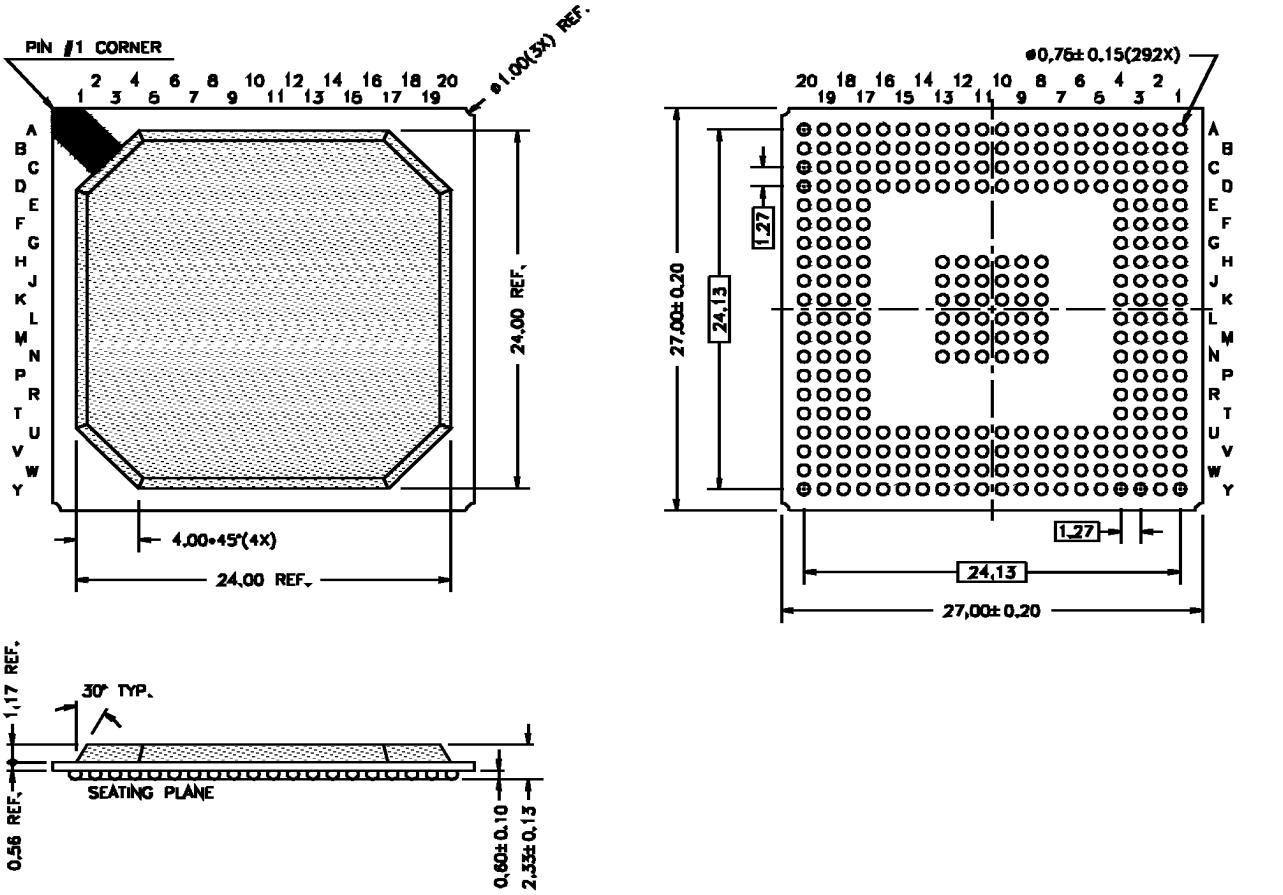
Package Diagrams

160-Pin Thin Plastic Quad Flat Pack (TQFP) A160



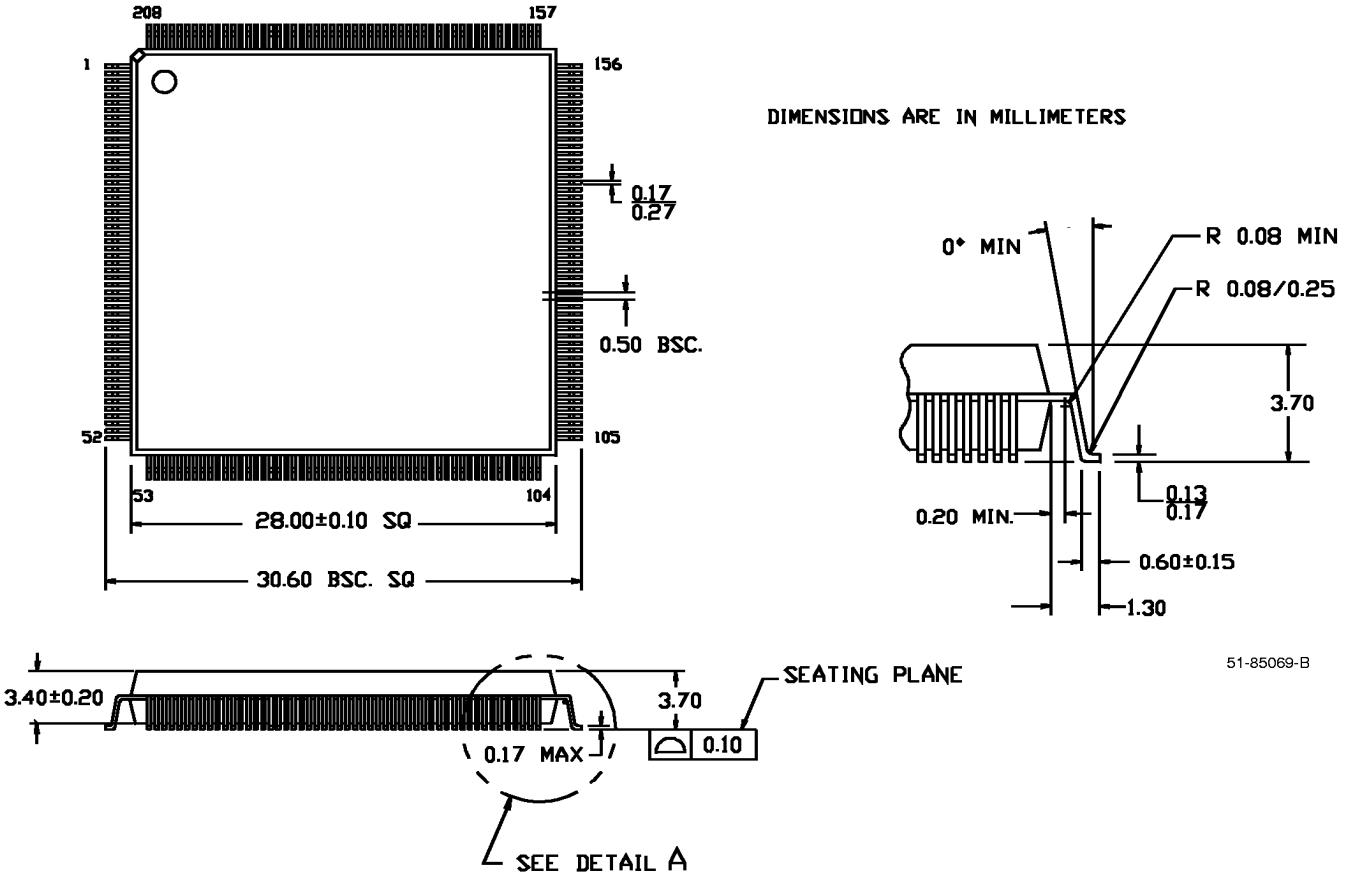
Package Diagrams (continued)

256-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG256



Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



Package Diagrams (continued)

160-Lead Ceramic Quad Flatpack (Cavity Up) U162