



1M x 1 Static RAM

Features

- High speed
— $t_{AA} = 12$ ns
- CMOS for optimum speed/power
- Low active power
— 825 mW
- Low standby power
— 275 mW
- 2.0V data retention (optional)
— 100 μ V
- Automatic power-down when deselected
- TTL-compatible inputs and outputs

Functional Description

The CY7C107A is a high-performance CMOS static RAM organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

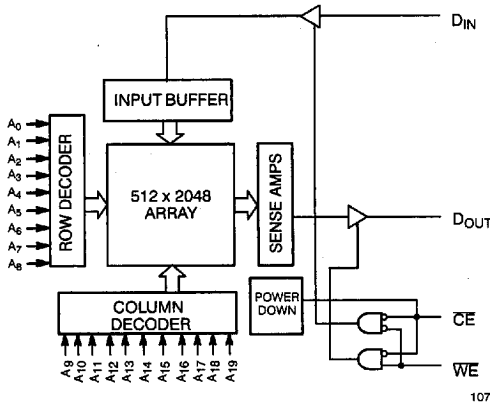
Writing to the device is accomplished by taking chip enable (CE) and write enable (WE) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A₀ through A₁₉).

Reading from the device is accomplished by taking chip enable (CE) LOW while write enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output (D_{OUT}) pin.

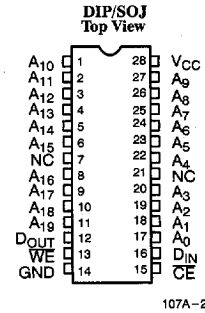
The output pin (D_{OUT}) is placed in a high-impedance state when the device is deselected (CE HIGH) or during a write operation (CE and WE LOW).

The CY7C107A is available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C107A-12	7C107A-15	7C107A-20	7C107A-25	7C107A-35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	150	135	125	120	110
	Military		145	135	130	120
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage on V _{CC} Relative to GND ^[1]	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[1]	-0.5V to V _{CC} +0.5V
DC Input Voltage ^[1]	-0.5V to V _{CC} +0.5V
Current into Outputs (LOW)	20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C107A-12		7C107A-15		7C107A-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.3	2.2	V _{CC} +0.3	2.2	V _{CC} +0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0mA, f = f _{MAX} = 1/trc	Com'l	150		135		125	mA
			Mil			145		135	
I _{SB1}	Automatic CE Power-Down Current - TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l	50		40		30	mA
			Mil			40		30	
I _{SB2}	Automatic CE Power-Down Current - CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f=0	Com'l	2		2		2	mA
			Mil			2		2	

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[3] (continued)

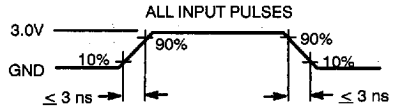
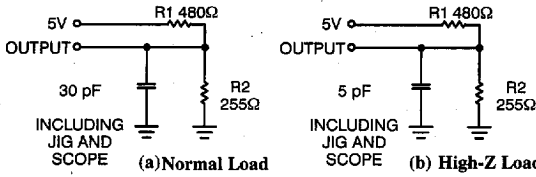
Parameter	Description	Test Conditions	7C107A-25		7C107A-35		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0mA, f = f _{MAX} = 1/trc	Com'l	120		110	mA
			Mil		130	120	
I _{SB1}	Automatic CE Power-Down Current - TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l	30		25	mA
			Mil		30	25	
I _{SB2}	Automatic CE Power-Down Current - CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f=0	Com'l	2		2	mA
			Mil		2	2	

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN} : Addresses	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	7	pF
C _{IN} : Controls			10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

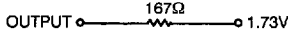
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

AC Test Loads and Waveforms


107A-3

107A-4

Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics^[3,6] Over the Operating Range

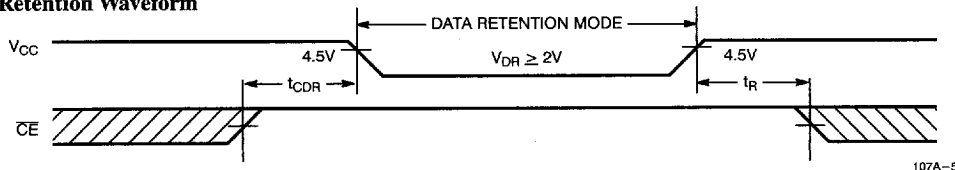
Parameter	Description	7C107A-12		7C107A-15		7C107A-20		7C107A-25		7C107A-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25		35	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[7]	3		3		3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[7,8]		6		7		8		10		10	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE^[9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	\overline{CE} LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3		3		3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7,8]		6		7		8		10		10	ns

Notes:

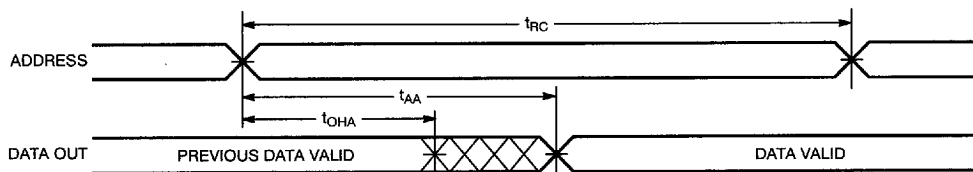
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range (L Version Only)

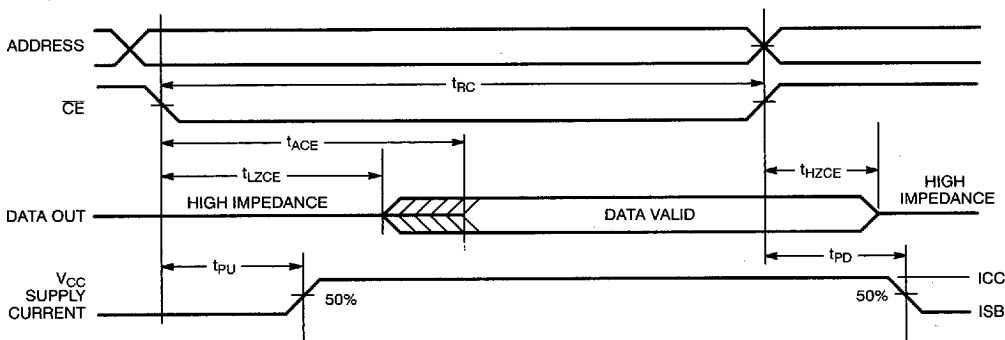
Parameter	Description	Conditions ^[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Data Retention		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3$ or $V_{IN} \leq 0.3V$		50		70	μA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0		0		ns
$t_R^{[5]}$	Operation Recovery Time		t_{RC}		t_{RC}		ns

Data Retention Waveform


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Switching Waveforms
Read Cycle No. 1^[11, 12]


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Read Cycle No. 2^[12, 13]


107A-7

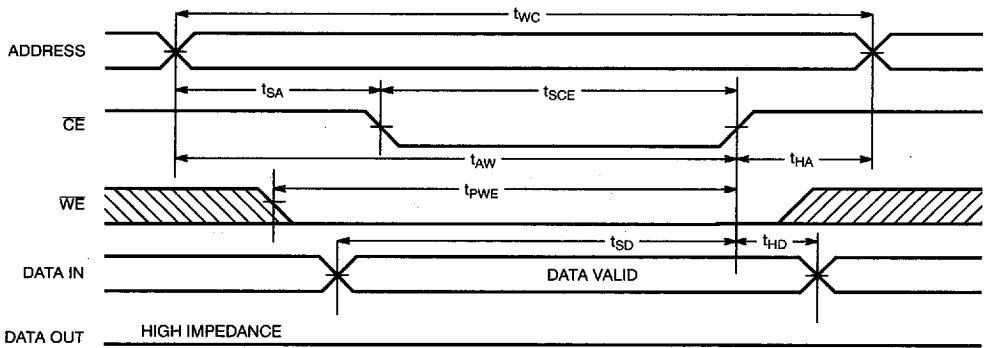
Notes:

 10. No input may exceed $V_{CC} + 0.5V$.

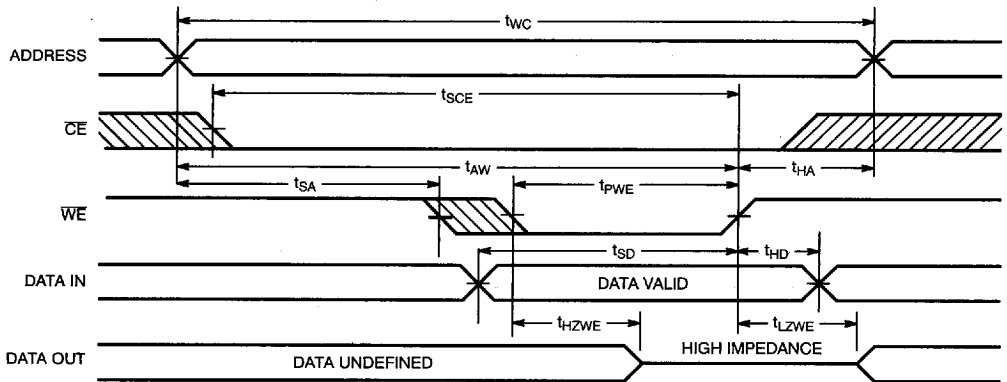
 11. Device is continuously selected, $\overline{CE} = V_{IL}$.

 12. \overline{WE} is HIGH for read cycle.

 13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE} Controlled)^[14]


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Write Cycle No. 2 (\overline{WE} Controlled)^[14]


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Truth Table

\overline{CE}	\overline{WE}	D _{OUT}	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	Write	Active (I_{CC})

Note:

 14. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C107A-12PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A-12VC	V28	28-Lead (400-Mil) Molded SOJ	
15	CY7C107A-15PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A-15VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A-15DMB	D42	28-Lead (400-Mil) CerDIP	
20	CY7C107A-20PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A-20VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A-20DMB	D42	28-Lead (400-Mil) CerDIP	Military
25	CY7C107A-25PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A-25VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A-25DMB	D42	28-Lead (400-Mil) CerDIP	Military
35	CY7C107A-35PC	P41	28-Lead (400-Mil) Molded DIP	Commercial
	CY7C107A-35VC	V28	28-Lead (400-Mil) Molded SOJ	
	CY7C107A-35DMB	D42	28-Lead (400-Mil) CerDIP	Military

Contact factory for "L" version availability.

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11