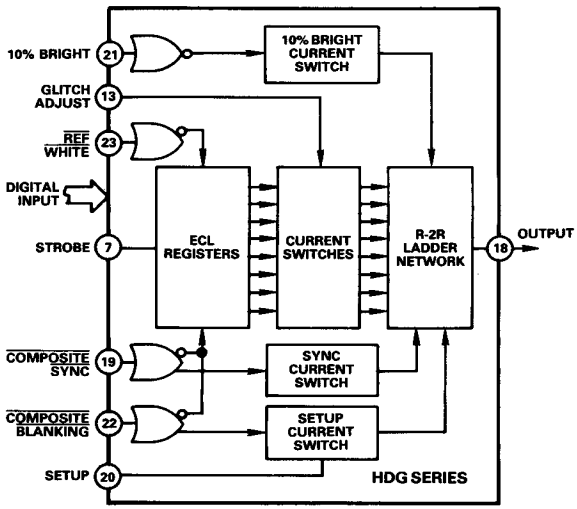
Hybrid Video Digital-to-Analog Converters

HDG Series

FEATURES
- **Update Rates to 150MHz**
- **Low Glitch Energy**
- **Complete Composite Inputs**
- **Single −5.2V Power Supply**
- **Military Temperature Range Available**

APPLICATIONS
- **Raster Scan Displays**
- **Color Graphics**
- **Analytical Instrumentation**
- **TV Video Reconstruction**

HDG SERIES FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

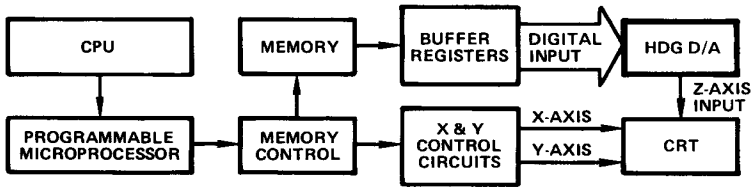
The HDG-Series D/A Converters have become the standard of comparison for fast-settling D/As with complete composite inputs. The HDG-0805 is an eight-bit (256 Gray levels) device.

All versions have complete composite controls, including self-contained, digitally-controlled sync and blanking; and a reference white control input to help assure compatibility with EIA Standards RS-170, RS-330, and RS-343-A. Their performance is enhanced even more with a 10% bright input capability.

Output inpedance is 75 ohms and their full-scale output current is capable of developing standard video levels across video loads. In addition to all of these characteristics which make them easy to incorporate into circuits, the need for a single −5.2V power supply also adds to their attractiveness.

The model number without a suffix designates the "original" HDG Series D/A Converter and is housed in 24-pin metal packages. The model numbers with suffixes make use internally of the Analog Devices Model AD9700 to obtain better performance; these devices are housed in ceramic DIP packages.

The "BD" and "BW" versions in the newer (suffixed) units are close equivalents to the original design, but a number of advantages accrue by using the newer units. Note particularly the parameters for linearity tempco; strobe input loading; Composite Sync and Composite Blanking outputs; Power Supply Rejection Ratio (PSRR); supply current; and power dissipation. Conversely, the original design is slightly better in terms of voltage settling time, glitch energy, and output compliance.



Typical Raster Scan Display System

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDG-0805	HDG-0805BD/ BW/SD
RESOLUTION	Bits	8	8
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Voltage (adjustable)	mV	2.5	*
Current (adjustable)	μA	67	*
ACCURACY			
(GS = Gray Scale; FS = Full-Scale)			
Linearity	± % GS	0.2	*
Differential Linearity	± % GS, max	0.2	*
Zero Offset (Initial)			
Voltage	mV, max	0.9	*
Monotonicity		Guaranteed	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C (max)	20 (35)	15 (30)
Gain	ppm/°C (max)	50 (125)	*
Zero Offset	ppm/°C (max)	10 (15)	*
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[1]			
Settling Time (0V to FS GS change)	% GS;	0.4	*
Voltage	ns (max)	8 (10)	9 (11)
Update Rate[2]	MHz (min)	150 (125)	*
Slew Rate	V/μs	200	*
Rise Time	ns	2	*
Glitch Energy[3]	pV-s	50	80
DIGITAL DATA INPUTS			
Logic Compatibility		ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading (each bit)		5pF and 50kΩ to −5.2V	*
STROBE INPUT			
Logic Compatibility		ECL	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		50pF and 5kΩ to −5.2V	5pF and 50kΩ to −5.2V
Setup Time (Data)	ns, min	2.5	*
Hold Time (Data)	ns, min	1.5	*
Propagation Delay	ns (max)	3 (4)	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS			
Logic Compatibility		ECL	*
Logic Levels			
"1"	V (min/max).	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		5pF and 50kΩ to −5.2V	*
SPEED PERFORMANCE – CONTROL INPUTS			
Settling Time to 10% of Final Value for:			
10% Bright	ns (max)	8 (10)	*
Reference White	ns (max)	8 (10)	*
Composite Sync	ns (max)	8 (10)	*
Composite Blanking	ns (max)	8 (10)	*
SETUP CONTROL			
Ground	mV (IRE Units)	0 (0)	*
Open	mV (IRE Units)	71 (10)	*
−5.2V	mV (IRE Units)	142 (20)	*
ANALOG OUTPUT			
GS Current	mA (± 1%)	0 to −17	*
GS Voltage[4]	mV	0 to −637.5	*
Compliance	V	−1.1 to +1.1	−1.2 to +0.1
Internal Impedance	Ω (min/max)	75 (71/79)	*

Parameter	Units	HDG-0805	HDG-0805BD/ BW/SD
OUTPUT – $\overline{\text{REFERENCE WHITE}}$[5]			
Current			
Logic "1"	mA (±4%)	Normal Operation	*
Logic "0"	mA (±4%)	0 or −1.9	*
Voltage			
Logic "1"	mV (±4%)	Normal Operation	*
Logic "0"	mV (±4%)	0 or −71	
OUTPUT – 10% BRIGHT[6]			
Current			
Logic "1"	mA (±5%)	−1.9	*
Logic "0"	mA (±5%)	0	*
Voltage			
Logic "1"	mV (±5%)	−71	*
Logic "0"	mV (±5%)	0	*
OUTPUT – $\overline{\text{COMPOSITE SYNC}}$[6,7]			
Current			
Logic "1"	mA (±4%)	0	*
Logic "0"	mA (±4%)	−7.6	*
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	−285	*
OUTPUT – $\overline{\text{COMPOSITE BLANKING}}$[6,7] (Assumes Setup is Open, Which is Equivalent to 10 IRE Units)			
Current			
Logic "1"	mA (±4%)	0	*
Logic "0"	mA (±4%)	−1.9	*
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	−71	*
POWER REQUIREMENTS			
−5.2V ±0.25V[8]	mA (max)	320 (360)	125 (140)
Power Supply Rejection Ratio	%/%	1/1	0.005/1
Power Dissipation	mW (max)	1665 (1875)	650 (730)
TEMPERATURE RANGE			
Operating (Case)[9]	°C	−25 to +85	* (BD and BW)
Operating ("SD" Case)	°C		−55 to +125
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[10]			
Junction to Air, θ_{JA} (free air)	°C/W, max	45	*
Junction to Case, θ_{JA}	°C/W, max	12	*
MTBF[11]			
Mean Time Between Failures	Hours		3.23×10^5
PACKAGE OPTIONS[12]			
M-24A		HDG-0805	
DH-24B			HDG-0805BD HDG-0805BW HDG-0805SD

For applications assistance, phone Computer Labs Division at (919) 668-9511

NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50%) points) is not included.
[2]Minimum update rates limited by full-scale settling time for useable number of bits.
Units can be updated to 150MHz with settling degradation.
[3]Glitch can be reduced with glitch adjustment.
[4]LSB value used for calibration causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform; both values are well within the output and EIA Standard RS-170 tolerances.
[5]Effect on analog output of logic "0" at $\overline{\text{Reference White}}$ input depends on 10% Bright signal input (See Table I).
[6]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray scale analog output at Pin 18 (See Table I).
[7]$\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ control signals reset input registers. $\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ should not be operated simultaneously with $\overline{\text{Reference White}}$.
[8]Power supply must have less than 5mV p-p ripple.
[9]Operating temperature −55°C to +125°C on "SD" units.
[10]Maximum junction temperature = 150°C.
[11]Calculated for HDG-0805SDB using MIL HNBK-217; Ground Fixed; +25°C Ambient.
[12]See Section 14 for package outline information.
* Specification same as HDG-0405.
**Specifications same as HDG-0405BD/BW/SD.
Specifications subject to change without notice.

PIN DESIGNATIONS

Pin	Function	Pin	Function
12	GROUND	13	GLITCH ADJUST
11	BIT 8 (LSB)	14	GROUND
10	BIT 7	15	GROUND
9	BIT 6	16	GROUND
8	BIT 5	17	GROUND
7	STROBE	18	ANALOG OUTPUT
6	BIT 4	19	COMPOSITE SYNC
5	BIT 3	20	SETUP
4	BIT 2	21	10% BRIGHT
3	BIT 1 (MSB)	22	COMPOSITE BLANKING
2	−5.2V	23	REFERENCE WHITE
1	GROUND	24	−5.2V

NOTE: Connect Pins 1, 12, and 14–17 together and to low-impedance ground plane as close to case as possible.

USING HDG-SERIES UNIT FOR RASTER SCAN

Refer to the block diagram of the HDG-Series D/A Converter and the idealized composite output waveform.

The digital input bits represent the Gray Scale values (the discrete levels between Reference Black and Reference White) in a composite video signal. There are 256 (2^8) of these levels.

The input bits are applied to Pins 3–6 or Pins 8–11 of the HDG-0805.

The output analog signal (at Pin 18) will be a function of these digital inputs. The output will also be affected by the ECL levels at the control inputs of 10% Bright, $\overline{\text{Reference White}}$, $\overline{\text{Composite Sync}}$, and $\overline{\text{Composite Blanking}}$; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs, and various combinations of control inputs are selected.

Refer to Table I.

DIGITAL INPUTS VS. ANALOG OUTPUT

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	10% BRIGHT	$\overline{\text{REF. WHITE}}$	$\overline{\text{BLANKING}}$	$\overline{\text{COMP. SYNC}}$	ANALOG OUTPUT IN mV[1] (HDG-0805BD/BW/SD)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.5[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.5mV[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.5mV[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.5mV[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.5mV[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.5mV[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.5mV[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.5mV[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.5mV[4]

NOTES

[1] Values are for Gray Scale output of 8-bit D/A's.
[2] Setup (Pin 20) grounded. (0 IRE units)
[3] Setup (Pin 20) open. (10 IRE units)
[4] Setup (Pin 20) to −5.2V (20 IRE units)

Actual analog output value of −637.5mV is different from ideal value of −643mV because of LSB value used in calibration.

Table I. Digital Inputs vs. Analog Output