HT7606
Low Power PIR Controller

Features

- Low stand-by current: 30μA (Max.)
- Operating voltage: 4.5V~12V
- 24 DIP/SOP or 28 DIP/SOP
- Built-in amplifiers and comparators
- An LED trigger indicator
- Relay driver output
- TRIAC driver output
- Two ranges of adjustable output duration:
  - "Long" range: 48~1536 seconds
  - "Short" range: 4~128 seconds
- Beep before system active
- CDS input pin
- Mode selection input (Toggle)
- AC 2-wire system application

Applications

- PIR light controllers
- Motion detectors
- Burglar alarm systems
- Door bell systems

General Description

The HT7606 is a single-chip low power PIR (pyroelectric infrared) controller LSI implemented in the CMOS technology. The low power feature makes the chip suitable for either AC (2 wires) or battery powered applications.

The HT7606 is equipped with operational amplifiers, a comparator, a signal stretcher, a timer, zero cross, control circuit, a voltage regulator, and an on-chip oscillator. When the chip detects a PIR signal whose level is greater than the pre-set level of the comparator, the output drivers are activated to turn on an LED indicator, Relay, and TRIAC respectively. The turn on duration of the relay and TRIAC is divided into two ranges (long/short by bonding option), and is adjustable within the selected range. A CDS pin is provided to disable the system during daytime. The power-on delay can be set to 24, 40, 56, or 72 seconds by mask option. During the power-on delay time, the relay and LED outputs are disabled but the TRIAC outputs are on a 30% duty cycle. After the power-on delay, the BUZ pin outputs a group of 6 pulses, the TRIAC turns off, and the system is then ready to detect input signals.

The MODE pin is used to select the output mode between ON or PIR-AUTO (toggle, positive edge trigger).

The HT7606 is enclosed in either a 24 pin DIP/SOP or 28 pin DIP/SOP depending on the function offered.

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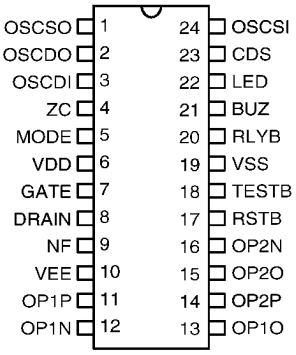
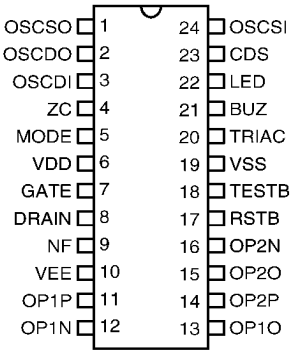
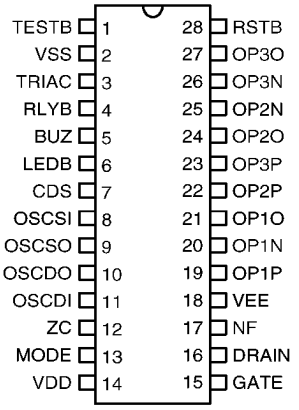
Pin Assignment



HT7606A (SHORT)
HT7606B (LONG)
Relay Version
– 24 DIP/SOP

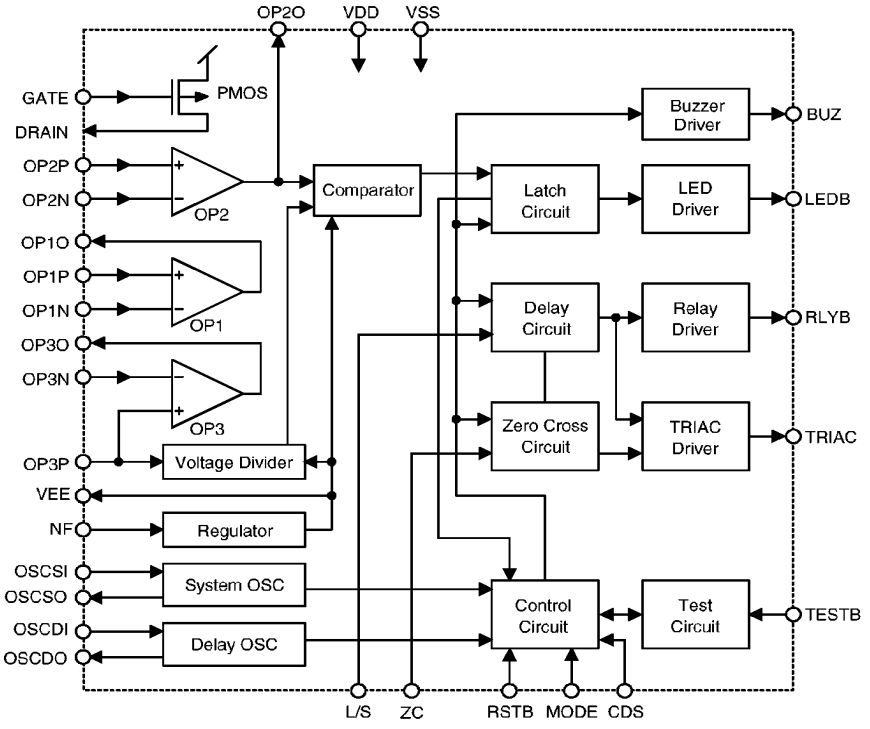


HT7606C (SHORT)
HT7606D (LONG)
TRIAC Version
– 24 DIP/SOP



HT7606S (SHORT)
HT7606L (LONG)
TRIAC Version
– 28 DIP/SOP

Block Diagram



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Pin Description

HT7606 24 Pin DIP/SOP Version

Pin No.	Pin Name		I/O	Internal Connection	Description
	A, B	C, D			
1	OSCSO		O	—	System oscillator output terminal (16KHz Typ.)
2	OSCDO		O	—	Delay oscillator output terminal The frequency can be altered by an external resistor.
3	OSCDI		I	—	Delay oscillator input terminal The frequency can be altered by an external resistor.
4	ZC		I	CMOS	Zero crossing input, schmitt trigger input
5	MODE		I	CMOS	ON or PIR-AUTO toggle selection input (positive edge trigger)
6	VDD		I	—	Positive power supply
7	GATE		I	PMOS IN	Independent PMOS gate terminal
8	DRAIN		O	—	Independent PMOS drain terminal
9	NF		I	CMOS	Negative feedback input of an internal regulator
10	VEE		O	NMOS	Output of an internal regulator This pin is set as output voltage externally.
11	OP1P		I	CMOS	Noninverting input of OP1
12	OP1N		I	CMOS	Inverting input of OP1
13	OP1O		O	NMOS	Output of OP1
14	OP2P		I	CMOS	Noninverting input of OP2, internally This pin is connected to the center of the comparator window.
15	OP2O		O	NMOS	Output of OP2 This pin is internally connected to a comparator.
16	OP2N		I	CMOS	Inverting input of OP2
17	RSTB		I	PMOS Pull-High	Chip reset input, low active
18	TESTB		I	Pull-High	Input low to this pin speeds up an internal counter by 64 times.
19	VSS		I	—	Negative power supply (GND)

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Pin No.	Pin Name		I/O	Internal Connection	Description
	A, B	C, D			
20		TRIAC	O	CMOS	Output to drive the TRIAC The output is a pulse output when active.
	RLYB				Output to drive an external transistor, active low
21	BUZ		O	CMOS	Output to drive a piezo buzzer
22	LEDB		O	NMOS Open Drain	Output to drive the LED, open drain, active low
23	CDS		I	CMOS	Input pin of CDS, schmitt trigger The input high can disable the outputs (RLYB and TRIAC).
24	OSCSI		I	—	Input terminal of a system oscillator (16KHz Typ.)

HT7606 28 Pin DIP/SOP Version

Pin No.	Pin Name	I/O	Internal Connection	Description
1	TESTB	I	Pull-High	Input low to this pin speeds up an internal counter by 64 times.
2	VSS	I	—	Negative power supply (GND)
3	TRIAC	O	CMOS	Output to drive the TRIAC The output is a pulse output when active.
4	RLYB	O	CMOS	Output to drive an external transistor, active low
5	BUZ	O	CMOS	Output to drive a piezo buzzer
6	LEDB	O	NMOS Open Drain	Output to drive the LED, open drain, active low.
7	CDS	I	CMOS	CDS input, schmitt trigger Its input high can disable the outputs (RLYB and TRIAC).
8	OSCSI	I	—	System oscillator input terminal (16KHz Typ.)
9	OSCSO	O	—	System oscillator output terminal (16KHz Typ.)
10	OSCDO	O	—	Delay oscillator output terminal The frequency can be altered by an external resistor.
11	OSCDI	I	—	Delay oscillator input terminal The frequency can be altered by an external resistor.
12	ZC	I	CMOS	Zero crossing input, schmitt trigger input

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Pin No.	Pin Name	I/O	Internal Connection	Description
13	MODE	I	CMOS	ON or PIR-AUTO toggle selection input (positive edge trigger)
14	VDD	I	—	Positive power supply
15	GATE	I	PMOS IN	Independent PMOS gate terminal
16	DRAIN	O	—	Independent PMOS drain terminal
17	NF	I	CMOS	Negative feedback input of an internal regulator
18	VEE	O	NMOS	Output of an internal regulator It is set as output voltage externally.
19	OP1P	I	CMOS	Noninverting input of OP1
20	OP1N	I	CMOS	Inverting input of OP1
21	OP1O	O	NMOS	Output of OP1
22	OP2P	I	CMOS	Noninverting input of OP2
23	OP3P	I	CMOS	Noninverting input of OP3 It's internally connected to the center of the comparator window.
24	OP2O	O	NMOS	Output of OP2 It's internally connected to a comparator.
25	OP2N	I	CMOS	Inverting input of OP2
26	OP3N	I	CMOS	Inverting input of OP3
27	OP3O	O	NMOS	Output of OP3
28	RSTB	I	PMOS Pull-High	Chip reset input, low active

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 13V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Operating Temperature.....–25°C to 70°C
Zero Crossing Current.....300μA
Storage Temperature.....–50°C to 125°C

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Electrical Characteristics

(Ta=25°C)

Symbol	Parameters	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	4.5	9	12	V
I_{STB}	Stand-by Current	9V	No load, OSC Off	—	20	30	μA
I_{OL4}	LED Pin Sink Current	9V	V_{OL}=0.9V	5	8	—	mA
I_{OL2}	RLYB Sink Current	9V	V_{OL}=0.9V	6	10	—	mA
I_{OH1}	TRIAC Source Current	9V	V_{OH}=8.1V	–2	–3.5	—	mA
I_{OL1}	TRIAC Sink Current	9V	V_{OL}=0.9V	15	40	—	mA
I_{OL5}	VEE Sink Current	9V	—	—	1000	—	μA
V_{TH}	CDS "H" Transfer Voltage	9V	—	—	6	—	V
V_{TL}	CDS "L" Transfer Voltage	9V	—	—	4	—	V
F_{OSCA}	System Osc. Frequency	9V	R=680KΩ	12.8	16	19.2	KHz
F_{OSCB}	Delay Osc. Frequency	9V	R=680KΩ	12.8	16	19.2	KHz
V_{IH}	"H" Input Voltage	—	—	$0.8V_{DD}$	—	—	V
V_{IL}	"L" Input Voltage	—	—	—	—	$0.2V_{DD}$	V
I_{OH2}	RLYB Source Current	9V	V_{OH}=8.1V	1.2	2	—	mA
I_{OH3}	BUZ Source Current	9V	V_{OH}=8.1V	–1.8	–3	—	mA
I_{OL3}	BUZ Sink Current	9V	V_{OL}=0.9V	6	12	—	mA

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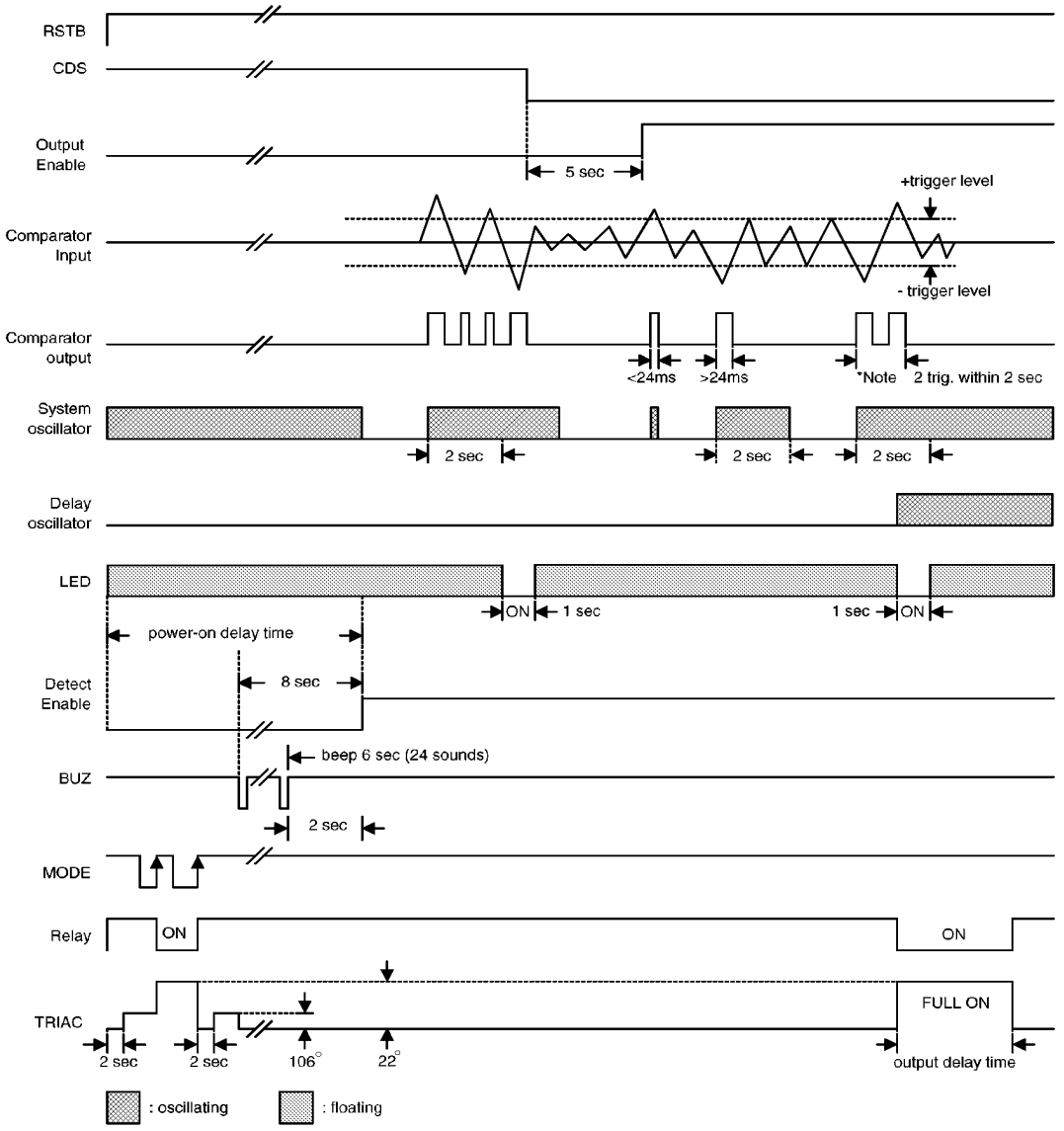
Trigger Timing



Note: The output is activated if the trigger signal conforms to the following criteria:

1. Two triggers occur within 2 seconds. (separation of 2 triggers ≥ 0.5 seconds).
2. The trigger signal sustain duration ≥ 0.5 seconds.

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Functional Description

NF, VEE

The VEE output is a regulated voltage for use in analog front end circuit, NF is the voltage feed-back to control the value of VEE.

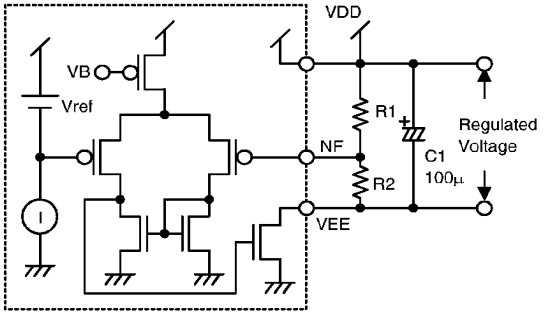

Fig.1 Regulator configuration

The configuration of an internal regulator is as shown. Vref provides a 1.45V ± 0.15V reference voltage. Selection of R1 or R2 can be made to obtain the desired value of VEE. A VEE of –4V with respect to VDD is suggested for normal applications. The value of VEE with respect to VDD can be calculated by the following equation:

$$VDD–VEE = Vref\left(\frac{R1+R2}{R1}\right)$$

The value of R1+R2 should be kept high enough to reduce current consumption. C1 is required for circuit stability.

OSCSI, OSCSO

OSCSI and OSCSO are system oscillator input and output pins. The system operating frequency is 16KHz for normal applications. If no trigger signal is input, the oscillator is turned off to reduce power consumption. At power-on, the oscillator is turned on until the warm-up time is over.

OSCDI, OSCDO

OSCDI and OSCDO are output delay time oscillator input and output pins. Once the chip detects a valid trigger input, the output device is

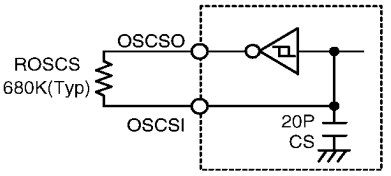

Fig.2 System oscillator

turned on with the duration controlled by the delay oscillator. The oscillating frequency can be adjusted to control the turn-on time. Lower oscillator frequency takes longer delay time. The following diagram shows the configuration of delay time oscillator.

$$T_{oscd} = RC \ln\left[\frac{V_p}{V_n}\left(\frac{V_{DD}-V_n}{V_{DD}-V_p}\right)\right]$$

where $V_n \cong \frac{1}{3}V_{DD}$, $V_p \cong \frac{2}{3}V_{DD}$,

$R = Ra + Rd$, $C = Cext + C_D$

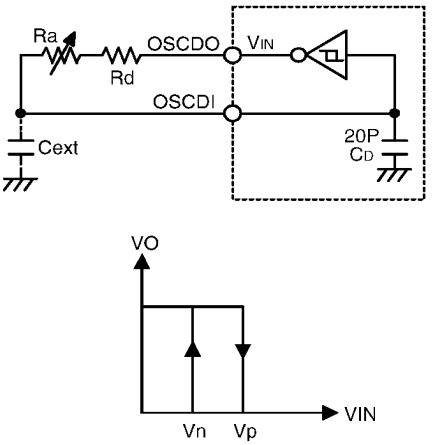

Fig.3 Delay oscillator

The output delay time:

T_D = Toscd × 128000 for the short delay time bonding option.

T_D = Toscd × 128000 × 12 for the long delay time bonding option.

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An external capacitor may be added to OSCDI so as to change the T_D adjustment range. The recommended value of Ra+Rd is 33KΩ ~ 1MΩ, The value of Cext should be ≤ 0.1μF. The oscillator is turned off when the chip is in stand-by state.

LEDB

LEDB is an NMOS open drain structure, acting as a valid trigger indicator. When a valid trigger is detected, it turns on for 1 second; otherwise it remains off.

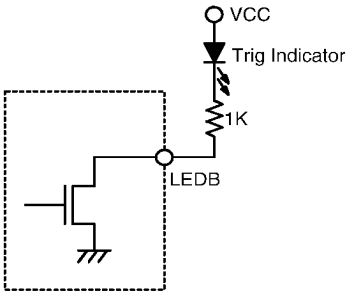

Fig.4 LEDB

TRIAC

TRIAC is a CMOS output structure, outputting a series of pulses when active. The pulse series is synchronized by the ZC (zero crossing) input.

The active duration is controlled by the delay oscillator and the MODE pin.

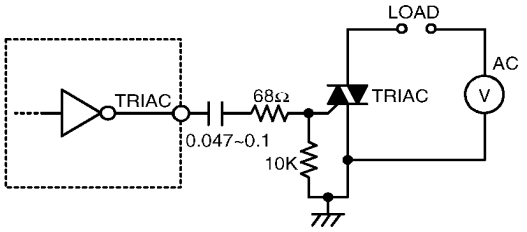

Fig.5 TRIAC application

ZC

ZC is a CMOS input structure. It receives AC line frequency and generates zero crossing pulses to synchronize the TRIAC driver. An external pull-high resistor is required for normal application.

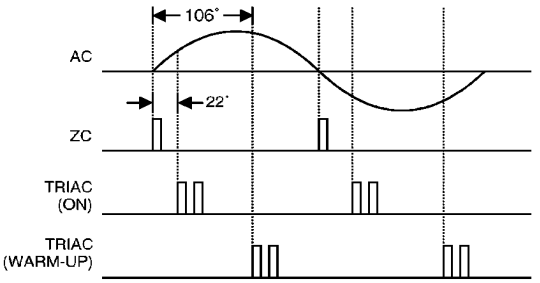

Fig.6 TRIAC waveform

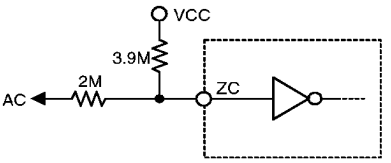

Fig.7 ZC application example

CDS

CDS is a CMOS schmitt trigger input structure. It is used to distinguish between day and night. When the input voltage of CDS is high (above $\frac{2}{3}$ VDD), the outputs TRIAC and RELAY are disabled. When CDS is low (below $\frac{1}{3}$ VDD), the outputs are both enabled. The output disable to enable debounce time is 5 seconds. Connect this pin to VSS when not using this function.

CDS	Status	Output
HIGH	Day Time	Disabled
LOW	Night	Enabled

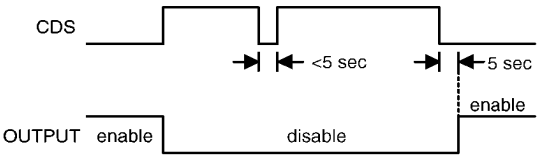

Fig.8 CDS timing

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In Fig.9, R_X can be adjusted to obtain the desired day time detection level. R_Y reduces the CDS sensitivity when the lamp (driven by the TRIAC) is on.

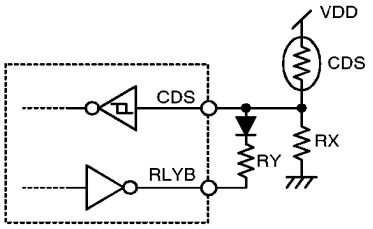

Fig.9 CDS application example

BUZ

BUZ is a CMOS output structure. It outputs 4 beep sounds 6 times continuously to indicate the warm-up time is about over. The pin can drive a piezo buzzer.

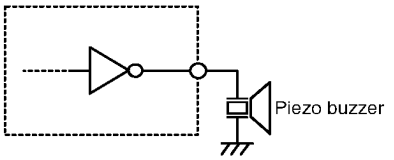

Fig.10 BUZ output drive piezo buzzer

RLYB

RLYB is a CMOS output structure, normally high, active low.

The low duration is controlled by the delay oscillator and the MODE pin. The pin can be used to drive a RELAY (see Fig.12) or a tone generator (see Fig.13)

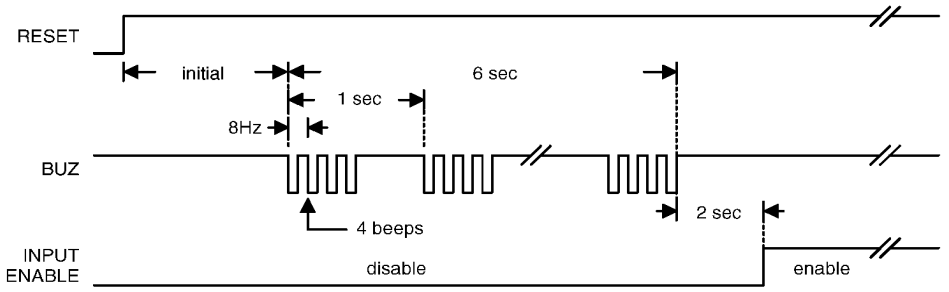

Fig.11 BUZ timing

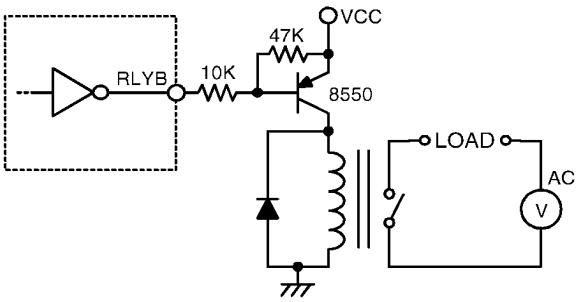

Fig.12 RLYB drive RELAY

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In the above example (Fig.13), RLYB drives KEY2 continuously (for ALARM) but drives key1 momentarily (for DOOR BELL). The BUZ output drives Q2 through C1.

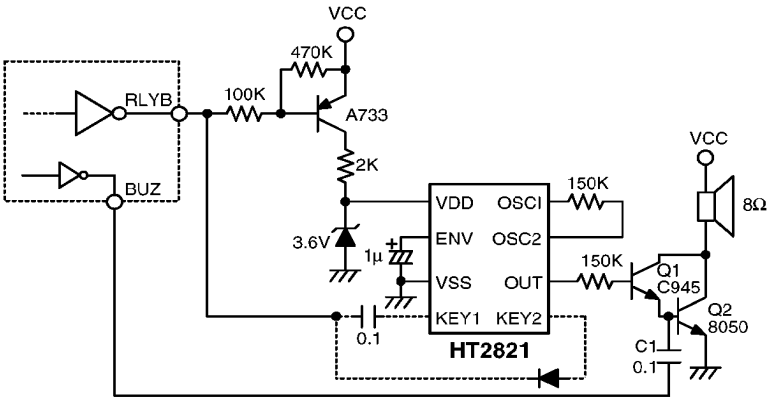

Fig.13 RLYB drive tone generator

MODE

MODE is a CMOS input structure. It toggles the chip to "ON" or "PIR" operating mode. The operating mode changes at the low to high transition of the MODE pin. Connect this pin to VDD when not using this function.

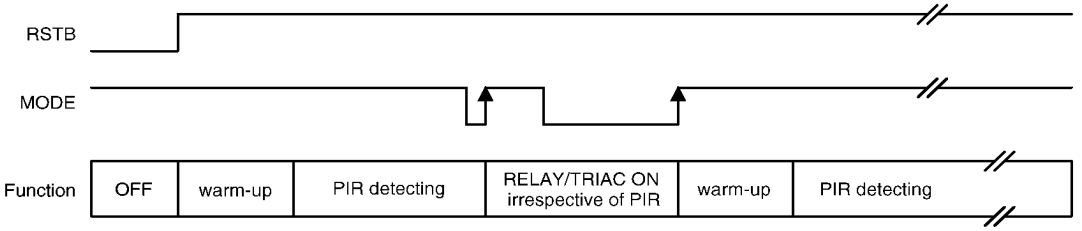

Fig.14 MODE operation

Fig.15 illustrates an example of the MODE application. The ON/OFF SW can change the operating mode.

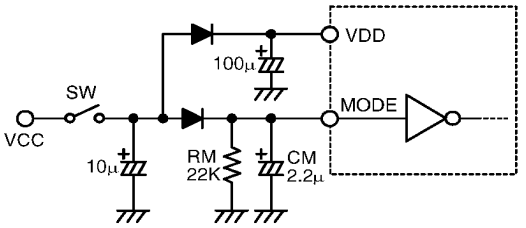

Fig.15 MODE application example

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RSTB

RSTB is used to reset the chip. It's internal pull high and active low.

Fig.16 shows an example of the RSTB application. The use of C_{RST} can extend the power-on initial time. If the RSTB pin is open circuited (without C_{RST}), the initial time equals to the default time (see the next paragraph).

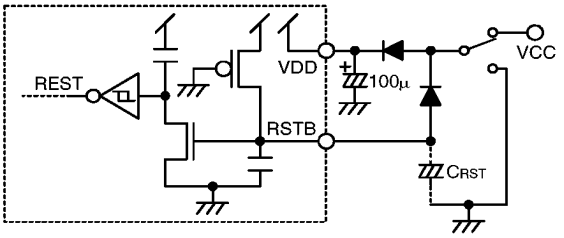

Fig.16 RSTB application example

Power on initial

The PIR signal amplifier requires settling time after power-on. So during this time the input and output should both be disabled.

The HT7606 provides 4 power-on initial time, namely 24 secs, 40 secs, 56 secs, and 72 secs that are decided by mask option. The power-on initial time is also referred to the warm-up time. The default time is 40 secs if it is not specified by the customer.

The chip accepts the MODE pin input control even during the warm-up time.

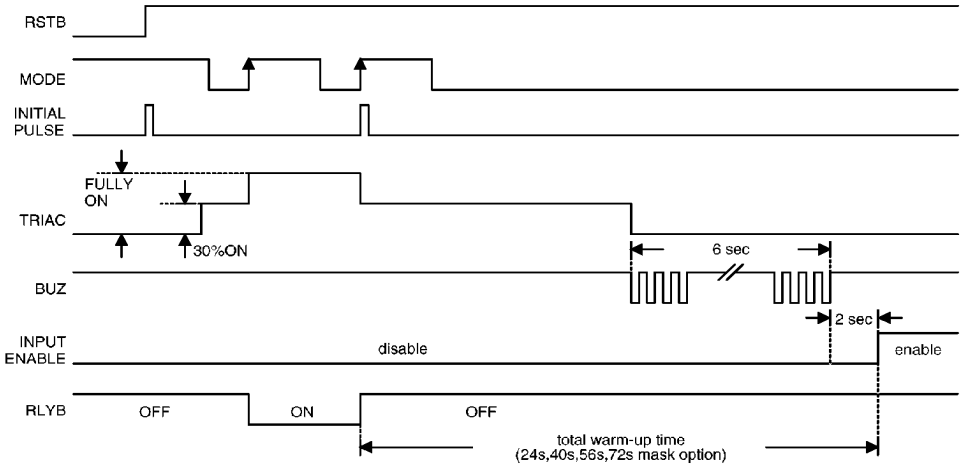

Fig.17 Power-on initial timing

Note: The warm-up time caused by the MODE input cannot be extended by using C_{RST} as in Fig.16.

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Trigger timing

The effective input trigger signal width should be ≥ 24ms. The output is valid either with (1) trigger signal width ≥ 0.5 seconds or (2) more than 2 effective trigger inputs within 2 seconds (separation of 2 triggers ≥ 0.5s).

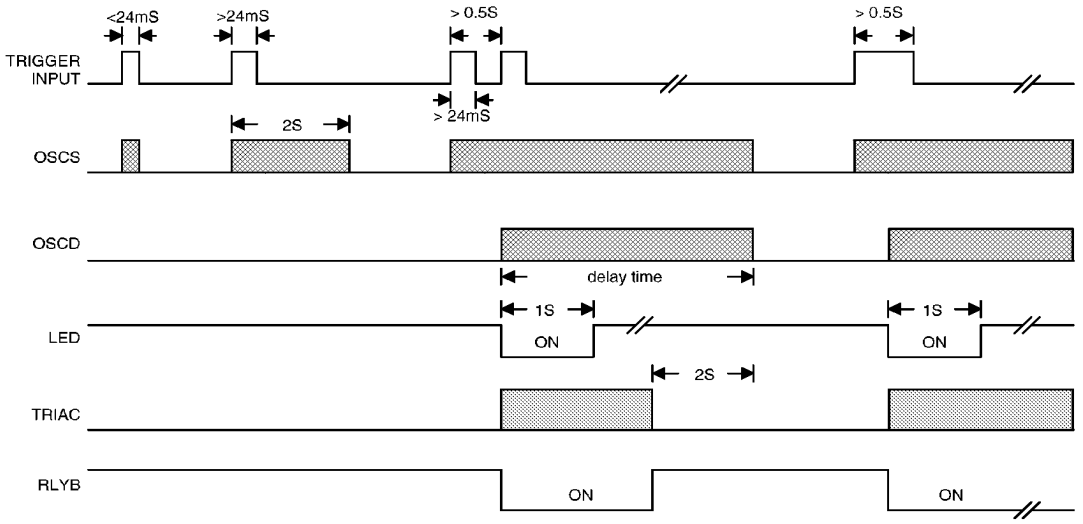

Fig.18 Trigger timing

PIR amplifier

Consult the diagram below for details on the PIR front end amplifier.

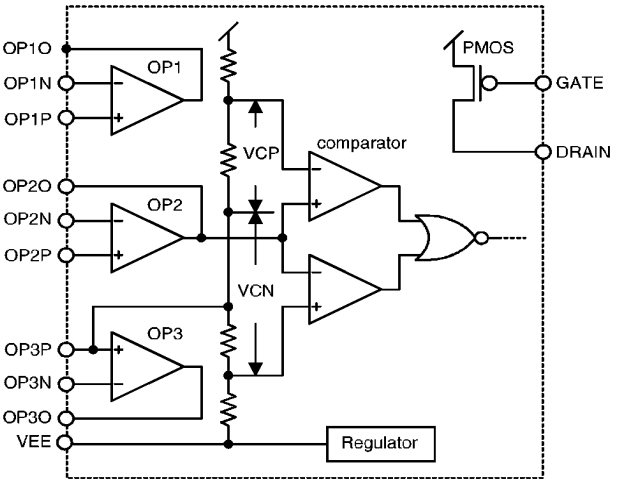

Fig.19 PIR amplifier block diagram

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In Fig.19 there are 3 op-amps all with different applications. OP1 can be used independently as a first stage inverting or a non-inverting amplifier for the PIR.

As the output of OP2 is directly connected to the input of the comparator it is used as a second stage amplifying device.

The non-inverting input of OP3 is connected to the input window centerpoint of the comparator and can be used to check this voltage. OP3 can be used as a buffer to provide a bias voltage that is equal to the centerpoint voltage of the comparator.

The PMOS provides an inverting amplifier which can be used to provide the PIR with a reduced and more stable operating current.

In Fig.19 the comparator can have 3 window levels set by mask options. 1. $\frac{1}{13.33}$ (VDD–VEE), 2. $\frac{1}{9.55}$ (VDD–VEE), 3. $\frac{1}{7.67}$ (VDD–VEE). If the window level fails to be specified the default window will be set to $\frac{1}{13.3}$ (VDD–VEE). The recommended voltage for VDD-VEE is 4V. The default values of V_{CP} and V_{CN} are 0.3V, ($\frac{4}{13.33}$V). For the 24-pin versions, OP3P and OP2P are shorted internally. The voltage level of OP3P is 0.7 (VDD–VEE) typically. It will be –2.8V with respect to VDD when VDD–VEE=4V.

The positive input of OP3 is linked to the center-tap of the comparator window's resistor chain. It can be used to provide OP2 with an accurate bias voltage in addition to monitoring the comparator center voltage.

Each op-amp has a current consumption of approx. 5μA with the op-amps and comparator's working voltage all provided by the regulator. During the battery operation OP3 can also be used as a voltage detector to prevent a low battery voltage from giving faulty operation.

Consult the following diagrams for typical PIR front end circuits.

- First stage of PIR amplifier

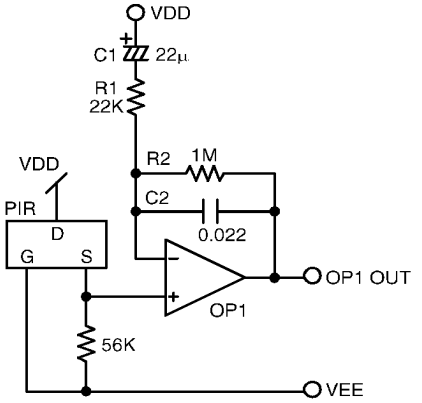

Fig.20 Typical PIR amplifier

Fig.20 demonstrates a typical first stage amplifier. C2 and R2 form a simple low pass filter with a cutoff frequency of 7Hz. The low frequency response is governed by R1 and C1 with a cut-off frequency of 0.33Hz.

$$Av=\frac{(R1+R2)}{R1}$$

Fig.20 and Fig.21 are similar but in Fig.21 the input signal of the amplifier is taken from the drain of the PIR. This has higher gain than that in Fig.20. Since OP1 has PMOS inputs, V_D has to be greater than 1.2V for accurate operation.

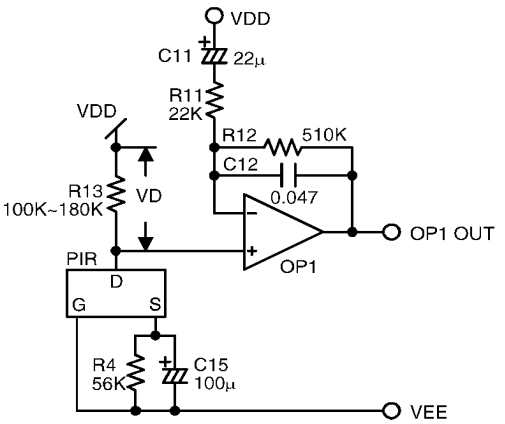

Fig.21 High gain first stage

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- Low current first stage

  Normally the PIR self bias V_{GS} is about 0.8V~1V at room temperature. The PIR $I_{DS} = \frac{0.8V}{56K} = 14.28\mu A$ at 25°C in Fig.20, but this will change with variations in the environmental temperature. For a reduced and more stable I_{DS} a specially provided PMOS can be used. The application circuit is shown in Fig.22.

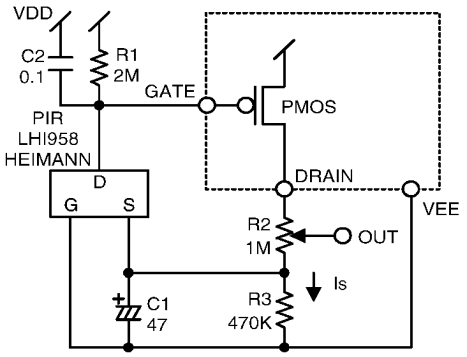

Fig.22 Low current first stage amplifier

The circuit is essentially a PMOS amplifier. In Fig.22 the total current $I_S = \frac{0.8}{R3} = 1.7\mu A$. This value is lower than that in Fig.20. By using the DC feedback the temperature characteristics are better than those in Fig.20 though their voltage gain is similar. The dynamic output range is however reduced.

- Second stage amplifier

  The second stage PIR amplifier is a simple capacitively coupled inverting amplifier with a low pass configuration. The noninverting input terminal is biased to the center point of the comparator window and the output of the second stage amplifier is directly coupled to the comparator center point.

  In Fig.23, OP3P is directly connected to the comparator window center, and with the C3 filter it can act as the bias for OP2. $A_V = \frac{R2}{R1}$, low cutoff frequency $f_L = \frac{1}{2\pi R1C1}$, high cutoff frequency $f_H = \frac{1}{2\pi R2C2}$. By changing the value of R2 the sensitivity can be varied. C1 and C3 should be low leakage types so as to prevent the DC operating point from change due to current leakage.

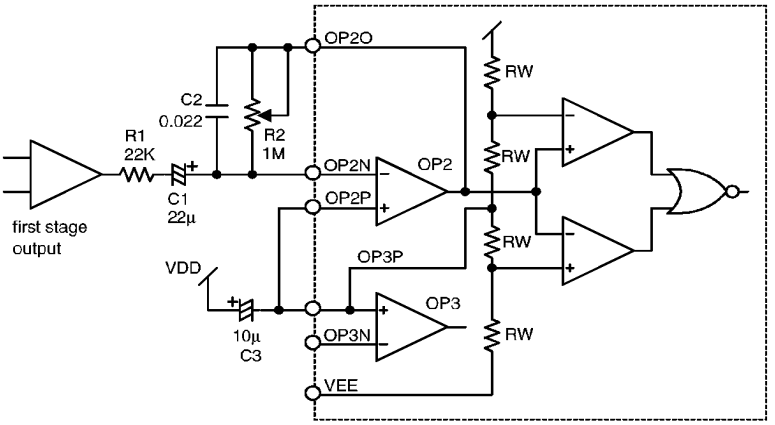

Fig.23 Typical second stage amplifier

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Second stage amplifier with DC feedback

A configuration of DC feedback circuit is recommended to eliminate the leakage effect of coupling capacitor. Refer to Fig.24.

$$A_V = \frac{R_2}{R_1}, \quad f_H = \frac{1}{2\pi R_2 C_1}, \quad f_L = \frac{1}{\pi R_3 C_I}$$

In Fig.24 the OP1 output is directly coupled to OP2. The DC operating point of OP2 is controlled by OP3 with OP3 being referenced to the window center. Therefore, The output operating point of OP2 is always equal to the window center voltage. For the integrating capacitor C_I it is suggested to use nonpolarized types of capacitor, or connect two polarized types oppositely.

Another advantage of DC feedback is that it can shorten the power-on settling time. The voltage variation on C_I is smaller than that of C1 in Fig.23 at power-on.

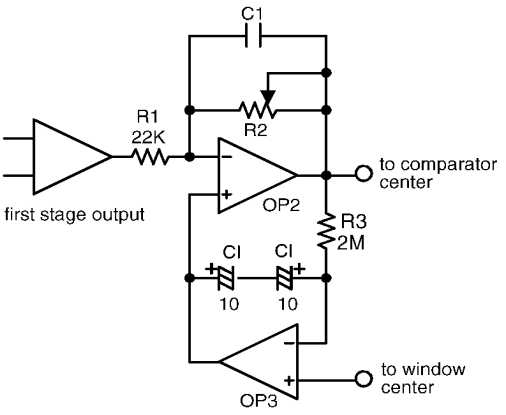

Fig.24 Second stage amplifier with DC feedback

Power supply

- Battery powered operating

  When using the 9V battery power supply, consult the following diagram:

In the circuit, the 9V battery is directly connected to a speaker and the LED. The supply is connected to the VDD of the HT7606's via D1, and is isolating the front end from the effect of the speaker and LED. The front end circuits are all supplied by VEE. The 3.6V supply to the tone generator chip is provided by the HT7606 RLYB output and Q3, D3, R5, R6, and R7.

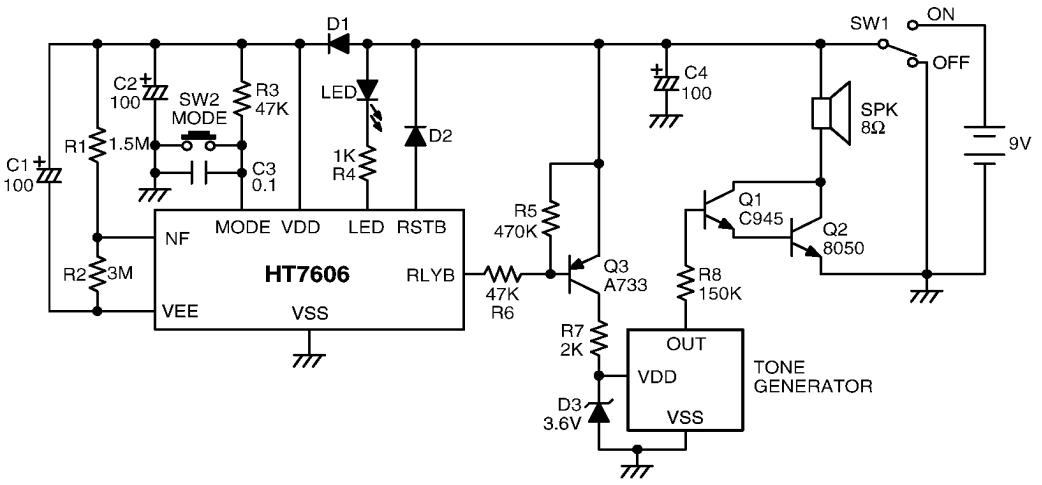

Fig.25 Battery power supply circuit

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- AC line power supply for TRIAC

The advantages of low power consumption design make the HT7606 suitable for applications on 2 wire direct line powered automatic lamp controllers.

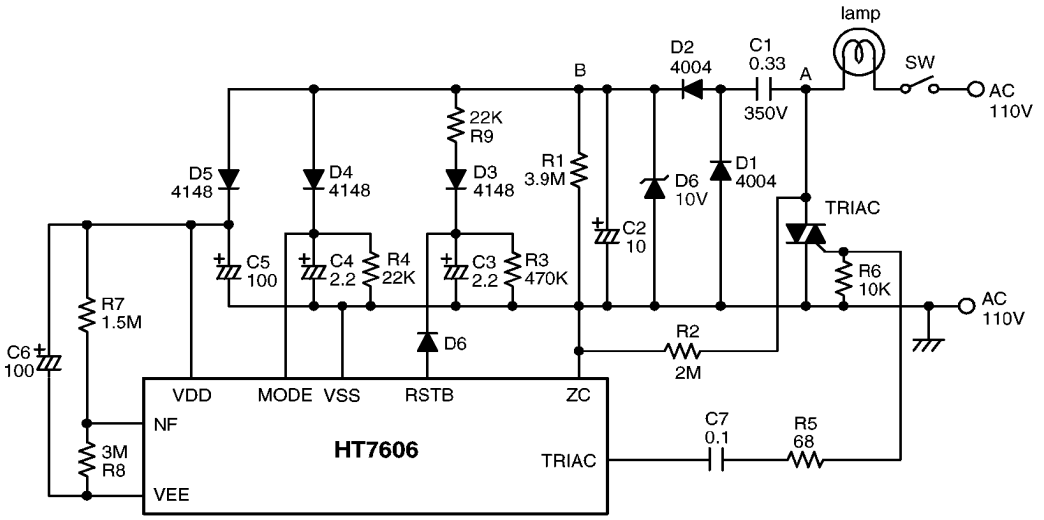

Fig.26 AC line power supply for TRIAC applications

The AC line voltage zero crossing point is 1 ms (60Hz) before the TRIAC fire point.

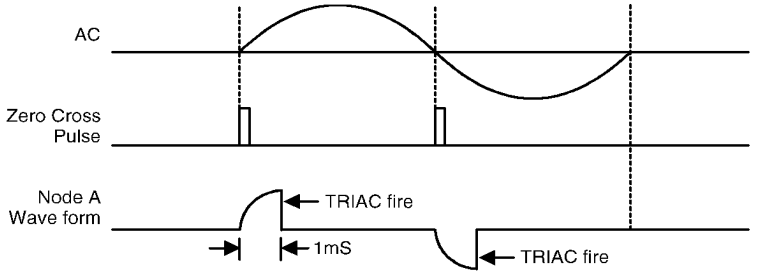

Fig.27 Power supply waveform (TRIAC active)

Node A's waveform is rectified by D1, D2 and smoothed by C2 to supply power for the system. R4 and C4 provide the time constant for MODE control debounce. R3 and C3 set the max. power-off time for automatic system reset. D5 isolates VDD from the effects of voltage variation on node B.

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• AC line power supply for RELAY applications

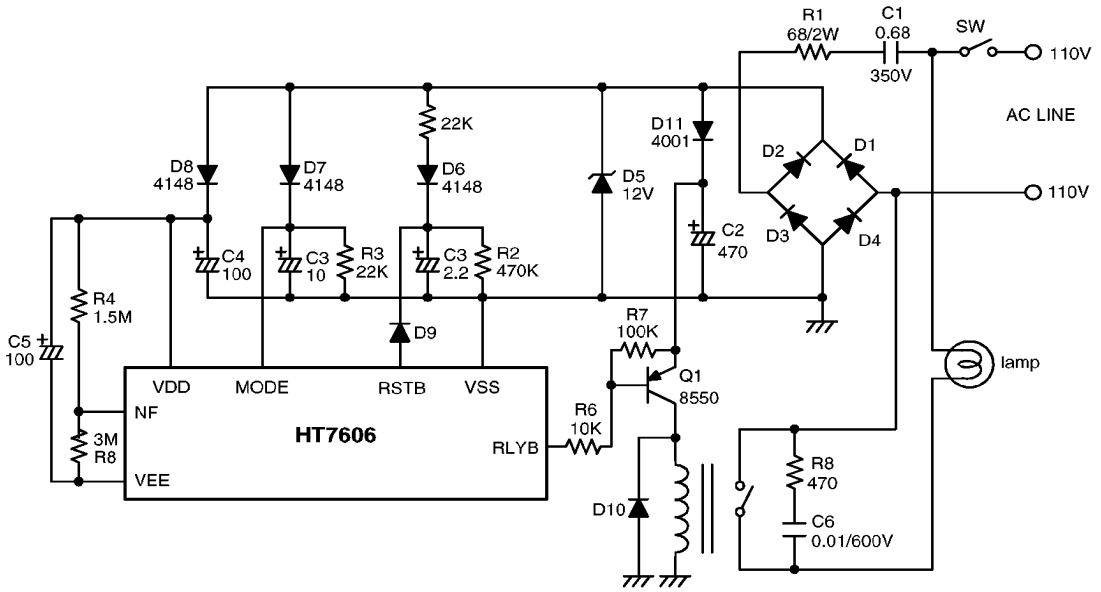

Fig.28 AC line power supply circuit for RELAY applications

In Fig.28 the D1~D4 bridge rectifier can supply enough power to drive the relay. The values of R1 and C1 depend on the relay current consumption. R8 and C6 reduce spikes with the relay turns on or off.

TESTB

TESTB is a CMOS input with internal pull-high. Connecting this pin to VSS can speed up the internal counter by 64 times to save time for final product testing.

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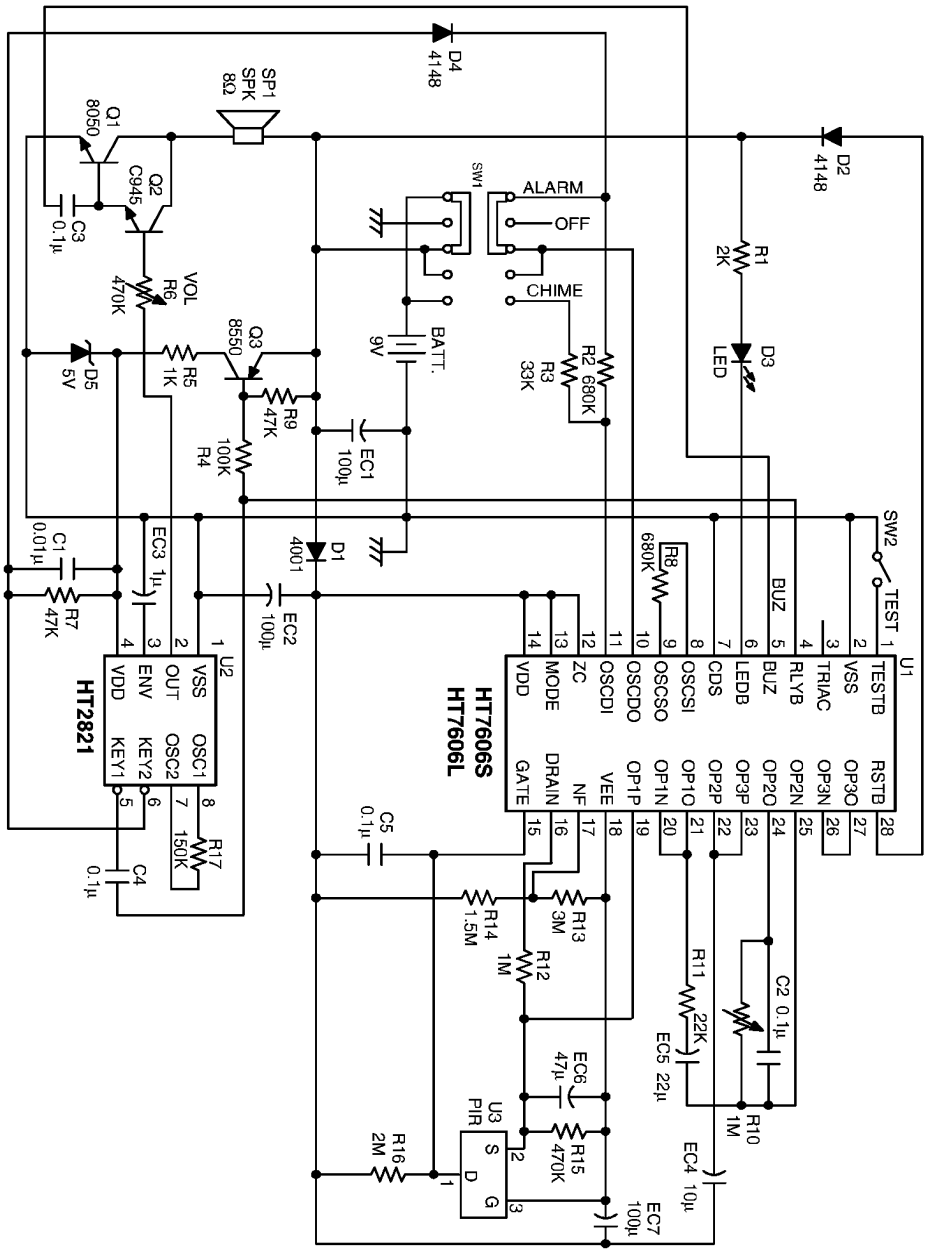
Application Circuit

DC power supply application (28 DIP/SOP)



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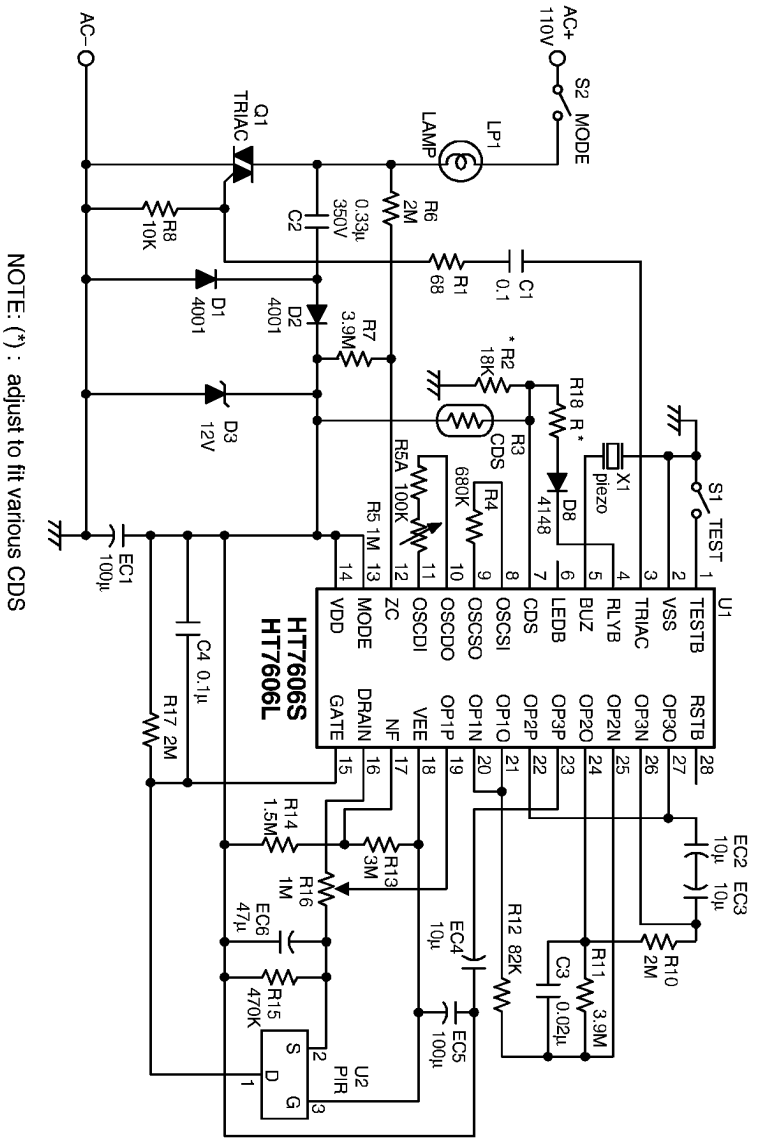
2-wire TRIAC application (28 DIP/SOP)



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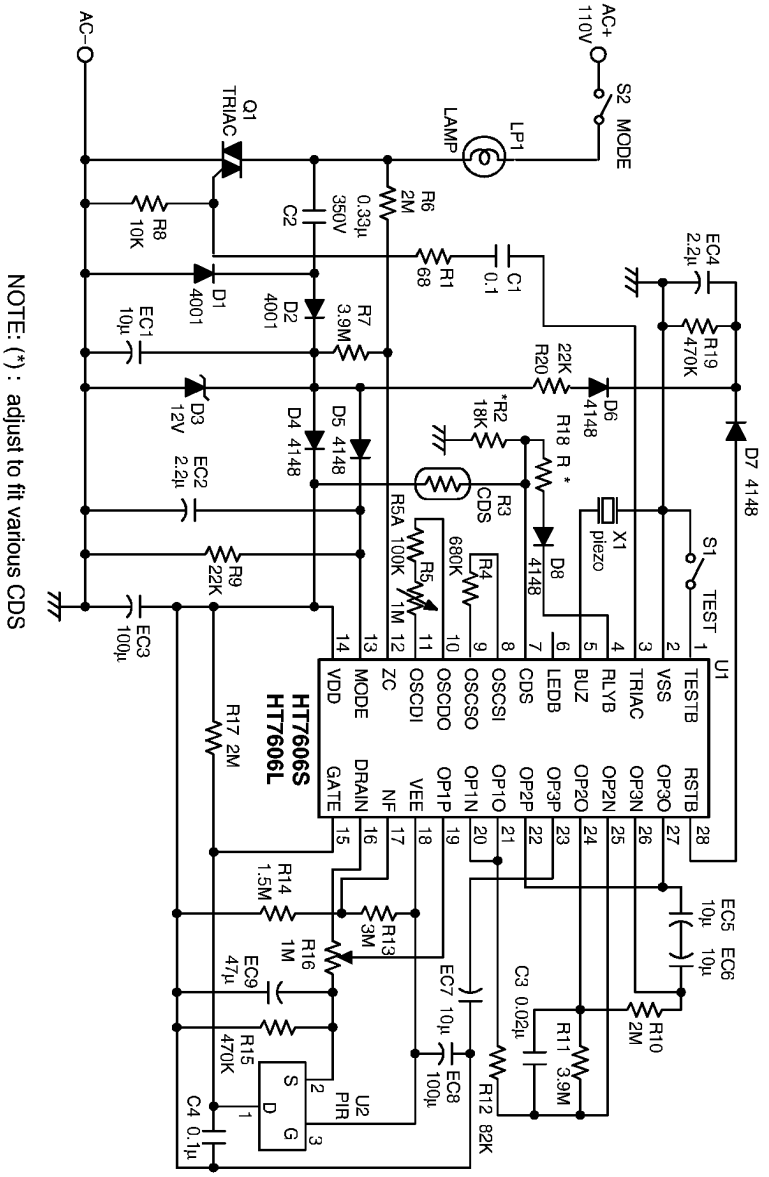
2-wire TRIAC application with MODE & reset control (28 DIP/SOP)



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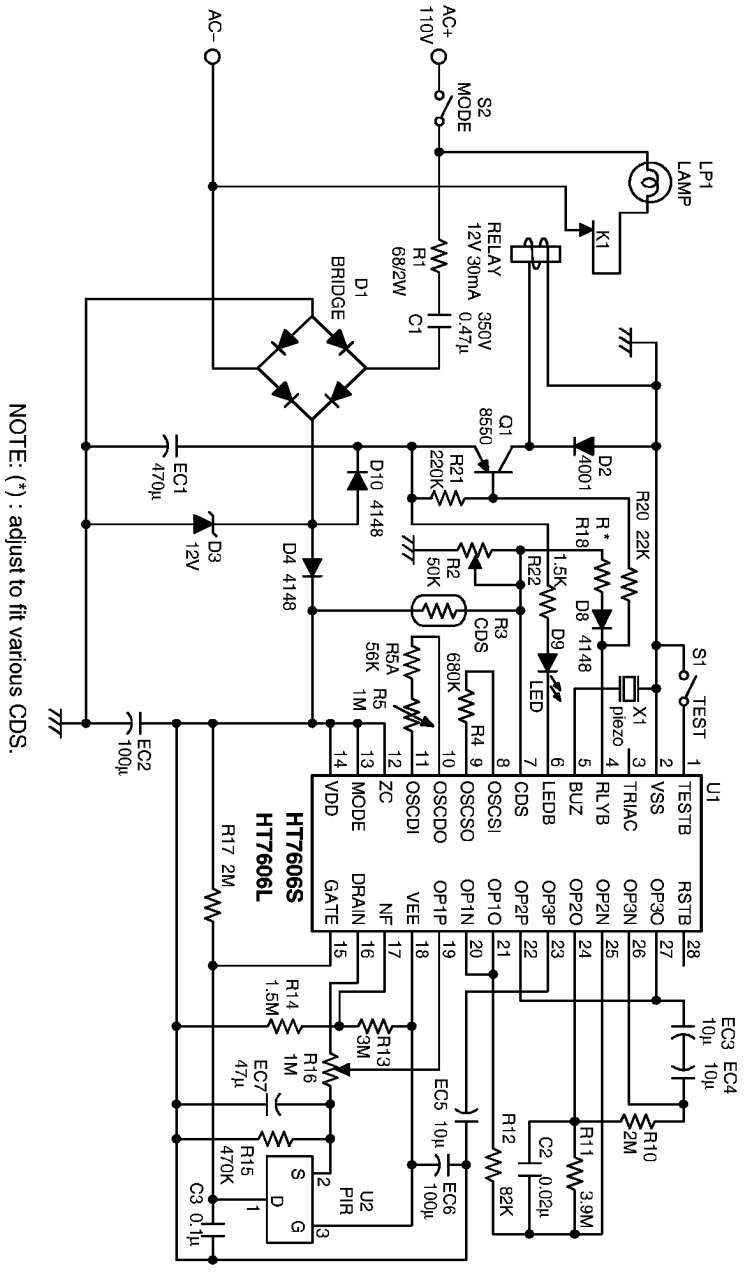
RELAY application (28 DIP/SOP)



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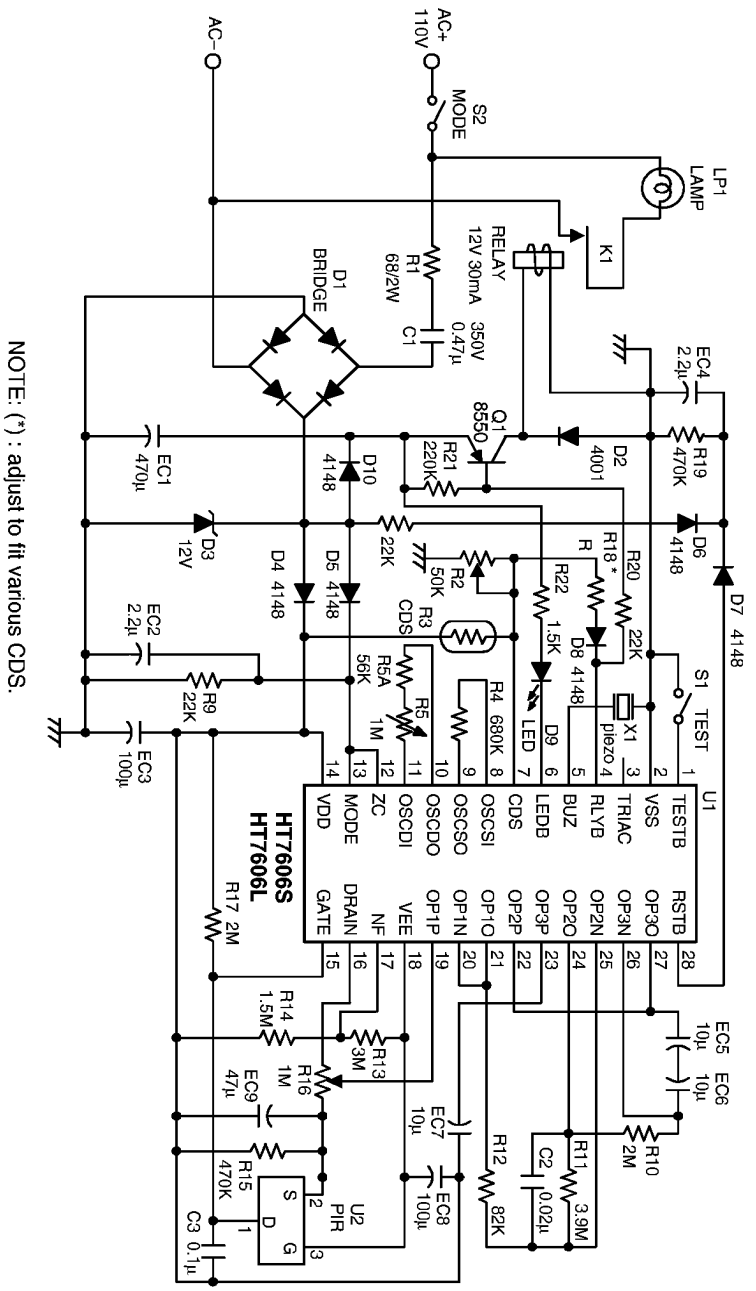
RELAY application with MODE & reset control (28 DIP/SOP)



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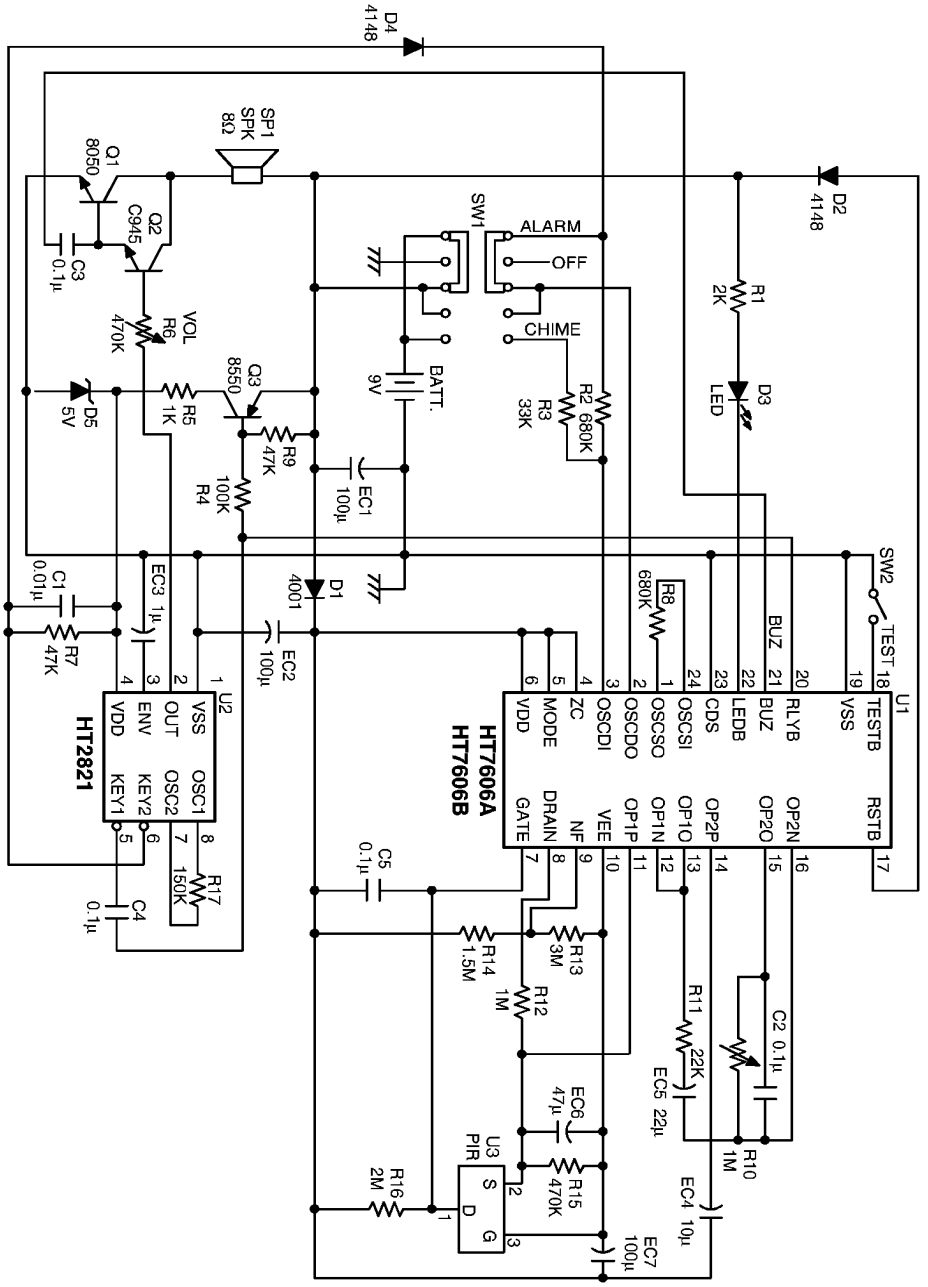
DC power supply application (24 DIP/SOP)



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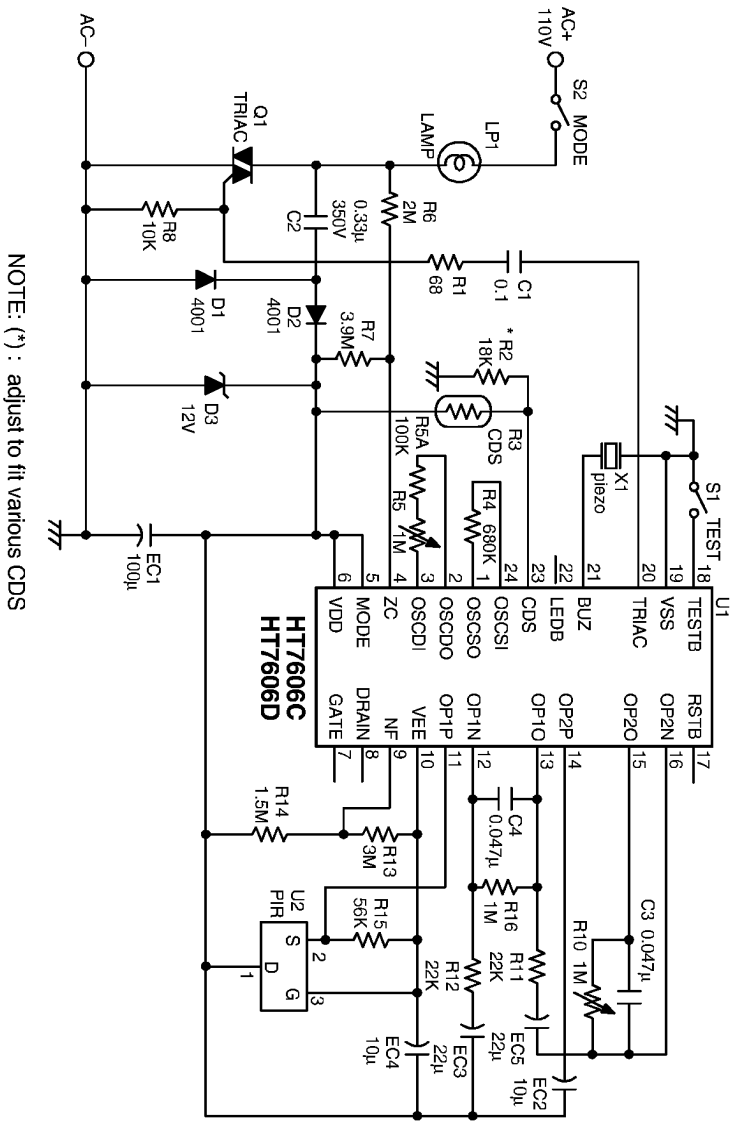
2-Line TRIAC application (24 DIP/SOP)



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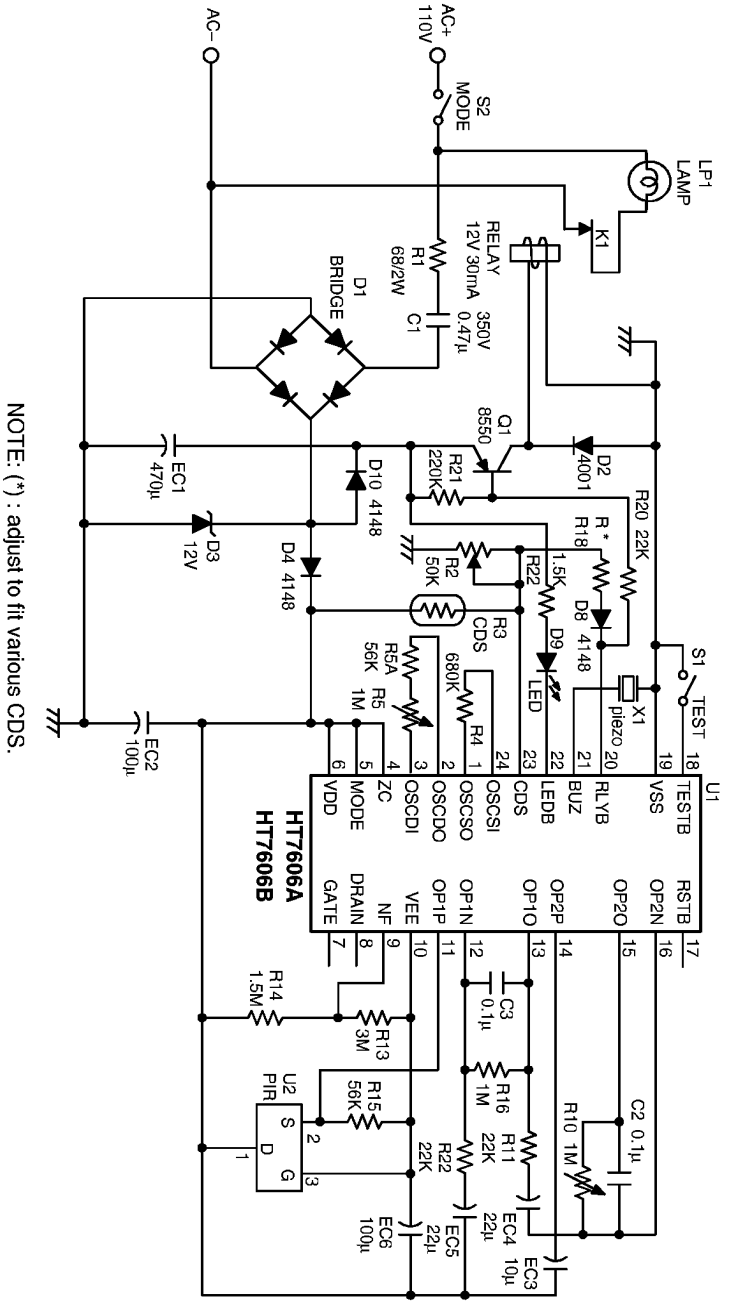
RELAY application (24 DIP/SOP)



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