405GPr

Data Sheet

Power PC 405GPr Embedded Processor

Features

- PowerPC® 405 32-bit RISC processor core operating up to 400MHz with 16KB I- and D-caches
- Synchronous DRAM (SDRAM) interface operating up to 133MHz
  - 32-bit interface for non-ECC applications
  - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- 4KB on-chip memory (OCM)
- External peripheral bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8-, 16-, or 32-bit SRAM and external peripherals
  - Up to eight devices
  - External Mastering supported
- DMA support for external peripherals, internal UART and memory
  - Scatter-gather chaining supported
  - Four channels
- PCI Revision 2.2 compliant interface (32-bit, up to 66MHz)
  - Synchronous or asynchronous PCI Bus interface
  - Internal or external PCI Bus Arbiter
- Ethernet 10/100Mbps (full-duplex) support with media independent interface (MII)
- Programmable interrupt controller supports 13 external and 19 internal edge triggered or level-sensitive interrupts
- Programmable timers
- Two serial ports (16550 compatible UART)
- One IIC interface
- General purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal processor local Bus (PLB) runs at SDRAM interface frequency
- Supports PowerPC processor boot from PCI memory
- Unique software-accessible 64-bit chip ID number (ECID).

Description

Designed specifically to address embedded applications, the PowerPC 405GPr (PPC405GPr) provides a high-performance, low-power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation requirements.

This chip contains a high-performance RISC processor core, SDRAM controller, PCI bus interface, Ethernet interface, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: CMOS SA-27E, 0.18 µm (0.11 µm L_{eff})

Package: 456-ball (35mm or 27mm) enhanced plastic ball grid array (E-PBGA) in both leaded and lead-free versions

Power (typical): 0.72W at 266MHz

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Figures

Ordering, PVR, and JTAG Information

Product Name	Order Part Number[1]	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC405GPr	PPC405GPr-3BB266	266MHz	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3JB266	266MHz	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3BB266Z	266MHz	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3JB266Z	266MHz	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3DB266	266MHz	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3KB266	266MHz	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3DB266Z	266MHz	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3KB266Z	266MHz	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3BB333	333MHz[2]	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3JB333	333MHz[2]	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3BB333Z	333MHz[2]	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3JB333Z	333MHz[2]	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3DB333	333MHz[2]	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3KB333	333MHz[2]	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3DB333Z	333MHz[2]	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3KB333Z	333MHz[2]	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3BB400	400MHz	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3JB400	400MHz	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3BB400Z	400MHz	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3JB400Z	400MHz	35mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3DB400	400MHz	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3KB400	400MHz	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3DB400Z	400MHz	27mm, 456 E-PBGA	B	0x50910951	0x24088049
PPC405GPr	PPC405GPr-3KB400Z	400MHz	27mm, 456 E-PBGA	B	0x50910951	0x24088049

Notes

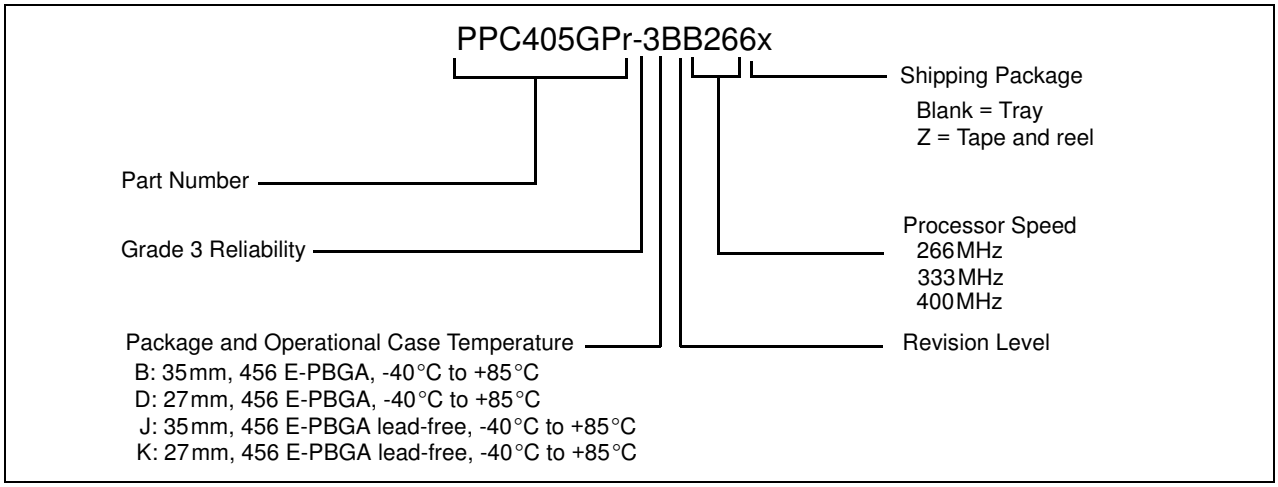
1: Z at the end of the Order Part Number indicates a tape-and-reel shipping package. Otherwise, the chips are shipped in a tray.

2. If the 333MHz parts are operated at 266MHz or less, the operational temperature range is extended to 105°C

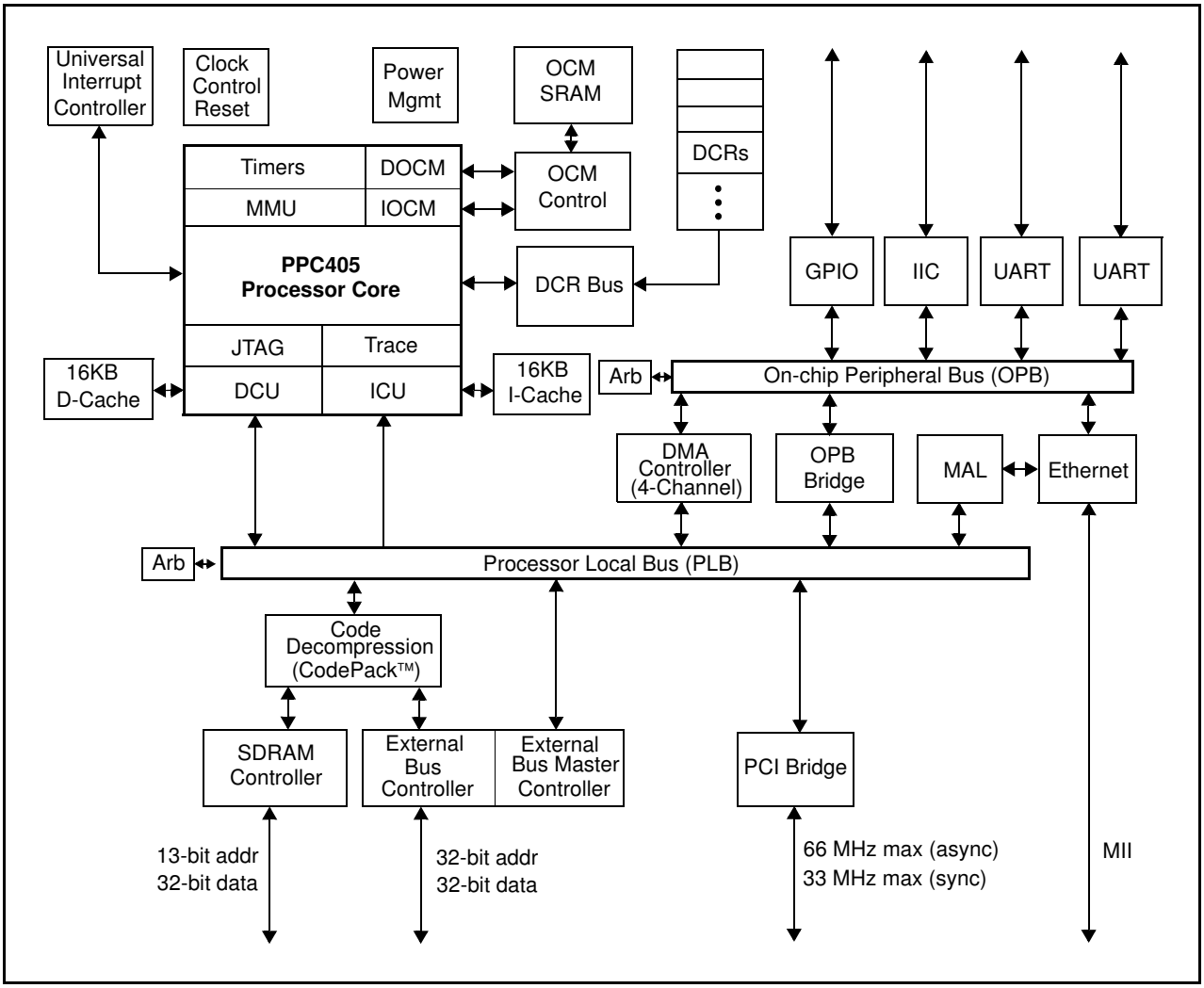
The part number contains a revision code. This refers to the die mask revision number and is included in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the *PowerPC 405GPr Embedded Processor User's Manual* for details on the register content.

Order Part Number Key



PPC405GPr Embedded Controller Functional Block Diagram



The PPC405GPr is designed using the IBM® Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific ASIC product. This approach provides a consistent way to create complex ASICs using IBM CoreConnect™ Bus Architecture.

Address Map Support

The PPC405GPr incorporates two simple and separate address maps. The first address map defines the possible use of address regions that the processor can access. The second address map is for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the PPC405GPr processor through the use of **mtdcr** and **mfdcr** instructions.

System Memory Address Map 4GB System Memory

Function	Subfunction	Start Address	End Address	Size
General Use	SDRAM, External Peripherals, and PCI Memory **Note:** Any of the address ranges listed at right may be use for any of the above functions.	0x00000000	0xE7FFFFFF	3712MB
		0xE8010000	0xE87FFFFF	8MB
		0xEC000000	0xEEBFFFFF	44MB
		0xEEE00000	0xEF3FFFFF	6MB
		0xEF500000	0xEF5FFFFF	1MB
		0xF0000000	0xFFFFFFFF	256MB
Boot-up	Peripheral Bus Boot [1]	0xFFE00000	0xFFFFFFFF	2MB
	PCI Boot [2]	0xFFFE0000	0xFFFFFFFF	128KB
PCI	PCI I/O	0xE8000000	0xE800FFFF	64KB
	PCI I/O	0xE8800000	0xEBFFFFFF	56MB
	Configuration Registers	0xEEC00000	0xEEC00007	8B
	Interrupt Acknowledge and Special Cycle	0xEED00000	0xEED00003	4B
	Local Configuration Registers	0xEF400000	0xEF40003F	64B
Internal Peripherals	UART0	0xEF600300	0xEF600307	8B
	UART1	0xEF600400	0xEF600407	8B
	IIC0	0xEF600500	0xEF60051F	32B
	OPB Arbiter	0xEF600600	0xEF60063F	64B
	GPIO Controller Registers	0xEF600700	0xEF60077F	128B
	Ethernet Controller Registers	0xEF600800	0xEF6008FF	256B

Notes:
1. When peripheral bus boot is selected, peripheral bank 0 is automatically configured at reset to the address range listed above.
2. If PCI boot is selected, a PLB-to-PCI mapping is automatically configured at reset to the address range listed above.
3. After the boot process, software may reassign the boot memory regions for other uses.
4. All address ranges not listed above are reserved.

DCR Address Map 4KB Device Configuration Registers

Function	Start Address	End Address	Size
Total DCR Address Space[1]	0x000	0x3FF	1KW (4KB)[1]
By function:			
Reserved	0x000	0x00F	16W
Memory Controller Registers	0x010	0x011	2W
External Bus Controller Registers	0x012	0x013	2W
Decompression Controller Registers	0x014	0x015	2W
Reserved	0x016	0x017	2W
On-Chip Memory Controller Registers	0x018	0x01F	8W
Reserved	0x020	0x07F	96W
PLB Registers	0x080	0x08F	16W
Reserved	0x090	0x09F	16W
OPB Bridge Out Registers	0x0A0	0x0A7	8W
Electronic Chip ID (ECID)	0x0A8	0x0A9	2W
Reserved	0x0AA	0x0AF	6W
Clock, Control, Interrupt Routing, and Reset	0x0B0	0x0B7	8W
Power Management	0x0B8	0x0BF	8W
Interrupt Controller	0x0C0	0x0CF	16W
Reserved	0x0D0	0x0FF	48W
DMA Controller Registers	0x100	0x13F	64W
Reserved	0x140	0x17F	64W
Ethernet MAL Registers	0x180	0x1FF	128W
Reserved	0x200	0x3FF	512W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

On-Chip Memory (OCM)

The OCM feature comprises a memory controller and a one-port 4KB static RAM (SRAM) accessed by the processor core.

Features include:

- Low-latency access to critical instructions and data
- Performance identical to cache hits without misses
- Contents change only under program control

PLB to PCI Interface

The PLB to PCI interface core provides a mechanism for connecting PCI devices to the local PowerPC processor and local memory. This interface is compliant with version 2.2 of the PCI Specification.

Features include:

- Internal PCI bus arbiter for up to six external devices at PCI bus speeds up to 66MHz. Internal arbiter use is optional and can be disabled for systems which employ an external arbiter.
- PCI bus frequency up to 66MHz
  - Synchronous operation at 1/n fractions of PLB speed (n = 1 to 4) to 33MHz maximum
  - Asynchronous operation from 1/8 PLB frequency to 66MHz maximum
- 32-bit PCI address/data bus
- Power Management:
  - PCI Bus Power Management v1.1 compliant
- Supports 1:1, 2:1, 3:1, 4:1 clock ratios from PLB to PCI
- Buffering between PLB and PCI:
  - PCI target 64-byte write post buffer
  - PCI target 96-byte read prefetch buffer
  - PLB slave 32-byte write post buffer
  - PLB slave 64-byte read prefetch buffer
- Error tracking/status
- Supports PCI target side configuration
- Supports processor access to all PCI address spaces:
  - Single-byte PCI I/O reads and writes
  - PCI memory single-beat and prefetch-burst reads and single-beat writes
  - Single-byte PCI configuration reads and writes (type 0 and type 1)
  - PCI interrupt acknowledge
  - PCI special cycle

- Supports PCI target access to all PLB address spaces
- Supports PowerPC processor boot from PCI memory

SDRAM Memory Controller

The PPC405GPr Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported. The memory controller supports up to four physical banks. Up to 256MB per bank are supported, up to a maximum of 1GB. Memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 addressing for SDRAM (2- and 4-bank)
- 32-bit memory interface support
- Programmable address compare for each bank of memory
- Industry standard 168-pin DIMMS are supported (some configurations)
- PC-133 support for 133 MHz memory
- 4MB to 256MB per bank
- Programmable address mapping and timing
- Auto refresh
- Page mode accesses with up to 4 open pages
- Power management (self-refresh)
- Error checking and correction (ECC) support
  - Standard single-error correct, double-error detect coverage
  - Aligned nibble error detect
  - Address error logging

External Peripheral Bus Controller (EBC)

- Supports eight banks of ROM, EPROM, SRAM, Flash memory, or slave peripherals
- Up to 66MHz operation
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus width support
- Latch data on Ready
- Programmable 2K clock time-out counter with disable for Ready
- Programmable access timing per device
  - 0–255 wait states for non-bursting devices
  - 0–31 burst wait states for first access and up to 7 wait states for subsequent accesses

  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (0 to 3 clock cycles) relative to CS
- Programmable address mapping
- Peripheral Device pacing with external “Ready”
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

DMA Controller

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

Serial Interface

- One 8-pin UART and one 4-pin UART interface provided
- Selectable internal or external serial clock to allow a wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with 16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

- Compliant with Philips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Fifteen memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses
- 23 of 24 GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. The 23 GPIOs are multiplexed with:
  - 7 of 8 chip selects
  - All 13 external interrupts
  - All nine instruction trace pins
- Each GPIO output is separately programmable to emulate an open-drain driver (i.e., drives to zero, three-stated if output bit is 1)

Universal Interrupt Controller (UIC)

The Universal Interrupt Controller (UIC) provides the control, status, and communications necessary between the various sources of interrupts and the local PowerPC processor.

Features include:

- Supports 13 external and 19 internal interrupts
  - Seven of the 13 interrupts are mapped to the same GPIOs as the PPC405GP.
  - The other six interrupts can be mapped to any of the GPIOs.
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

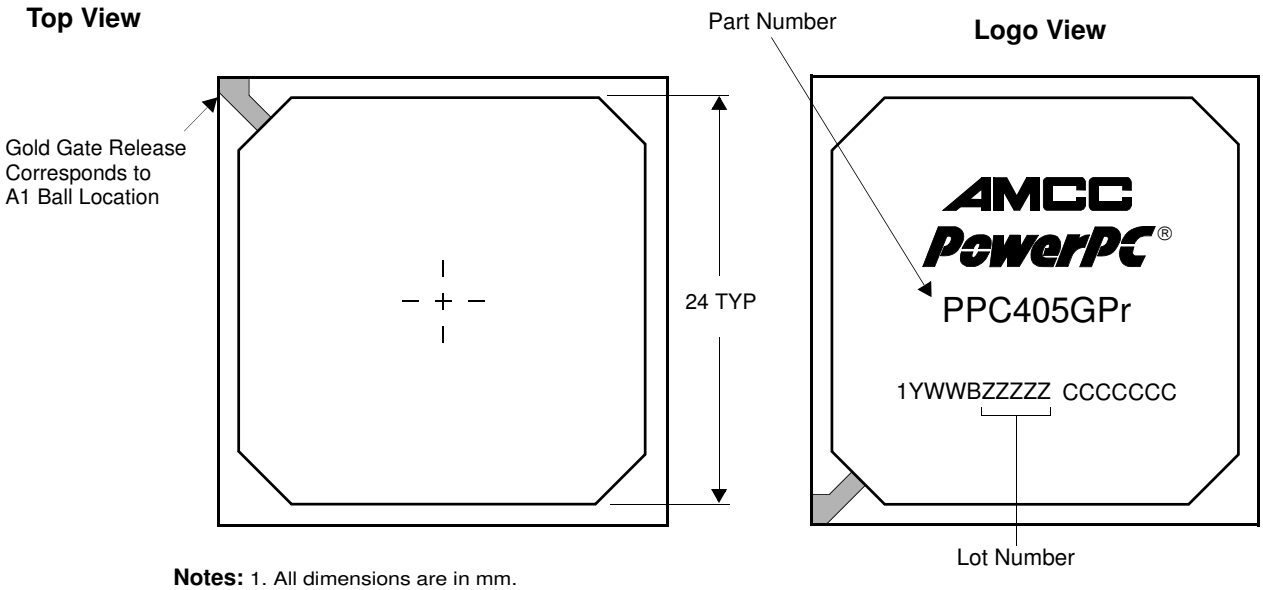
10/100 Mbps Ethernet MAC

- Capable of handling full/half duplex 100Mbps and 10Mbps operation
- Uses the medium independent interface (MII) to the physical layer (PHY not included on chip)

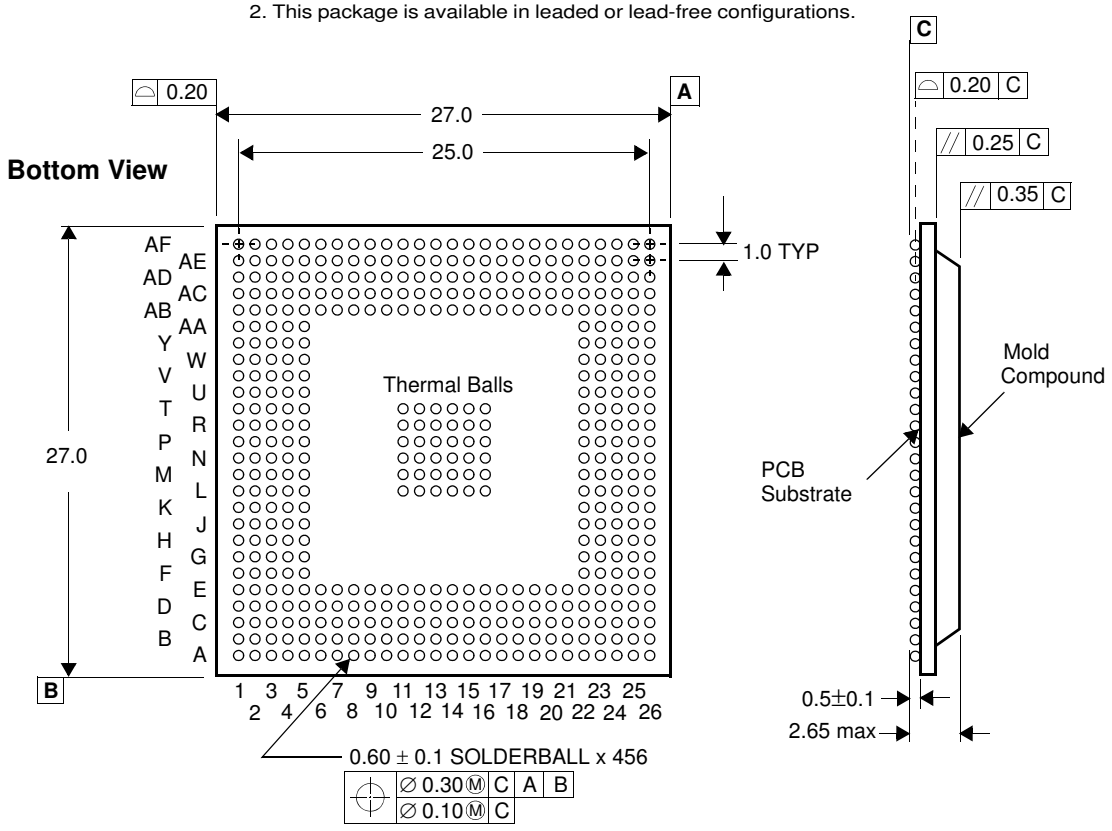
JTAG

- IEEE 1149.1 test access port
- IBM RISCWatch debugger support
- JTAG Boundary Scan Description Language (BSDL)

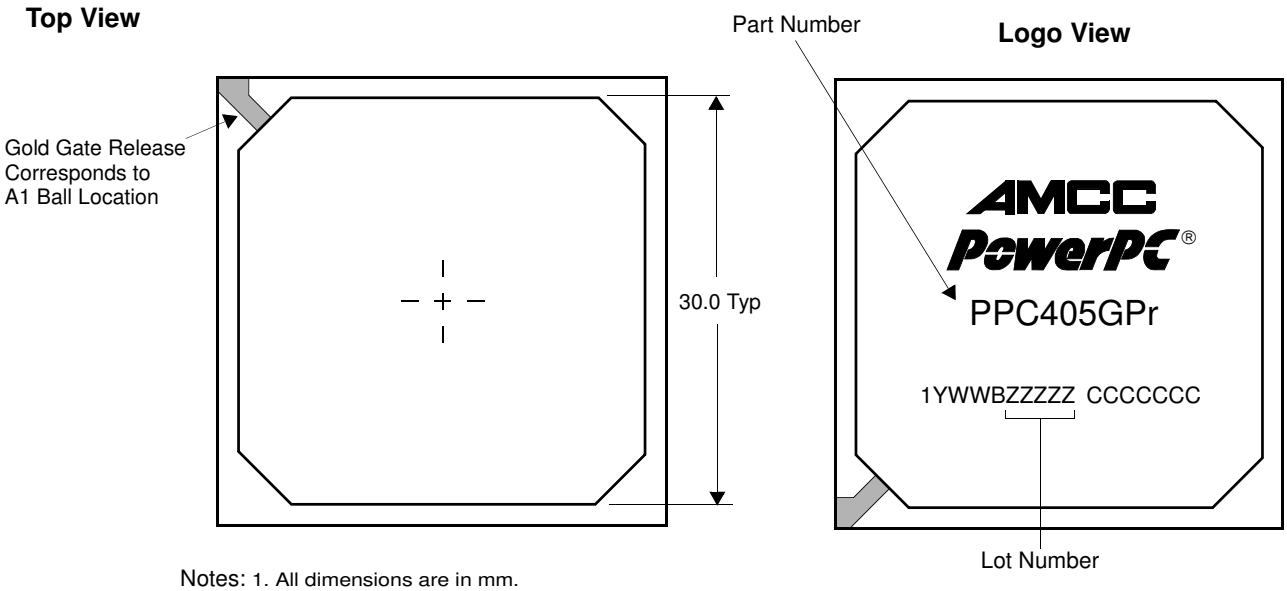
27mm, 456-Ball E-PBGA Package



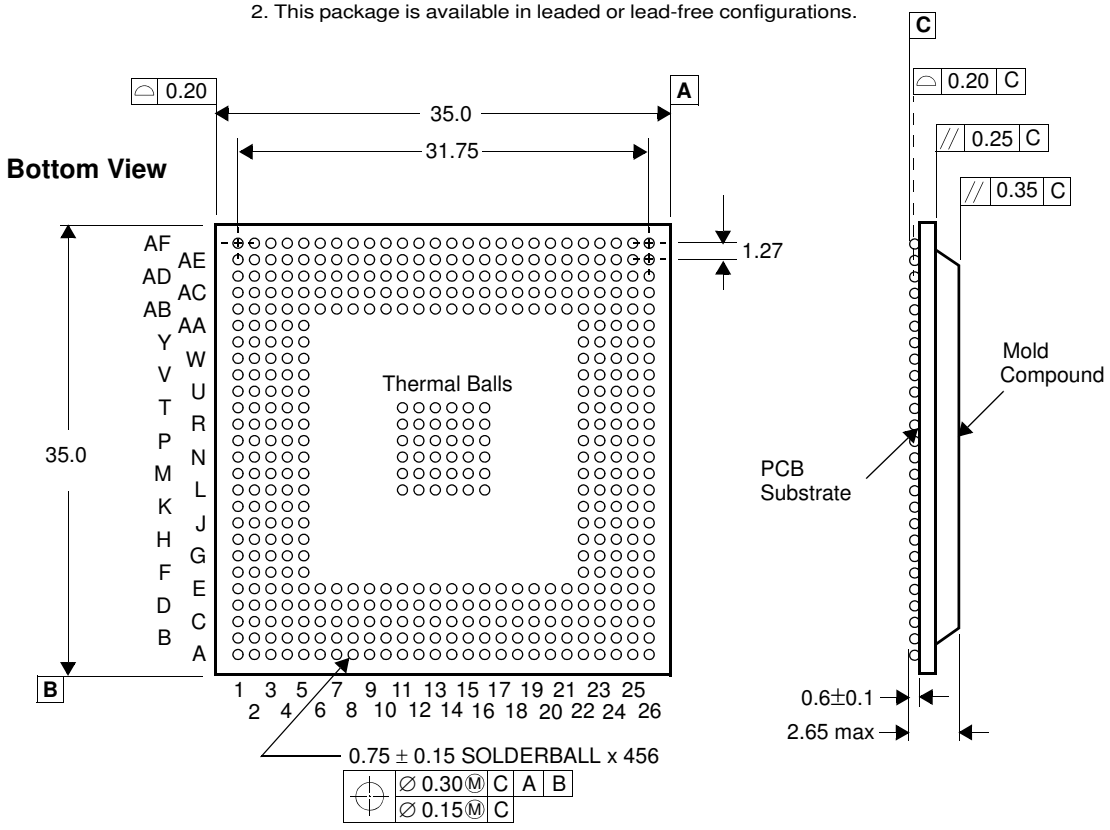
Notes: 1. All dimensions are in mm.
2. This package is available in leaded or lead-free configurations.



35mm, 456-Ball E-PBGA Package



Notes: 1. All dimensions are in mm.
2. This package is available in leaded or lead-free configurations.



Pin Lists

The PPC405GPr embedded controller is available as a 456-ball E-PBGA leaded or lead-free package. The 456-ball package is available in two sizes—35 millimeters and 27 millimeters. In this section there are two tables that correlate the external signals to the physical package pin (ball) on which they appear.

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in "Signal Functional Description" on page 30 where the signals in the indicated interface group begin.

Signals Listed Alphabetically (Sheet 1 of 9)

Signal Name	Ball	Interface Group	Page
AGND	E22	System	35
AV_{DD}	D25	System	35
BA0 BA1	AB24 AC24	SDRAM	32
$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$	AD17 AF17 AE15 AC14	SDRAM	32
$\overline{\text{BE0}}$[PCIC0] $\overline{\text{BE1}}$[PCIC1] $\overline{\text{BE2}}$[PCIC2] $\overline{\text{BE3}}$[PCIC3]	D19 F24 K24 R26	PCI	30
BusReq	R3	External Master Peripheral	34
$\overline{\text{CAS}}$	AB23	SDRAM	32
ClkEn0 ClkEn1	AB25 AC25	SDRAM	32
DMAAck0 DMAAck1 DMAAck2 DMAAck3	D16 B15 B14 C12	External Slave Peripheral	32
DMAReq0 DMAReq1 DMAReq2 DMAReq3	C16 D14 C11 A7	External Slave Peripheral	32
DQM0 DQM1 DQM2 DQM3	AC12 AC10 AC6 AA3	SDRAM	32
DQMCB	AC15	SDRAM	32
ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7	AE14 AF15 AF14 AD13 AF13 AF12 AE13 AD12	SDRAM	32
EMCMDClk	H24	Ethernet	31
EMCMDIO[PHYMDIO]	AD26	Ethernet	31
EMCTxD0 EMCTxD1 EMCTxD2 EMCTxD3	J26 L25 L24 P25	Ethernet	31
EMCTxEn	K23	Ethernet	31

Signals Listed Alphabetically (Sheet 2 of 9)

Signal Name	Ball	Interface Group	Page
EMCTxErr	K25	Ethernet	31
EOT0/TC0 EOT1/TC1 EOT2/TC2 EOT3/TC3	F3 G2 V2 Y1	External Slave Peripheral	32
$\overline{\text{ExtAck}}$	Y3	External Master Peripheral	34
$\overline{\text{ExtReq}}$	Y4	External Master Peripheral	34
$\overline{\text{ExtReset}}$	T3	External Master Peripheral	34
GND	A1 A2 A6 A11 A16 A19 A21 A26 B2 B25 B26 C3 C24 D4 D23 E5 E9 E13 E14 E18 F1 F26 H1 J5 J22 L1 L11-L16 L26 M11-M16 N5 N11-N16 N22 P5 P11-P16 P22 R11-R16 T1 T11-T16 T26 V5 V22 W26 AA1 AA26 AB5	Ground **Note:** L11-L16, M11-M16, N11-N16, P11-P16, R11-R16, and T11-T16 are also thermal balls.	37

Signals Listed Alphabetically (Sheet 3 of 9)

Signal Name	Ball	Interface Group	Page
GND	AB9 AB13 AB14 AB18 AB22 AC4 AC23 AD3 AD24 AE1 AE2 AE25 AF1 AF6 AF8 AF11 AF16 AF21 AF25 AF26	Ground **Note:** L11-L16, M11-M16, N11-N16, P11-P16, R11-R16, and T11-T16 are also thermal balls.	37
Gnt[PCIReq0]	C19	PCI	30
GPIO1[TS1E] GPIO2[TS2E] GPIO3[TS1O] GPIO4[TS2O] GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6] GPIO9[TrcClk]	D18 C20 A22 AF18 AC9 AE8 AF5 AC7 AB3	System	35
[GPIO10]PerCS1 [GPIO11]PerCS2 [GPIO12]PerCS3 [GPIO13]PerCS4 [GPIO14]PerCS5 [GPIO15]PerCS6 [GPIO16]PerCS7	C4 C5 A4 B9 B10 A9 B11	System	35
[GPIO17]IRQ0 [GPIO18]IRQ1 [GPIO19]IRQ2 [GPIO20]IRQ3 [GPIO21]IRQ4 [GPIO22]IRQ5 [GPIO23]IRQ6 GPIO24	V25 V23 W24 W25 Y24 Y25 AA24 D20	System	35
Halt	AB26	System	35
HoldAck	U2	External Master Peripheral	34
HoldPri	T2	External Master Peripheral	34
HoldReq	V1	External Master Peripheral	34
IICSCL	AD6	Internal Peripheral	34
IICSDA	AE7	Internal Peripheral	34
IRQ0[GPIO17] IRQ1[GPIO18] IRQ2[GPIO19] IRQ3[GPIO20] IRQ4[GPIO21] IRQ5[GPIO22] IRQ6[GPIO23]	V25 V23 W24 W25 Y24 Y25 AA24	Interrupts	35

Signals Listed Alphabetically (Sheet 4 of 9)

Signal Name	Ball	Interface Group	Page
MemAddr0 MemAddr1 MemAddr2 MemAddr3 MemAddr4 MemAddr5 MemAddr6 MemAddr7 MemAddr8 MemAddr9 MemAddr10 MemAddr11 MemAddr12	AE22 AC21 AE21 AD21 AF22 AE20 AC19 AE19 AD19 AC18 AF19 AD18 AC17	SDRAM **Note:** During a $\overline{CAS}$ cycle MemAddr0 is the least significant bit (lsb) on this bus.	32
MemClkOut0 MemClkOut1	AC26 AA23	SDRAM	32
MemData0 MemData1 MemData2 MemData3 MemData4 MemData5 MemData6 MemData7 MemData8 MemData9 MemData10 MemData11 MemData12 MemData13 MemData14 MemData15 MemData16 MemData17 MemData18 MemData19 MemData20 MemData21 MemData22 MemData23 MemData24 MemData25 MemData26 MemData27 MemData28 MemData29 MemData30 MemData31	AC13 AE12 AD11 AC11 AF10 AE11 AD10 AF9 AD9 AE9 AD8 AF7 AC8 AD7 AE6 AE5 AE4 AD5 AD4 AC5 AD1 AB2 AA4 AA2 AB1 Y2 W4 W2 W3 V4 W1 V3	SDRAM **Note:** MemData0 is the most significant bit (msb) on this bus.	32

Signals Listed Alphabetically (Sheet 5 of 9)

Signal Name	Ball	Interface Group	Page
OV_{DD}	B17 C13 E6 E7 E8 E19 E20 E21 F5 F22 G5 G22 H5 H22 K2 N24 P3 U25 W5 W22 Y5 Y22 AA5 AA22 AB6 AB7 AB8 AB19 AB20 AB21 AD14 AE10	Output driver voltage	37
PCIAD0 PCIAD1 PCIAD2 PCIAD3 PCIAD4 PCIAD5 PCIAD6 PCIAD7 PCIAD8 PCIAD9 PCIAD10 PCIAD11 PCIAD12 PCIAD13 PCIAD14 PCIAD15 PCIAD16 PCIAD17 PCIAD18 PCIAD19 PCIAD20 PCIAD21 PCIAD22 PCIAD23 PCIAD24 PCIAD25 PCIAD26 PCIAD27 PCIAD28 PCIAD29 PCIAD30 PCIAD31	A17 B16 C17 A18 D17 C18 B18 A20 B21 A23 D21 B22 B23 C22 C26 F25 K26 L23 M25 M23 N25 M26 N26 P24 R24 R23 P23 R25 T24 U26 T25 V26	PCI **Note**: PCIAD31 is the most significant bit (msb) on this bus.	30
PCIC0[$\overline{BE0}$] PCIC1[$\overline{BE1}$] PCIC2[$\overline{BE2}$] PCIC3[$\overline{BE3}$]	D19 F24 K24 R26	PCI	30

Signals Listed Alphabetically (Sheet 6 of 9)

Signal Name	Ball	Interface Group	Page
PCIClk	B20	PCI	30
PCIDevSel	H25	PCI	30
PCIFrame	J24	PCI	30
PCIGnt0[Req] PCIGnt1 PCIGnt2 PCIGnt3 PCIGnt4 PCIGnt5	U23 T23 F23 H26 N23 M24	PCI	30
PCIIDSel	P26	PCI	30
PCIINT[PerWE]	C23	PCI	30
PCIIRDY	J23	PCI	30
PCIParity	E26	PCI	30
PCIPErr	G25	PCI	30
PCIReq0[Gnt] PCIReq1 PCIReq2 PCIReq3 PCIReq4 PCIReq5	C19 C21 B19 A24 G23 J25	PCI	30
PCIReset	B24	PCI	30
PCISErr	G24	PCI	30
PCIStop	H23	PCI	30
PCITRDY	G26	PCI	30
PerAddr0 PerAddr1 PerAddr2 PerAddr3 PerAddr4 PerAddr5 PerAddr6 PerAddr7 PerAddr8 PerAddr9 PerAddr10 PerAddr11 PerAddr12 PerAddr13 PerAddr14 PerAddr15 PerAddr16 PerAddr17 PerAddr18 PerAddr19 PerAddr20 PerAddr21 PerAddr22 PerAddr23 PerAddr24 PerAddr25 PerAddr26 PerAddr27 PerAddr28 PerAddr29 PerAddr30 PerAddr31	D5 A3 B4 B5 D6 B6 C6 D7 A5 B7 C7 D8 B8 C8 D9 A8 C9 D10 C10 A10 D11 B12 D13 D12 B13 A12 A13 C14 A14 A15 C15 D15	External Slave Peripheral	32
PerBLast	F2	External Slave Peripheral	32
PerClk	E4	External Master Peripheral	34

Signals Listed Alphabetically (Sheet 7 of 9)

Signal Name	Ball	Interface Group	Page
PerCS0 PerCS1[GPIO10] PerCS2[GPIO11] PerCS3[GPIO12] PerCS4[GPIO13] PerCS5[GPIO14] PerCS6[GPIO15] PerCS7[GPIO16]	B3 C4 C5 A4 B9 B10 A9 B11	External Slave Peripheral	32
PerData0 PerData1 PerData2 PerData3 PerData4 PerData5 PerData6 PerData7 PerData8 PerData9 PerData10 PerData11 PerData12 PerData13 PerData14 PerData15 PerData16 PerData17 PerData18 PerData19 PerData20 PerData21 PerData22 PerData23 PerData24 PerData25 PerData26 PerData27 PerData28 PerData29 PerData30 PerData31	U4 U3 U1 T4 R2 P4 R4 P2 R1 P1 N3 N1 M1 N2 M3 M4 N4 M2 L3 L4 K1 L2 K3 J1 K4 J3 J2 J4 H3 G1 H2 H4	External Slave Peripheral	32
PerErr	B1	External Master Peripheral	34
PerOE	C2	External Slave Peripheral	32
PerPar0 PerPar1 PerPar2 PerPar3	D3 G4 G3 E1	External Slave Peripheral	32
PerReady	E3	External Slave Peripheral	32
PerR/W	C1	External Slave Peripheral	32
PerWBE0 PerWBE1 PerWBE2 PerWBE3	D2 E2 F4 D1	External Slave Peripheral	32
[PerWE]PCIINT	C23	External Slave Peripheral	32
PHYCol	AA25	Ethernet	31
PHYCrS	W23	Ethernet	31
PHYRxClk	AF20	Ethernet	31
PHYMDIO[EMCMDIO]	AD26	Ethernet	31
PHYRxD0 PHYRxD1 PHYRxD2 PHYRxD3	AE23 AF23 AC20 AD20	Ethernet	31
PHYRxDV	V24	Ethernet	31

Signals Listed Alphabetically (Sheet 8 of 9)

Signal Name	Ball	Interface Group	Page
PHYRxErr	U24	Ethernet	31
PHYTxClk	E25	Ethernet	31
$\overline{\text{RAS}}$	AF24	SDRAM	32
Reserved	C25 E23 E24 Y23 Y26 AF4[1]	Other **Note:** AF4 must be tied to OV_{DD} or GND. All other reserved pins should be left unconnected.	37
$\overline{\text{Req}}$[$\overline{\text{PCIGnt0}}$]	U23	PCI	30
SysClk	A25	System	35
SysErr	AD25	System	35
$\overline{\text{SysReset}}$	D22	System	35
TCK	AD22	JTAG	35
TDI	AE24	JTAG	35
TDO	AD23	JTAG	35
TestEn	D26	System	35
TmrClk	D24	System	35
TMS	AC22	JTAG	35
$\overline{\text{TRST}}$	AE26	JTAG	35
[TS1E]GPIO1 [TS2E]GPIO2 [TS1O]GPIO3 [TS2O]GPIO4 [TS3]GPIO5 [TS4]GPIO6 [TS5]GPIO7 [TS6]GPIO8 [TrcClk]GPIO9	D18 C20 A22 AF18 AC9 AE8 AF5 AC7 AB3	System	35
$\overline{\text{UART0\_CTS}}$	AB4	Internal Peripheral	34
$\overline{\text{UART0\_DCD}}$	AE18	Internal Peripheral	34
$\overline{\text{UART0\_DSR}}$	AE3	Internal Peripheral	34
$\overline{\text{UART0\_DTR}}$	AF2	Internal Peripheral	34
$\overline{\text{UART0\_RI}}$	AD15	Internal Peripheral	34
$\overline{\text{UART0\_RTS}}$	AD16	Internal Peripheral	34
UART0_Rx	AE16	Internal Peripheral	34
UART0_Tx	AF3	Internal Peripheral	34
$\overline{\text{UART1\_CTS}}$/$\overline{\text{UART1\_DSR}}$	AC3	Internal Peripheral	34
$\overline{\text{UART1\_DSR}}$/$\overline{\text{UART1\_CTS}}$	AC3	Internal Peripheral	34
$\overline{\text{UART1\_DTR}}$/$\overline{\text{UART1\_RTS}}$	AD2	Internal Peripheral	34
$\overline{\text{UART1\_RTS}}$/$\overline{\text{UART1\_DTR}}$	AD2	Internal Peripheral	34
UART1_Rx	AC1	Internal Peripheral	34
UART1_Tx	AC2	Internal Peripheral	34
UARTSerClk	AE17	Internal Peripheral	34

Signals Listed Alphabetically (Sheet 9 of 9)

Signal Name	Ball	Interface Group	Page
V_{DD}	E10 E11 E12 E15 E16 E17 K5 K22 L5 L22 M5 M22 R5 R22 T5 T22 U5 U22 AB10 AB11 AB12 AB15 AB16 AB17	Logic voltage	37
$\overline{WE}$	AC16	SDRAM	32

Signals Listed by Ball Assignment (Sheet 1 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A1	GND	B14	DMAAck2	D1	PerWBE3	E14	GND
A2	GND	B15	DMAAck1	D2	PerWBE0	E15	V_{DD}
A3	PerAddr1	B16	PCIAD1	D3	PerPar0	E16	V_{DD}
A4	PerCS3[GPIO12]	B17	OV_{DD}	D4	GND	E17	V_{DD}
A5	PerAddr8	B18	PCIAD6	D5	PerAddr0	E18	GND
A6	GND	B19	PCIReq2	D6	PerAddr4	E19	OV_{DD}
A7	DMAReq3	B20	PCIClk	D7	PerAddr7	E20	OV_{DD}
A8	PerAddr15	B21	PCIAD8	D8	PerAddr11	E21	OV_{DD}
A9	PerCS6[GPIO15]	B22	PCIAD11	D9	PerAddr14	E22	AGND
A10	PerAddr19	B23	PCIAD12	D10	PerAddr17	E23	Reserved
A11	GND	B24	PCIReset	D11	PerAddr20	E24	Reserved
A12	PerAddr25	B25	GND	D12	PerAddr23	E25	PHYTxClk
A13	PerAddr26	B26	GND	D13	PerAddr22	E26	PCIParity
A14	PerAddr28	C1	PerR/W	D14	DMAReq1	F1	GND
A15	PerAddr29	C2	PerOE	D15	PerAddr31	F2	PerBLast
A16	GND	C3	GND	D16	DMAAck0	F3	EOT0/TC0
A17	PCIAD0	C4	PerCS1[GPIO10]	D17	PCIAD4	F4	PerWBE2
A18	PCIAD3	C5	PerCS2[GPIO11]	D18	GPIO1[TS1E]	F5	OV_{DD}
A19	GND	C6	PerAddr6	D19	PCIC0[BE0]	F22	OV_{DD}
A20	PCIAD7	C7	PerAddr10	D20	GPIO24	F23	PCIGnt2
A21	GND	C8	PerAddr13	D21	PCIAD10	F24	PCIC1[BE1]
A22	GPIO3[TS1O]	C9	PerAddr16	D22	SysReset	F25	PCIAD15
A23	PCIAD9	C10	PerAddr18	D23	GND	F26	GND
A24	PCIReq3	C11	DMAReq2	D24	TmrClk	G1	PerData29
A25	SysClk	C12	DMAAck3	D25	AV_{DD}	G2	EOT1/TC1
A26	GND	C13	OV_{DD}	D26	TestEn	G3	PerPar2
B1	PerErr	C14	PerAddr27	E1	PerPar3	G4	PerPar1
B2	GND	C15	PerAddr30	E2	PerWBE1	G5	OV_{DD}
B3	PerCS0	C16	DMAReq0	E3	PerReady	G22	OV_{DD}
B4	PerAddr2	C17	PCIAD2	E4	PerClk	G23	PCIReq4
B5	PerAddr3	C18	PCIAD5	E5	GND	G24	PCISErr
B6	PerAddr5	C19	PCIReq0[Gnt]	E6	OV_{DD}	G25	PCIPErr
B7	PerAddr9	C20	GPIO2[TS2E]	E7	OV_{DD}	G26	PCITRDY
B8	PerAddr12	C21	PCIReq1	E8	OV_{DD}	H1	GND
B9	PerCS4[GPIO13]	C22	PCIAD13	E9	GND	H2	PerData30
B10	PerCS5[GPIO14]	C23	PCIINT[PerWE]	E10	V_{DD}	H3	PerData28
B11	PerCS7[GPIO16]	C24	GND	E11	V_{DD}	H4	PerData31
B12	PerAddr21	C25	Reserved	E12	V_{DD}	H5	OV_{DD}
B13	PerAddr24	C26	PCIAD14	E13	GND	H22	OV_{DD}
H23	PCIStop	M1	PerData12	P14	GND	U1	PerData2
H24	EMCMDClk	M2	PerData17	P15	GND	U2	HoldAck
H25	PCIDevSel	M3	PerData14	P16	GND	U3	PerData1
H26	PCIGnt3	M4	PerData15	P22	GND	U4	PerData0

Signals Listed by Ball Assignment (Sheet 2 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J1	PerData23	M5	V_{DD}	P23	PCIAD26	U5	V_{DD}
J2	PerData26	M11	GND	P24	PCIAD23	U22	V_{DD}
J3	PerData25	M12	GND	P25	EMCTxD3	U23	$\overline{\text{PCIGnt0}}$[$\overline{\text{Req}}$]
J4	PerData27	M13	GND	P26	PCIIDSel	U24	PHYRxErr
J5	GND	M14	GND	R1	PerData8	U25	OV_{DD}
J22	GND	M15	GND	R2	PerData4	U26	PCIAD29
J23	$\overline{\text{PCIIRDY}}$	M16	GND	R3	BusReq	V1	HoldReq
J24	$\overline{\text{PCIFrame}}$	M22	V_{DD}	R4	PerData6	V2	EOT2/TC2
J25	$\overline{\text{PCIReq5}}$	M23	PCIAD19	R5	V_{DD}	V3	MemData31
J26	EMCTxD0	M24	$\overline{\text{PCIGnt5}}$	R11	GND	V4	MemData29
K1	PerData20	M25	PCIAD18	R12	GND	V5	GND
K2	OV_{DD}	M26	PCIAD21	R13	GND	V22	GND
K3	PerData22	N1	PerData11	R14	GND	V23	IRQ1[GPIO18]
K4	PerData24	N2	PerData13	R15	GND	V24	PHYRxDV
K5	V_{DD}	N3	PerData10	R16	GND	V25	IRQ0[GPIO17]
K22	V_{DD}	N4	PerData16	R22	V_{DD}	V26	PCIAD31
K23	EMCTxEn	N5	GND	R23	PCIAD25	W1	MemData30
K24	PCIC2[$\overline{\text{BE2}}$]	N11	GND	R24	PCIAD24	W2	MemData27
K25	EMCTxErr	N12	GND	R25	PCIAD27	W3	MemData28
K26	PCIAD16	N13	GND	R26	PCIC3[$\overline{\text{BE3}}$]	W4	MemData26
L1	GND	N14	GND	T1	GND	W5	OV_{DD}
L2	PerData21	N15	GND	T2	HoldPri	W22	OV_{DD}
L3	PerData18	N16	GND	T3	$\overline{\text{ExtReset}}$	W23	PHYCrS
L4	PerData19	N22	GND	T4	PerData3	W24	IRQ2[GPIO19]
L5	V_{DD}	N23	$\overline{\text{PCIGnt4}}$	T5	V_{DD}	W25	IRQ3[GPIO20]
L11	GND	N24	OV_{DD}	T11	GND	W26	GND
L12	GND	N25	PCIAD20	T12	GND	Y1	EOT3/TC3
L13	GND	N26	PCIAD22	T13	GND	Y2	MemData25
L14	GND	P1	PerData9	T14	GND	Y3	$\overline{\text{ExtAck}}$
L15	GND	P2	PerData7	T15	GND	Y4	$\overline{\text{ExtReq}}$
L16	GND	P3	OV_{DD}	T16	GND	Y5	OV_{DD}
L22	V_{DD}	P4	PerData5	T22	V_{DD}	Y22	OV_{DD}
L23	PCIAD17	P5	GND	T23	$\overline{\text{PCIGnt1}}$	Y23	Reserved
L24	EMCTxD2	P11	GND	T24	PCIAD28	Y24	IRQ4[GPIO21]
L25	EMCTxD1	P12	GND	T25	PCIAD30	Y25	IRQ5[GPIO22]
L26	GND	P13	GND	T26	GND	Y26	Reserved
AA1	GND	AB26	$\overline{\text{Halt}}$	AD9	MemData8	AE18	$\overline{\text{UART0\_DCD}}$
AA2	MemData23	AC1	UART1_Rx	AD10	MemData6	AE19	MemAddr7
AA3	DQM3	AC2	UART1_Tx	AD11	MemData2	AE20	MemAddr5
AA4	MemData22	AC3	$\overline{\text{UART1\_DSR}}$/ $\overline{\text{UART1\_CTS}}$	AD12	ECC7	AE21	MemAddr2
AA5	OV_{DD}	AC4	GND	AD13	ECC3	AE22	MemAddr0
AA22	OV_{DD}	AC5	MemData19	AD14	OV_{DD}	AE23	PHYRxD0
AA23	MemClkOut1	AC6	DQM2	AD15	$\overline{\text{UART0\_RI}}$	AE24	TDI
AA24	IRQ6[GPIO23]	AC7	GPIO8[TS6]	AD16	$\overline{\text{UART0\_RTS}}$	AE25	GND

Signals Listed by Ball Assignment (Sheet 3 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA25	PHYCol	AC8	MemData12	AD17	$\overline{\text{BankSel0}}$	AE26	$\overline{\text{TRST}}$
AA26	GND	AC9	GPIO5[TS3]	AD18	MemAddr11	AF1	GND
AB1	MemData24	AC10	DQM1	AD19	MemAddr8	AF2	$\overline{\text{UART0\_DTR}}$
AB2	MemData21	AC11	MemData3	AD20	PHYRxD3	AF3	UART0_Tx
AB3	GPIO9[TrcClk]	AC12	DQM0	AD21	MemAddr3	AF4	Reserved
AB4	$\overline{\text{UART0\_CTS}}$	AC13	MemData0	AD22	TCK	AF5	GPIO7[TS5]
AB5	GND	AC14	$\overline{\text{BankSel3}}$	AD23	TDO	AF6	GND
AB6	OV_{DD}	AC15	DQMCB	AD24	GND	AF7	MemData11
AB7	OV_{DD}	AC16	$\overline{\text{WE}}$	AD25	SysErr	AF8	GND
AB8	OV_{DD}	AC17	MemAddr12	AD26	EMCMDIO [PHYMDIO]	AF9	MemData7
AB9	GND	AC18	MemAddr9	AE1	GND	AF10	MemData4
AB10	V_{DD}	AC19	MemAddr6	AE2	GND	AF11	GND
AB11	V_{DD}	AC20	PHYRxD2	AE3	$\overline{\text{UART0\_DSR}}$	AF12	ECC5
AB12	V_{DD}	AC21	MemAddr1	AE4	MemData16	AF13	ECC4
AB13	GND	AC22	TMS	AE5	MemData15	AF14	ECC2
AB14	GND	AC23	GND	AE6	MemData14	AF15	ECC1
AB15	V_{DD}	AC24	BA1	AE7	IICSDA	AF16	GND
AB16	V_{DD}	AC25	ClkEn1	AE8	GPIO6[TS4]	AF17	$\overline{\text{BankSel1}}$
AB17	V_{DD}	AC26	MemClkOut0	AE9	MemData9	AF18	GPIO4[TS2O]
AB18	GND	AD1	MemData20	AE10	OV_{DD}	AF19	MemAddr10
AB19	OV_{DD}	AD2	$\overline{\text{UART1\_RTS}}$/ $\overline{\text{UART1\_DTR}}$	AE11	MemData5	AF20	PHYRxClk
AB20	OV_{DD}	AD3	GND	AE12	MemData1	AF21	GND
AB21	OV_{DD}	AD4	MemData18	AE13	ECC6	AF22	MemAddr4
AB22	GND	AD5	MemData17	AE14	ECC0	AF23	PHYRxD1
AB23	$\overline{\text{CAS}}$	AD6	IICSCL	AE15	$\overline{\text{BankSel2}}$	AF24	$\overline{\text{RAS}}$
AB24	BA0	AD7	MemData13	AE16	UART0_Rx	AF25	GND
AB25	ClkEn0	AD8	MemData10	AE17	UARTSerClk	AF26	GND

Signal List

The following table provides a summary of the number of package pins associated with each functional interface group.

Pin Summary

Group	No. of Pins
PCI	60
Ethernet	18
SDRAM	71
External peripheral	96
External master	9
Internal peripheral	15
Interrupts	7
JTAG	5
System	18
Total Signal Pins	**299**
OV_{DD}	32
V_{DD}	24
Gnd	59
Thermal (and Gnd)	36
Reserved	6
Total Pins	**456**

Multiplexed Pins

In the table “Signal Functional Description” on page 30, each external signal is listed along with a description of the signal function. Some signals are multiplexed on the same pin (ball) so that the pin can be used for different functions. Multiplexed signals are shown as a default signal with a secondary signal in square brackets (for example, GPIO1[TS1E]). Active-low signals (for example, $\overline{RAS}$) are marked with an overline.

It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, many pins are also multi-purpose. For example, the EBC peripheral controller address pins are used as outputs by the PPC405GPr to broadcast an address to external slave devices when the PPC405GPr has control of the external bus. When, during the course of normal chip operation, an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC405GPr. In this example, the pins are also bidirectional, serving as both inputs and outputs.

Intialization Strapping

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 51). Note that the use of these pins for strapping is not considered multiplexing since the strapping function is not programmable.

Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors are used for strapping during reset and to retain unused or undriven inputs in an appropriate state. The recommended pull-up value of 3kΩ to +3.3V (10kΩ to +5V can be used on 5V tolerant I/Os) and pull-down value of 1kΩ to GND, applies only to individually terminated signals. To prevent possible damage to the device, I/Os capable of becoming outputs *must never* be tied together and terminated through a common resistor.

If your system-level test methodology permits, input-only signals can be connected together and terminated through either a common resistor or directly to +3.3V or GND. When a resistor is used, its value must ensure that the grouped I/Os reach a valid logic zero or logic one state when accounting for the total input current into the PPC405GPr.

Unused I/Os

For some interfaces, it is possible to turn off input receivers for some or all of the signals by means of bit settings in register CPC0_CR1. When this gating capability is applied to unused signals, it is not necessary to terminate them. Refer to the *PowerPC 405GPr Embedded Processor User's Manual* for details.

If receiver gating is not used, termination of some pins may be necessary when they are unused. Although the PPC405GPr requires only the pull-up and pull-down terminations as specified in the "Signal Functional Description" on page 30, good design practice is to terminate all unused inputs or to configure I/Os such that they always drive. If unused, and receiver gating is not used, the peripheral, SDRAM, and PCI buses should be configured and terminated as follows:

- Peripheral interface—PerAddr0:31, PerData0:31, and all of the control signals are driven by default. Terminate PerReady high and PerError low.
- SDRAM—Program SDRAM0_CFG[EMDULR]=1 and SDRAM0_CFG[DCE]=1. This causes the PPC405GPr to actively drive all of the SDRAM address, data, and control signals.
- PCI—The PCI pull-up requirements given in the Signal Functional Description apply only when the PCI interface is being used. When the PCI bridge is unused, configure the PCI controller to park on the bus and actively drive PCIAD31:0, PCIC3:0[$\overline{\text{BE3:0}}$], and the remaining PCI control signals by doing the following:
  - Strap the PPC405GPr to disable the internal PCI arbiter and to operate the PCI interface in synchronous mode.
  - Individually connect $\overline{\text{PCISErr}}$, $\overline{\text{PCIPErr}}$, $\overline{\text{PCITRDY}}$, and $\overline{\text{PCIStop}}$ through 3kΩ resistors to +3.3V.
  - Terminate $\overline{\text{PCIReq1:5}}$ to +3.3V.
  - Terminate $\overline{\text{PCIReq0}}$[$\overline{\text{Gnt}}$] to GND.

External Bus Control Signals

All peripheral bus control signals ($\overline{\text{PerCS0:7}}$, PerR/$\overline{\text{W}}$, $\overline{\text{PerWBE0:3}}$, $\overline{\text{PerOE}}$, $\overline{\text{PerWE}}$, $\overline{\text{PerBLast}}$, HoldAck, $\overline{\text{ExtAck}}$) are set to the high-impedance state when $\overline{\text{ExtReset}}$=0. In addition, as detailed in the *PowerPC 405GPr Embedded Processor User's Manual*, the peripheral bus controller can be programmed via EBC0_CFG to float some of these control signals between transactions and/or when an external master owns the peripheral bus. As a result, a pull-up resistor should be added to those control signals where an undriven state may affect any devices receiving that particular signal.

The following table lists all of the I/O signals provided by the PPC405GPr. Please refer to "Signals Listed Alphabetically" on page 16 for the pin number to which each signal is assigned.

Signal Functional Description (Sheet 1 of 8)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 29.

Signal Name	Description	I/O	Type	Notes
PCI Interface				
PCIAD31:0	PCI Address/Data Bus. Multiplexed address and data bus.	I/O	5V tolerant 3.3V PCI	
PCIC3:0[$\overline{\text{BE3:0}}$]	PCI bus command and byte enables.	I/O	5V tolerant 3.3V PCI	
PCIParity	PCI parity. Parity is even across PCIAD0:31 and PCIC0:3[$\overline{\text{BE0:3}}$]. PCIParity is valid one cycle after either an address or data phase. The PCI device that drove PCIAD0:31 is responsible for driving PCIParity on the next PCI bus clock.	I/O	5V tolerant 3.3V PCI	
$\overline{\text{PCIFrame}}$	$\overline{\text{PCIFrame}}$ is driven by the current PCI bus master to indicate the beginning and duration of a PCI access.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCIIRDY}}$	$\overline{\text{PCIIRDY}}$ is driven by the current PCI bus master. Assertion of $\overline{\text{PCIIRDY}}$ indicates that the PCI initiator is ready to transfer data.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCITRDY}}$	The target of the current PCI transaction drives $\overline{\text{PCITRDY}}$. Assertion of $\overline{\text{PCITRDY}}$ indicates that the PCI target is ready to transfer data.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCIStop}}$	The target of the current PCI transaction can assert $\overline{\text{PCIStop}}$ to indicate to the requesting PCI master that it wants to end the current transaction.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCIDevSel}}$	$\overline{\text{PCIDevSel}}$ is driven by the target of the current PCI transaction. A PCI target asserts $\overline{\text{PCIDevSel}}$ when it has decoded an address and command encoding and claims the transaction.	I/O	5V tolerant 3.3V PCI	2
PCIIDSel	PCIIDSel is used during configuration cycles to select the PCI slave interface for configuration.	I	5V tolerant 3.3V PCI	
$\overline{\text{PCISErr}}$	$\overline{\text{PCISErr}}$ is used for reporting address parity errors or catastrophic failures detected by a PCI target.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCIPErr}}$	$\overline{\text{PCIPErr}}$ is used for reporting data parity errors on PCI transactions. $\overline{\text{PCIPErr}}$ is driven active by the device receiving PCIAD0:31, PCIC0:3[$\overline{\text{BE0:3}}$], and PCIParity, two PCI clocks following the data in which bad parity is detected.	I/O	5V tolerant 3.3V PCI	2
PCIClk	PCIClk is used as the asynchronous PCI clock when in asynchronous mode. It is unused when the PCI interface is operated synchronously with the PLB bus.	I	5V tolerant 3.3V PCI	
$\overline{\text{PCIReset}}$	PCI specific reset.	O	5V tolerant 3.3V PCI	
$\overline{\text{PCIINT}}$[$\overline{\text{PerWE}}$]	PCI interrupt. Open-drain output (two states; 0 or open circuit) or Peripheral write enable. Low when any of the four $\overline{\text{PerWBE0:3}}$ write byte enables are low.	O	5V tolerant 3.3V PCI	
$\overline{\text{PCIReq0}}$[$\overline{\text{Gnt}}$]	Multipurpose signal, used as $\overline{\text{PCIReq0}}$ when internal arbiter is used, and as $\overline{\text{Gnt}}$ when external arbiter is used.	I	5V tolerant 3.3V PCI	
$\overline{\text{PCIReq1:5}}$	Used as $\overline{\text{PCIReq1:5}}$ input when internal arbiter is used.	I	5V tolerant 3.3V PCI	

Signal Functional Description (Sheet 2 of 8)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See "Pull-Up and Pull-Down Resistors" on page 29 for recommended termination values.
3. Must pull down. See "Pull-Up and Pull-Down Resistors" on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See "External Bus Control Signals" on page 29.

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PCIGnt0}}$[$\overline{\text{Req}}$]	$\overline{\text{Gnt0}}$ when internal arbiter is used or $\overline{\text{Req}}$ when external arbiter is used.	O	5V tolerant 3.3V PCI	
$\overline{\text{PCIGnt1:5}}$	Used as $\overline{\text{PCIGnt1:5}}$ output when internal arbiter is used.	O	5V tolerant 3.3V PCI	
Ethernet Interface				
PHYRxD3:0	Received data. This is a nibble wide bus from the PHY. The data is synchronous with the PHYRxClk.	I	5V tolerant 3.3V LVTTL	1
EMCTxD3:0	Transmit data. A nibble wide data bus towards the net. The data is synchronous to the PHYTxClk.	O	5V tolerant 3.3V LVTTL	6
PHYRxErr	Receive Error. This signal comes from the PHY and is synchronous to the PHYRxClk.	I	5V tolerant 3.3V LVTTL	1
PHYRxClk	Receiver Medium clock. This signal is generated by the PHY.	I	5V tolerant 3.3V LVTTL	1
PHYRxDV	Receive Data Valid. Data on the Data Bus is valid when this signal is activated. Deassertion of this signal indicates end of the frame reception.	I	5V tolerant 3.3V LVTTL	1
PHYCrS	Carrier Sense signal from the PHY. This is an asynchronous signal.	I	5V tolerant 3.3V LVTTL	1
EMCTxErr	Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHYTxClk. It informs the PHY that an error was detected.	O	5V tolerant 3.3V LVTTL	6
EMCTxEn	Transmit Enable. This signal is driven by the EMAC to the PHY. Data is valid during the active state of this signal. Deassertion of this signal indicates end of frame transmission. This signal is synchronous to the PHYTxClk.	O	5V tolerant 3.3V LVTTL	6
PHYTxClk	This clock comes from the PHY and is the Medium Transmit clock.	I	5V tolerant 3.3V LVTTL	1
PHYCol	Collision signal from the PHY. This is an asynchronous signal.	I	5V tolerant 3.3V LVTTL	1
EMCMDClk	Management Data Clock. The MDClk is sourced to the PHY. This clock has a period of 400ns, adjustable via EMAC0_STACR[OPBC]. Management information is transferred synchronously with respect to this clock.	O	5V tolerant 3.3V LVTTL	
EMCMDIO[PHYMDIO]	Management Data Input/Output is a bidirectional signal between the Ethernet controller and the PHY. It is used to transfer control and status information.	I/O	5V tolerant 3.3V LVTTL	1

Signal Functional Description (Sheet 3 of 8)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 29.

Signal Name	Description	I/O	Type	Notes
SDRAM Interface				
MemData0:31	Memory data bus. **Notes:** 1. MemData0 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb).	I/O	3.3V LVTTL	
MemAddr12:0	Memory address bus. **Notes:** 1. MemAddr12 is the most significant bit (msb). 2. MemAddr0 is the least significant bit (lsb).	O	3.3V LVTTL	
BA1:0	Bank Address supporting up to 4 internal banks.	O	3.3V LVTTL	
$\overline{\text{RAS}}$	Row Address Strobe.	O	3.3V LVTTL	
$\overline{\text{CAS}}$	Column Address Strobe.	O	3.3V LVTTL	
DQM0:3	DQM for byte lane: 0 (MemData0:7), 1 (MemData8:15), 2 (MemData16:23), and 3 (MemData24:31)	O	3.3V LVTTL	
DQMCB	DQM for ECC check bits.	O	3.3V LVTTL	
ECC0:7	ECC check bits 0:7.	I/O	3.3V LVTTL	
$\overline{\text{BankSel0:3}}$	Select up to four external SDRAM banks.	O	3.3V LVTTL	
$\overline{\text{WE}}$	Write Enable.	O	3.3V LVTTL	
ClkEn0:1	SDRAM Clock Enable.	O	3.3V LVTTL	
MemClkOut0:1	Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attach without requiring this signal to be repowered by a PLL or zero-delay buffer.	O	3.3V LVTTL	
External Slave Peripheral Interface				
PerData0:31	Peripheral data bus used by PPC405GPr when not in external master mode, otherwise used by external master. **Note:** PerData0 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerAddr0:31	Peripheral address bus used by PPC405GPr when not in external master mode, otherwise used by external master. **Note:** PerAddr0 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerPar0:3	Peripheral byte parity signals.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerWBE0:3}}$	As outputs, these pins can act as byte-enables which are valid for an entire cycle or as write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. As outputs, pins are used by either the pripheral controller or the DMA controller depending upon the type of transfer involved. Used as inputs when an external bus master owns the external interface.	I/O	5V tolerant 3.3V LVTTL	1, 7
[$\overline{\text{PerWE}}$]$\overline{\text{PCIINT}}$	Peripheral write enable. Low when any of the four $\overline{\text{PerWBE0:3}}$ write byte enables are low. or PCI interrupt. Open-drain output (two states; 0 or open circuit)	O	5V tolerant 3.3V PCI	

Signal Functional Description (Sheet 4 of 8)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 29.

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PerCS0}}$	Peripheral chip select bank 0.	O	5V tolerant 3.3V LVTTL	7
$\overline{\text{PerCS1:7}}$[GPIO10:16]	Seven additional peripheral chip selects or General Purpose I/O. To access this function, software must toggle a DCR bit.	O[I/O]	5V tolerant 3.3V LVTTL	1, 7
$\overline{\text{PerOE}}$	Used by either the peripheral controller or the DMA controller depending upon the type of transfer involved. When the PPC405GPr is the bus master, it enables the selected device to drive the bus.	O	5V tolerant 3.3V LVTTL	7
PerR/$\overline{\text{W}}$	Used by the PPC405GPr when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise it used by the external master as an input to indicate the direction of data transfer.	I/O	5V tolerant 3.3V LVTTL	1
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerBLast}}$	Used by the PPC405GPr when not in external master mode, otherwise used by external master. Indicates the last transfer of a memory access.	I/O	5V tolerant 3.3V LVTTL	1, 7
DMAReq0:3	DMAReq0:3 are used by slave peripherals to indicate they are prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1
DMAAck0:3	DMAAck0:3 are used by the PPC405GPr to cause the DMA peripheral to transfer data.	O	5V tolerant 3.3V LVTTL	6
EOT0:3/TC0:3	End Of Transfer/Terminal Count.	I/O	5V tolerant 3.3V LVTTL	1

Signal Functional Description (Sheet 5 of 8)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 29.

Signal Name	Description	I/O	Type	Notes
External Master Peripheral Interface				
PerClk	Peripheral clock to be used by an external master and by synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtReset}}$	Peripheral reset to be used by an external master and by synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
HoldReq	Hold Request, used by an external master to request ownership of the peripheral bus.	I	5V tolerant 3.3V LVTTL	1, 5
HoldAck	Hold Acknowledge, used by the PPC405GPr to transfer ownership of peripheral bus to an external master.	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{ExtReq}}$	ExtReq is used by an external master to indicate it is prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{ExtAck}}$	ExtAck is used by the PPC405GPr to indicate a data transfer cycle.	O	5V tolerant 3.3V LVTTL	6
HoldPri	Used by an external master to indicate the priority of a given external master tenure.	I	5V tolerant 3.3V LVTTL	1
BusReq	Used when the PPC405GPr needs to regain control of peripheral interface from an external master.	O	5V tolerant 3.3V LVTTL	
PerErr	An input used to indicate to the PPC405GPr that an external slave peripheral error occurred.	I	5V tolerant 3.3V LVTTL	1, 5
Internal Peripheral Interface				
UARTSerClk	Serial Clock used to provide an alternate clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either UART.	I	5V tolerant 3.3V LVTTL	1
UART0_Rx	UART0 Serial Data In.	I	5V tolerant 3.3V LVTTL	1
UART0_Tx	UART0 Serial Data Out.	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send.	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator.	I	5V tolerant 3.3V LVTTL	1
UART1_Rx	UART1 Serial Data In.	I	5V tolerant 3.3V LVTTL	1

Signal Functional Description (Sheet 6 of 8)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 29.

Signal Name	Description	I/O	Type	Notes
UART1_Tx	UART1 Serial Data Out.	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART1\_DSR}}$/ $\overline{\text{UART1\_CTS}}$	UART1 Data Set Ready or UART1 Clear To Send. To access this function, software must toggle a DCR bit.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{UART1\_RTS}}$/ $\overline{\text{UART1\_DTR}}$	UART1 Request To Send or UART1 Data Terminal Ready. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	6
IICSCL	IIC Serial Clock.	I/O	5V tolerant 3.3V LVTTL	1, 2
IICSDA	IIC Serial Data.	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface				
IRQ0:6[GPIO17:23]	Interrupt requests or General Purpose I/O. To access this function, software must toggle a DCR bit.	I[I/O]	5V tolerant 3.3V LVTTL	1
JTAG Interface				
TDI	Test data in.	I	5V tolerant 3.3V LVTTL	1, 4
TMS	JTAG test mode select.	I	5V tolerant 3.3V LVTTL	1, 4
TDO	Test data out.	O	5V tolerant 3.3V LVTTL	
TCK	JTAG test clock. The frequency of this input can range from DC to 25MHz.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{TRST}}$	JTAG reset. $\overline{\text{TRST}}$ must be low at power-on to initialize the JTAG controller and for normal operation of the PPC405GPr.	I	5V tolerant 3.3V LVTTL	5
System Interface				
SysClk	Main system clock input.	I	5V tolerant 3.3V LVTTL	
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software. Implemented as an open-drain output (two states; 0 or open circuit).	I/O	5V tolerant 3.3V LVTTL	1, 2
AV_{DD}	Clean voltage input for the PLL.	I		
AGND	Clean Ground input for the PLL.	I		
SysErr	Set to 1 when a Machine Check is generated.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL	1, 2

Signal Functional Description (Sheet 7 of 8)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 29.

Signal Name	Description	I/O	Type	Notes
GPIO1[TS1E] GPIO2[TS2E]	General Purpose I/O or Even Trace execution status. To access this function, software must toggle a DCR bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 6
GPIO3[TS1O]	General Purpose I/O or Odd Trace execution status. To access this function, software must toggle a DCR bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 6
GPIO4[TS2O]	General Purpose I/O or Odd Trace execution status. To access this function, software must toggle a DCR bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 6
GPIO5:8[TS3:6]	General Purpose I/O or Trace status. To access this function, software must toggle a DCR bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 6
GPIO9[TrcClk]	General Purpose I/O or Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR bit. **Note:** Initialization strapping must hold this pin low (0) during reset.	I/O[O]	5V tolerant 3.3V LVTTL	1, 6
GPIO24	General Purpose I/O. **Note:** The pull-up initialization strapping resistor must be 1kΩ rather than 3kΩ in order to overcome the internal pull-down resistor.	I/O	3.3V LVTTL w/pull-down	1, 6
TestEn	Test Enable. Used only for manufacturing tests. Pull down for normal operation.	I	1.8V CMOS w/pull-down	
TmrClk	An external clock input that can be used to clock the timers in the CPU core.	I	5V tolerant 3.3V LVTTL	1
Trace Interface				
[TS1E]GPIO1 [TS2E]GPIO2	Even Trace execution status. To access this function, software must toggle a DCR bit or General Purpose I/O.	O[I/O]	5V tolerant 3.3V LVTTL	1, 6
[TS1O]GPIO3	Odd Trace execution status. To access this function, software must toggle a DCR bit or General Purpose I/O.	O[I/O]	5V tolerant 3.3V LVTTL	1, 6
[TS2O]GPIO4	Odd Trace execution status. To access this function, software must toggle a DCR bit or General Purpose I/O.	O[I/O]	5V tolerant 3.3V LVTTL	1, 6
[TS3:6]GPIO5:8	Trace status. To access this function, software must toggle a DCR bit or General Purpose I/O.	O[I/O]	5V tolerant 3.3V LVTTL	1, 6

Signal Functional Description (Sheet 8 of 8)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 29.

Signal Name	Description	I/O	Type	Notes
[TrcClk]GPIO9	Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR bit or General Purpose I/O. **Note:** Initialization strapping must hold this pin low (0) during reset.	O[I/O]	5V tolerant 3.3V LVTTL	1, 6
Ground pins				
GND	Ground **Note:** L11-L16, M11-M16, N11-N16, P11-P16, R11-R16, and T11-T16 are also thermal balls.			
OV_{DD} pins				
OV_{DD}	Output driver voltage—3.3V.			
V_{DD} pins				
V_{DD}	Logic voltage—1.8V.			
Other pins				
Reserved	Reserved—Except for AF4, do not connect signals, voltage, or ground to these pins. AF4 must be tied to OV_{DD} or GND.			

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to +1.95	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to +3.6	V
PLL Supply Voltage	AV_{DD}	0 to +1.95	V
Input Voltage (1.8V CMOS receivers)	V_{IN}	-0.6 to V_{DD} + 0.45	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	-0.6 to OV_{DD} + 0.6	V
Input Voltage (5.0V LVTTL receivers)	V_{IN}	-0.6 to OV_{DD} + 2.4	V
Storage Temperature Range	T_{STG}	-55 to +150	°C
Case temperature under bias	T_C	-40 to +120	°C

Notes:

1. All specified voltages are with respect to GND.
2. Empirical data indicates that all chip voltages should begin to ramp-up within 1 ms of each other. There should never be voltage present at the I/O pins before OV_{DD} is within operating range.

Package Thermal Specifications

The PPC405GPr is designed to operate within a case temperature range of -40°C to +85°C[3]. Thermal resistance values for the E-PBGA packages (leaded and lead-free) in a convection environment are as follows:

Package—Thermal Resistance	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
35mm, 456-balls—Junction-to-Case	θ_{JC}	2	2	2	°C/W
35mm, 456-balls—Case-to-Ambient[1]	θ_{CA}	14	13	12	°C/W
27mm, 456-balls—Junction-to-Case	θ_{JC}	2	2	2	°C/W
27mm, 456-balls—Case-to-Ambient[1]	θ_{CA}	18	16	15	°C/W

Notes:

1. For a chip mounted on a JEDEC 2S2P card without a heat sink.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
   a. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
   b. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
   c. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.
3. 333MHz operated at 266MHz or less can operate at +105°C.

Recommended DC Operating Conditions

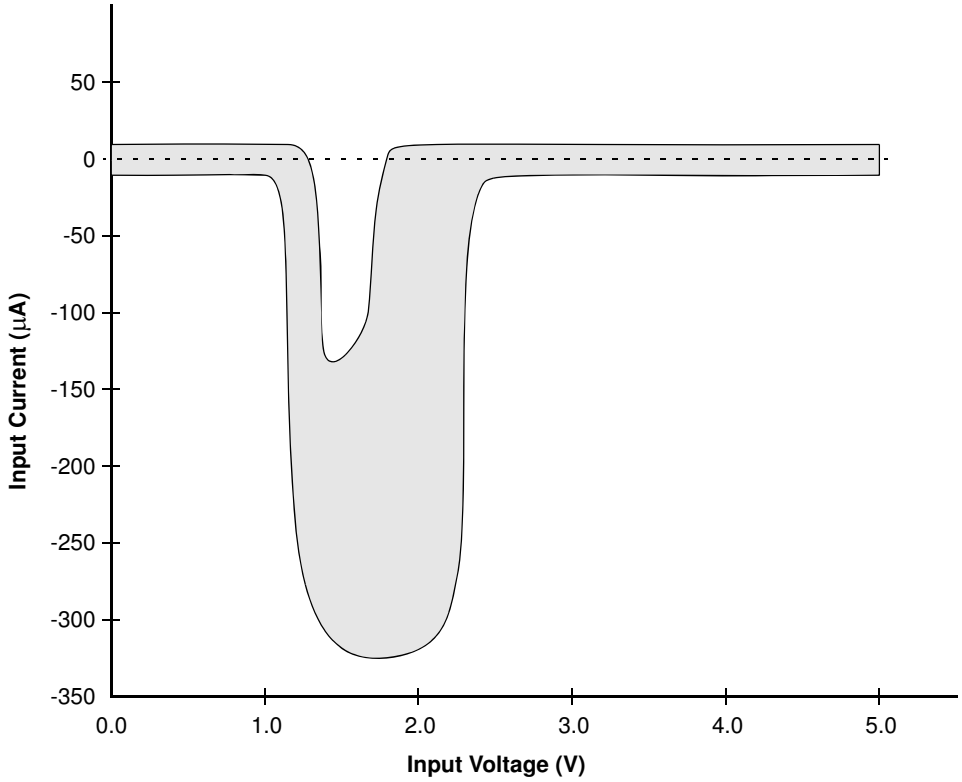
Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Notes:

1. PCI drivers meet PCI specifications.
2. See "5V-Tolerant Input Current" on page 40.
3. 333MHz operated at 266MHz or less can operate at +105°C.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage (266 &333MHz)	V_{DD}	1.7	1.8	1.9	V	
Logic Supply Voltage (400MHz)	V_{DD}	1.8	1.85	1.9	V	
I/O Supply Voltage	OV_{DD}	3.0	3.3	3.6	V	
PLL Supply Voltage	AV_{DD}	1.7	1.8	1.9	V	
Input Logic High (1.8V CMOS receivers)	V_{IH}	$0.65V_{DD}$		V_{DD}	V	
Input Logic High (3.3V LVTTL receivers)	V_{IH}	2.0		OV_{DD}	V	
Input Logic High (5.0V LVTTL receivers)	V_{IH}	2.0		5.0	V	
Input Logic Low (1.8V CMOS receivers)	V_{IL}	0		$0.65V_{DD}$	V	
Input Logic Low (3.3/5.0V LVTTL receivers)	V_{IL}	0		0.8	V	
Output Logic High	V_{OH}	2.4		OV_{DD}	V	
Output Logic Low	V_{OL}	0		0.4	V	
3.3V I/O Input Current (no pull-up or pull-down)	I_{IL1}			±10	µA	
Input Current (with internal pull-down)	I_{IL2}	±10 (@ 0V)		200 (@ V_{DD})	µA	
5V Tolerant I/O Input Current	I_{IL4}	±10		-325	µA	2
Input Max Allowable Overshoot (1.8V CMOS receivers)	$V_{IMAO1.8}$			V_{DD} + 0.6	V	
Input Max Allowable Overshoot (3.3V LVTTL receivers)	V_{IMAO3}			OV_{DD} + 0.6	V	
Input Max Allowable Overshoot (5.0V LVTTL receivers)	V_{IMAO5}			5.5	V	
Input Max Allowable Undershoot	V_{IMAU}	-0.6			V	
Output Max Allowable Overshoot	V_{OMAO}			OV_{DD} + 0.3	V	
Output Max Allowable Undershoot	V_{OMAU3}	-0.6			V	
Case Temperature	T_C	-40		+85	°C	3

5V-Tolerant Input Current



Input Capacitance

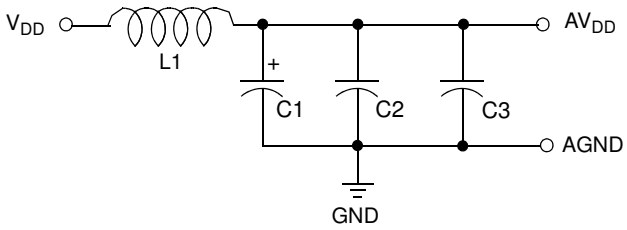
Parameter	Symbol	Maximum	Unit	Notes
3.3V LVTTL I/O	C_{IN1}	8.8	pF	
5V tolerant LVTTL I/O	C_{IN2}	8	pF	
PCI I/O	C_{IN3}	9.3	pF	
Rx only pins	C_{IN4}	4.5	pF	

DC Electrical Characteristics

Parameter	Symbol	Typical	Maximum	Unit
Active Operating Current (V_{DD})–266MHz	I_{DD}	300	610	mA
Active Operating Current (V_{DD})–333MHz	I_{DD}	325	690	mA
Active Operating Current (V_{DD})–400MHz	I_{DD}	355	770	mA
Active Operating Current (OV_{DD})	I_{ODD}	45	200	mA
PLL V_{DD} Input current	I_{PLL}	16	23	mA
Active Operating Power–266 MHz	P_{DD}	0.72	1.92	W
Active Operating Power–333MHz	P_{DD}	0.76	2.07	W
Active Operating Power–400MHz	P_{DD}	0.82	2.23	W

Note:

1. The maximum current and power values listed above are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results. V_{DD} (logic) current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, PCI, Ethernet, and so on). OV_{DD} (I/O) current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses. The following information provides details about the conditions under which the listed values were obtained:
   a. In general, the values were measured using a PPC405GPr Evaluation Board with four PCI devices, an external bus master on the peripheral bus, and external wrap-back on the Ethernet port. For all CPU clock rates, PLB = 133.3MHz, OPB = PerClk = 66.6MHz, PCI = SysClk = 33.3MHz.
   b. Typical current and power are characterized at V_{DD} = +1.8V, OV_{DD} = +3.3V, and T_C = +36°C while running various applications under the Linux operating system.
   c. Maximum current and power are characterized at V_{DD} = +1.9V, OV_{DD} = +3.6V, and T_C = +85°C while running applications designed to maximize CPU power consumption. An external PCI master heavily loads the PCI bus with transfers targeting SDRAM while the internal DMA controller further increases SDRAM bus traffic.
2. AV_{DD} should be derived from V_{DD} using the following circuit:



L1 – 2.2µH SMT inductor (equivalent to MuRata LQH3C2R2M34) or SMT chip ferrite bead (equivalent to MuRata BLM31A700S)

C1 – 3.3 µF SMT tantalum

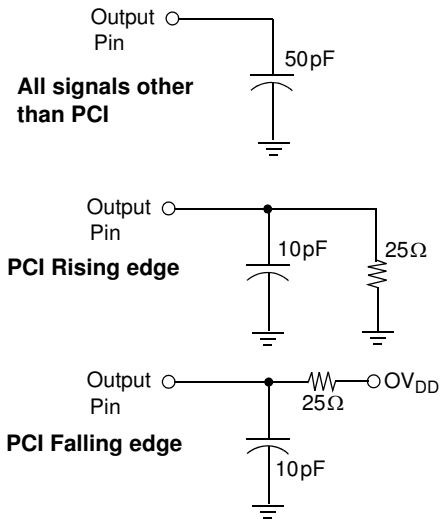
C2 – 0.1µF SMT monolithic ceramic capacitor with X7R dielectric or equivalent

C3 – 0.01µF SMT monolithic ceramic capacitor with X7R dielectric or equivalent

Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” For all signals other than PCI signals, AC specifications are characterized at OV_{DD} = +3V and T_C = +85°C with the 50pF test load shown in the figure at right.

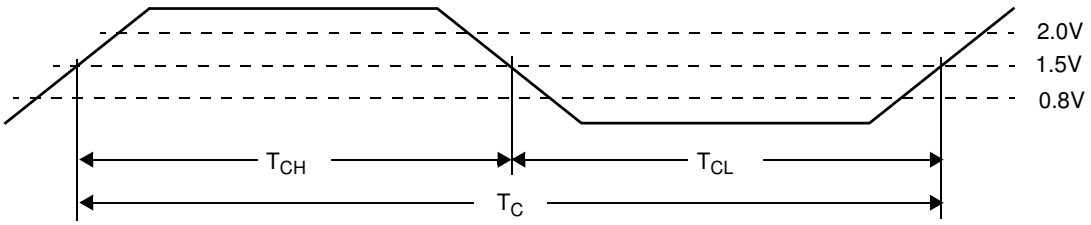
For PCI signals there are two different test load circuits, one for the rising edge and one the falling edge as shown in the figures at right.



Clocking Specifications

Symbol	Parameter	Min	Max	Units
CPU				
PF_C	Processor clock frequency		266.66/333.33/400	MHz
PT_C	Processor clock period	3.75/3/2.5		ns
SysClk Input				
SCF_C	Clock input frequency	25	66.66	MHz
SCT_C	Clock period	15	40	ns
SCT_{CS}	Clock edge stability (phase jitter, cycle to cycle)		± 0.15	ns
SCT_{CH}	Clock input high time	40% of nominal period	60% of nominal period	ns
SCT_{CL}	Clock input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate > 1 V/ns between 0.8 V and 2.0 V				
MemClkOut Output				
$MCOF_C$	Clock output frequency @ PF_C = 266 MHz		133.33	MHz
$MCOT_C$	Clock period @ PF_C = 266 MHz	7.5		ns
$MCOT_{CS}$	Clock edge stability (phase jitter, cycle to cycle)		± 0.2	ns
$MCOT_{CH}$	Clock output high time	45% of nominal period	55% of nominal period	ns
$MCOT_{CL}$	Clock output low time	45% of nominal period	55% of nominal period	ns
TrcClk Output				
TCF_C	Clock output frequency		PF_C / 2	MHz
TCT_C	Clock period		PT_C x 2	ns
TCT_{CS}	Clock edge stability (phase jitter, cycle to cycle)		± 0.2	ns
TCT_{CH}	Clock output high time	45% of nominal period	55% of nominal period	ns
TCT_{CL}	Clock output low time	45% of nominal period	55% of nominal period	ns
Other Clocks				
$VCOF_C$	VCO frequency	500	1000	MHz
$VCOF_C$	VCO frequency @ PF_C = 333 MHz or 400 MHz	500	1333	MHz
$PLBF_C$	PLB frequency		133.33	MHz
$OPBF_C$	OPB frequency		66.66	MHz

Clocking Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC405GPr. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC405GPr the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC405GPr with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC405GPr peripherals impose more stringent requirements (see Note 1).
- Use the peripheral bus clock (PerClk) for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClkOut since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates. If an external serial clock is used the baud rate is unaffected by the modulation.

2. Operation of the PPC405GPr PCI Bridge is unaffected by the use of a SSCG.

   For PCI frequencies of 33.33 MHz and below the PCI controller supports synchronous mode operation. This is accomplished by strapping the PPC405GPr for synchronous mode PCI and connecting the PCI bus clock to the PPC405GPr SysClk input. For 33.33 MHz signalling, the PCI specification has no limitation on the amount of frequency deviation or modulation that may be applied to the PCI clock. Therefore, the PPC405GPr SSCG requirements stated above take precedence.

   At PCI frequencies above 33.33 MHz, the PCI controller must be operated in asynchronous mode. When in asynchronous mode, the PCI bus clock must be driven into the PPC405GPr PCIClk input. In this configuration the PCI controller supports the 66.66 MHz PCI clock specification which specifies a maximum frequency deviation of -1% at a modulation of between 30 kHz and 33 kHz.

3. Ethernet operation is unaffected.

4. IIC operation is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the PPC405GPr meets the above requirements and does not adversely affect other aspects of the system.

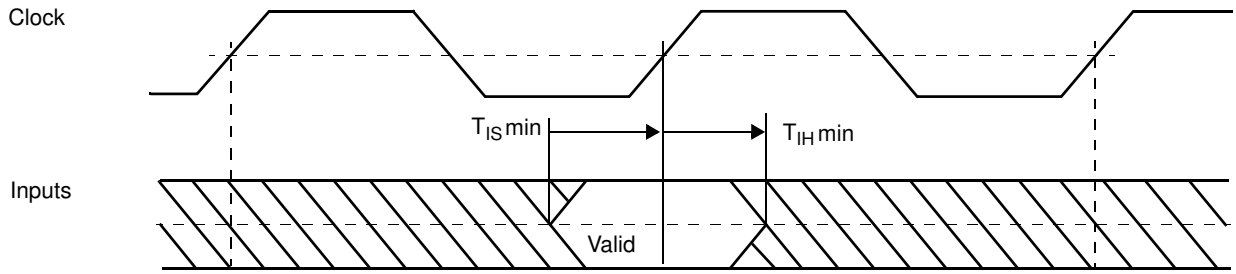
Peripheral Interface Clock Timings

Parameter	Min	Max	Units
PCIClk input frequency (asynchronous mode)	Note 1	66.66	MHz
PCIClk period (asynchronous mode)	15	Note 1	ns
PCI Clock frequency (synchronous mode)	25	33.33	MHz
PCI Clock period (synchronous mode - Note 2)	30	40	ns
PCIClk input high time	40% of nominal period	60% of nominal period	ns
PCIClk input low time	40% of nominal period	60% of nominal period	ns
EMCMDClk output frequency	–	2.5	MHz
EMCMDClk period	400	–	ns
EMCMDClk output high time	160	–	ns
EMCMDClk output low time	160	–	ns
PHYTxClk input frequency	2.5	25	MHz
PHYTxClk period	40	400	ns
PHYTxClk input high time	35% of nominal period	–	ns
PHYTxClk input low time	35% of nominal period	–	ns
PHYRxClk input frequency	2.5	25	MHz
PHYRxClk period	40	400	ns
PHYRxClk input high time	35% of nominal period	–	ns
PHYRxClk input low time	35% of nominal period	–	ns
PerClk output frequency	–	66.66	MHz
PerClk period	15	–	ns
PerClk output high time	45% of nominal period	55% of nominal period	ns
PerClk output low time	45% of nominal period	55% of nominal period	ns
PerClk clock edge stability (phase jitter, cycle to cycle)		± 0.3	ns
UARTSerClk input frequency (Note 3)	–	$1000/(2T_{OPB}+2ns)$	MHz
UARTSerClk period	$2T_{OPB}+2$	–	ns
UARTSerClk input high time	$T_{OPB}+1$	–	ns
UARTSerClk input low time	$T_{OPB}+1$	–	ns
TmrClk input frequency	–	66.66	MHz
TmrClk period	15	–	ns
TmrClk input high time	40% of nominal period	60% of nominal period	ns
TmrClk input low time	40% of nominal period	60% of nominal period	ns

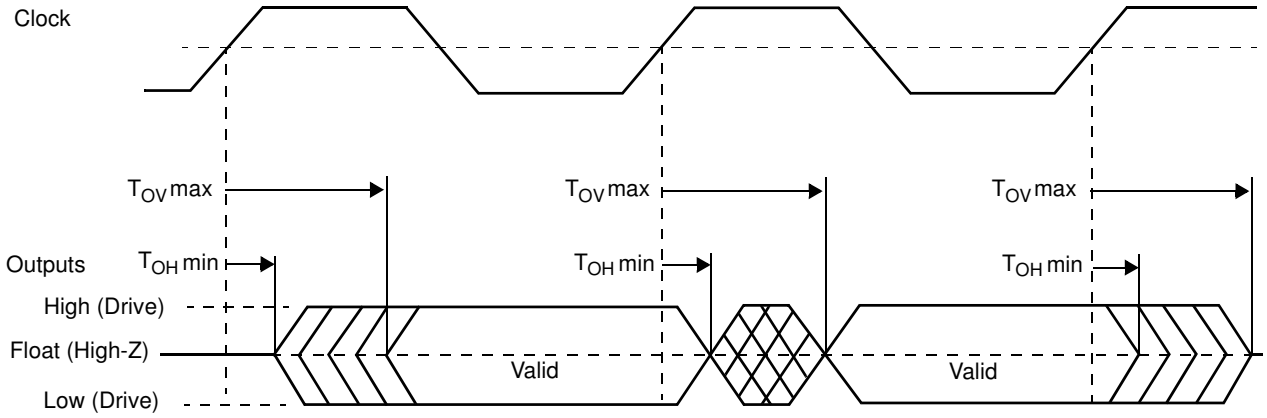
Note:

1. In asynchronous PCI mode the minimum PCIClk frequency is 1/8 the PLB Clock. Refer to the *PowerPC 405GPr Embedded Processor User's Manual* for more information.
2. In synchronous PCI mode the PCI clock is derived from SysClk and the PCIClk input pin is unused.
3. T_{OPB} is the period in ns of the OPB clock. The maximum OPB clock frequency is 66.66MHz.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



Notes: 1. In all of the following I/O Specifications tables a timing values of “na” means “not applicable” and “dc” means “don’t care.”
2. See “Test Conditions” on page 42 for output capacitive loading.

I/O Specifications—Group 1 (Sheet 1 of 3)

Notes:
1. PCI timings are for operation up to 66.66 MHz. PCI output hold time requirement is 1 ns for 66.66 MHz and 2 ns for 33.33 MHz. In synchronous mode, timing is relative to SysClk. In asynchronous mode, timing is relative to PCIClk.
2. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
3. For PCI, I/O H is specified at $0.9OV_{DD}$ and I/O L is specified at $0.1OV_{DD}$. For all other interfaces, I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (min)	I/O L (min)		
PCI Interface								
PCIAD31:0	3	0	6	1	0.5	1.5	PCI Clock	1
PCIC3:0[$\overline{\text{BE3:0}}$]	3	0	6	1	0.5	1.5	PCI Clock	1
PCIClk	dc	dc	na	na	na	na		async
$\overline{\text{PCIDevSel}}$	3	0	6	1	0.5	1.5	PCI Clock	1
$\overline{\text{PCIFrame}}$	3	0	6	1	0.5	1.5	PCI Clock	1
$\overline{\text{PCIGnt0}}$[$\overline{\text{Req}}$] $\overline{\text{PCIGnt1:5}}$	na	na	na	na	0.5	1.5	PCI Clock	1
PCIIDSel	3	0	6	1	na	na	PCI Clock	1
$\overline{\text{PCIINT}}$[PerWE]	na	na	dc	dc	0.5	1.5	PCI Clock	async
$\overline{\text{PCIIRDY}}$	3	0	6	1	0.5	1.5	PCI Clock	1
PCIParity	3	0	6	1	0.5	1.5	PCI Clock	1
$\overline{\text{PCIPErr}}$	3	0	6	1	0.5	1.5	PCI Clock	1
$\overline{\text{PCIReq0}}$[$\overline{\text{Gnt}}$] $\overline{\text{PCIReq1:5}}$	5	0	na	na	na	na	PCI Clock	1
$\overline{\text{PCIReset}}$	na	na	na	na	0.5	1.5	PCI Clock	
$\overline{\text{PCISErr}}$	na	na	na	na	0.5	1.5	PCI Clock	
$\overline{\text{PCIStop}}$	3	0	6	1	0.5	1.5	PCI Clock	1
$\overline{\text{PCITRDY}}$	3	0	6	1	0.5	1.5	PCI Clock	1
Ethernet Interface								
EMCMDClk	na	na	settable	2	10.3	7.1		2, async
EMCMDIO[PHYMDIO]	100	0	1 OPB clock period + 10ns	1 OPB clock period	10.3	7.1	EMCMDClk	2
EMCTxD3:0	na	na	20	2	10.3	7.1	PHYTX	2
EMCTxEn	na	na	20	2	10.3	7.1	PHYTX	2
EMCTxErr	na	na	20	2	10.3	7.1	PHYTX	2
PHYCol					10.3	7.1		2, async
PHYCrS					10.3	7.1		2, async
PHYRxClk					na	na		2, async
PHYRxD3:0	4	1	na	na	10.3	7.1	PHYRX	2
PHYRxDV	4	1	na	na	10.3	7.1	PHYRX	2
PHYRxErr	4	1	na	na	10.3	7.1	PHYRX	2
PHYTxClk					na	na		2, async

I/O Specifications—Group 1 (Sheet 2 of 3)

Notes:

1. PCI timings are for operation up to 66.66 MHz. PCI output hold time requirement is 1 ns for 66.66 MHz and 2 ns for 33.33 MHz. In synchronous mode, timing is relative to SysClk. In asynchronous mode, timing is relative to PCIClk.
2. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
3. For PCI, I/O H is specified at $0.9OV_{DD}$ and I/O L is specified at $0.1OV_{DD}$. For all other interfaces, I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (min)	I/O L (min)		
Internal Peripheral Interface								
IICSCL	na	na	na	na	15.3	10.2		
IICSDA	na	na	na	na	15.3	10.2		
$\overline{\text{UART0\_CTS}}$	na	na			10.3	7.1		
$\overline{\text{UART0\_DCD}}$	na	na			10.3	7.1		
$\overline{\text{UART0\_DSR}}$	na	na			10.3	7.1		
$\overline{\text{UART0\_DTR}}$					10.3	7.1		
$\overline{\text{UART0\_RI}}$	na	na			10.3	7.1		
$\overline{\text{UART0\_RTS}}$			na	na	10.3	7.1		
UART0_Rx	na	na			10.3	7.1		
UART0_Tx			na	na	10.3	7.1		
$\overline{\text{UART1\_RTS}}$/ $\overline{\text{UART1\_DTR}}$			na	na	10.3	7.1		
$\overline{\text{UART1\_DSR}}$/ $\overline{\text{UART1\_CTS}}$	na	na			na	na		
UART1_Rx	na	na			na	na		
UART1_Tx			na	na	10.3	7.1		
UARTSerClk	na	na			na	na		
Interrupts Interface								
IRQ0:6[GPIO17:23]					10.3	7.1		
JTAG Interface								
TCK					na	na		async
TDI					na	na		async
TDO					10.3	7.1		async
TMS					na	na		async
$\overline{\text{TRST}}$					na	na		async
System Interface								
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO24					10.3	7.1		
$\overline{\text{Halt}}$	dc	dc	na	na	na	na		async
SysClk			na	na	na	na		
SysErr			na	na	10.3	7.1		async
$\overline{\text{SysReset}}$			10	1	10.3	7.1		async
TestEn	dc	dc	na	na	na	na		async
TmrClk	dc	dc	na	na	na	na		async

I/O Specifications—Group 1 (Sheet 3 of 3)

Notes:

1. PCI timings are for operation up to 66.66 MHz. PCI output hold time requirement is 1 ns for 66.66 MHz and 2 ns for 33.33 MHz. In synchronous mode, timing is relative to SysClk. In asynchronous mode, timing is relative to PCIClk.
2. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
3. For PCI, I/O H is specified at $0.9OV_{DD}$ and I/O L is specified at $0.1OV_{DD}$. For all other interfaces, I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (min)	I/O L (min)		
Trace								
[TS1E] [TS2E] [TS1O] [TS2O] [TS3] [TS4] [TS5] [TS6]	na	na	$PT_C/2+0.7$	$PT_C/2-0.5$	10.3	7.1	TrcClk	10 pF load on clk/data

I/O Specifications—Group 2

Notes:

1. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM.
2. SDRAM I/O timings are specified relative to a MemClkOut terminated into a lumped 10pF load.
3. SDRAM interface hold times are guaranteed at the PPC405GPr package pin. System designers must use the PPC405GPr IBIS model (available from **www.amcc.com**) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
4. PerClk timing is specified with a 10pF load at the package pin. The indicated timing is valid only if PerClk feedback is selected. Refer to the *PowerPC 405GPr Embedded Processor User's Manual* for more information.
5. Input timings are specified at 1.5V, assuming transition times between 1 and 2ns, when measured between the 10% and 90% points of the output voltage.
6. I/O H is specified at 2.4 V and I/O L is specified at 0.4 V.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
SDRAM Interface								
BA1:0	na	na	4.5	1.6	15.3	10.2	MemClkOut	1, 2, 5
$\overline{\text{BankSel3:0}}$	na	na	4.5	1.5	15.3	10.2	MemClkOut	2, 5
$\overline{\text{CAS}}$	na	na	4.4	1.5	15.3	10.2	MemClkOut	1, 2, 5
ClkEn0:1	na	na	3.9	1.4	23	19.3	MemClkOut	2, 5
DQM0:3	na	na	4.5	1.4	15.3	10.2	MemClkOut	2, 5
DQMCB	na	na	4.3	1.4	15.3	10.2	MemClkOut	2, 5
ECC0:7	1.4	0	4.5	1.5	15.3	10.2	MemClkOut	2, 5
MemAddr12:0	na	na	4.6	1.5	15.3	10.2	MemClkOut	1, 2, 5
MemData0:31	1.4	0	5.1	1.4	15.3	10.2	MemClkOut	2, 5
$\overline{\text{RAS}}$	na	na	4.4	1.5	15.3	10.2	MemClkOut	1, 2, 5
$\overline{\text{WE}}$	na	na	4.4	1.5	15.3	10.2	MemClkOut	1, 2, 5
External Slave Peripheral Interface								
DMAAck0:3	na	na	6.1	2.2	10.3	7.1	PerClk	5
DMAReq0:3	3.2	0	na	na	na	na	PerClk	5
EOT0:3/TC0:3	dc	dc	6.4	2	10.3	7.1	PerClk	5
PerAddr0:31	2.2	0	7.1	2	15.3	10.2	PerClk	5
$\overline{\text{PerBLast}}$	3.3	0	6.5	2.3	10.3	7.1	PerClk	5
$\overline{\text{PerCS0}}$ $\overline{\text{PerCS1:7}}$[GPIO10:16]	na	na	6.5	2.1	10.3	7.1	PerClk	5
PerData0:31	4.7	0.9	7.2	1.9	15.3	10.2	PerClk	5
$\overline{\text{PerOE}}$	na	na	6.5	2.1	10.3	7.1	PerClk	5
PerPar0:3	2.3	0	7.2	2.1	15.3	10.2	PerClk	5
PerR/$\overline{\text{W}}$	3.3	0	6.6	2.1	10.3	7.1	PerClk	5
PerReady	5.5	0	na	na	na	na	PerClk	5
$\overline{\text{PerWBE0:3}}$	2.3	0	6.1	2.2	10.3	7.1	PerClk	5
External Master Peripheral Interface								
BusReq	na	na	6.1	2.2	10.3	7.1	PerClk	5
$\overline{\text{ExtAck}}$	na	na	5.9	2.1	10.3	7.1	PerClk	5
$\overline{\text{ExtReq}}$	4.1	0	na	na	na	na	PerClk	5
$\overline{\text{ExtReset}}$	na	na	6	1	15.3	10.2	PerClk	5
HoldAck	na	na	6.1	2	10.3	7.1	PerClk	5
HoldPri	2.1	0	na	na	na	na	PerClk	5
HoldReq	3.1	0	na	na	na	na	PerClk	5
PerClk	na	na	0.7	-0.5	15.3	10.2	SysClk	4, 5
PerErr	2.4	0	na	na	na	na	PerClk	5

Strapping

When the SysReset input is driven low by an external device (system reset), the state of certain I/O pins is read to enable default initial conditions prior to PPC405GPr start-up. The actual capture instant is the nearest SysClk edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. The recommended pull-up is 3kΩ to +3.3V or 10kΩ to +5V. The recommended pull-down is 1KΩ to GND. These pins are use for strap functions only during reset. They are used for other signals during normal operation. The following tables list the strapping pins along with their functions and strapping options. The signal names assigned to the pins for normal operation follow the pin number.

The PPC405GPr can be used as a replacement for the PPC405GP. When the PPC405GPr is used for this purpose, it should be strapped to operate in the PPC405GPr Legacy Mode. This option is selected by strapping ball D20 (GPIO24) low (0). If Legacy Mode is selected, the "PPC405GPr Legacy Mode Strapping Pin Assignments" table should be used to determine the strapping options. To operate the chip as a PPC405GPr, strap D20 (GPIO24) high (1) and use "PPC405GPr New Mode Strapping Pin Assignments" on page 53 to determine the strapping options.

PPC405GPr Legacy Mode Strapping Pin Assignments (Sheet 1 of 2)

Function	Option	Ball Strapping		
PLL Tuning [1] for $6 \le M \le 7$ use choice 3 for $7 < M \le 12$ use choice 5 for $12 < M \le 32$ use choice 6		**AF3** UART0_Tx	**AF2** $\overline{\text{UART0\_DTR}}$	**AD16** $\overline{\text{UART0\_RTS}}$
	Choice 1; TUNE[9:0] = 1010111100	0	0	0
	Choice 2; TUNE[9:0] = 0100111000	0	0	1
	Choice 3; TUNE[9:0] = 0100110110	0	1	0
	Choice 4; TUNE[9:0] = 0100111100	0	1	1
	Choice 5; TUNE[9:0] = 0100111000	1	0	0
	Choice 6; TUNE[9:0] = 1000111100	1	0	1
	Choice 7; TUNE[9:0] = 1000111110	1	1	0
	Choice 8; TUNE[9:0] = 1011111110	1	1	1
PLL Forward Divider [2]		**D16** DMAAck0	**B15** DMAAck1	
	Bypass mode	0	0	
	Divide by 3	0	1	
	Divide by 4	1	0	
	Divide by 6	1	1	
PLL Feedback Divider [2]		**B14** DMAAck2	**C12** DMAAck3	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
PLB Divider from CPU [2]		**P25** EMCTxD3	**L24** EMCTxD2	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	

PPC405GPr Legacy Mode Strapping Pin Assignments (Sheet 2 of 2)

Function	Option	Ball Strapping		
OPB Divider from PLB [2]		**L25** EMCTxD1	**J26** EMCTxD0	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
PCI Divider from PLB [2, 3]		**D18** GPIO1[TS1E]	**C20** GPIO2[TS2E]	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
External Bus Divider from PLB [2]		**K25** EMCTxErr	**K23** EMCTxEn	
	Divide by 2	0	0	
	Divide by 3	0	1	
	Divide by 4	1	0	
	Divide by 5	1	1	
ROM Width		**AC2** UART1_Tx	**AD2** $\overline{\text{UART1\_RTS}}$/ $\overline{\text{UART1\_DTR}}$	
	8-bit ROM	0	0	
	16-bit ROM	0	1	
	32-bit ROM	1	0	
	Reserved	1	1	
ROM Location		**U2** HoldAck		
	PPC405GPr Peripheral Attach	0		
	PPC405GPr PCI Attach	1		
PCI Asynchronous Mode Enable		**Y3** $\overline{\text{ExtAck}}$		
	Synchronous PCI Mode	0		
	Asynchronous Mode	1		
PCI Arbiter Enable [3]		**AF18** GPIO4[TS2O]		
	Internal Arbiter Disabled	0		
	Internal Arbiter Enabled	1		

Note:

1. The tune bits adjust parameters that control PLL jitter. The recommended values minimize jitter for the PLL implemented in the PPC405GPr. These bits are shown for information only; and do not require modification except in special clocking circumstances such as spread spectrum clocking. For details on the use of Spread Spectrum Clock Generators (SSCGs) with the PPC405GPr, visit the technical documents area of the AMCC PowerPC web site.
2. Not all combinations of dividers produce valid operating configurations. Frequencies must be within the limits specified in “Clocking Specifications” on page 43. Further requirements are detailed in the Clocking chapter of the *PowerPC 405GPr Embedded Processor User’s Manual*.
3. Additional consideration must be given to pins that normally function as Trace signals. Improved design margin can be gained by using three-state buffers instead of strapping resistors, and minimizing trace lengths and stubs.

PPC405GPr New Mode Strapping Pin Assignments (Sheet 1 of 3)

Function	Option	Ball Strapping			
PLL Tuning See the *PowerPC 405GPr Embedded Processor User's Manual* for details.		**AF3** UART0_Tx	**AF2** UART0_DTR	**AD16** UART0_RTS	
	Choice 1; TUNE[9:0] = 1010111100	0	0	0	
	Choice 2; TUNE[9:0] = 0100111000	0	0	1	
	Choice 3; TUNE[9:0] = 0100110110	0	1	0	
	Choice 4; TUNE[9:0] = 0100111100	0	1	1	
	Choice 5; TUNE[9:0] = 0100111000	1	0	0	
	Choice 6; TUNE[9:0] = 1000111100	1	0	1	
	Choice 7; TUNE[9:0] = 1000111110	1	1	0	
	Choice 8; TUNE[9:0] = 1011111110	1	1	1	
PLL Forward Divider A [2]		**D16** DMAAck0	**B15** DMAAck1	**AC9** GPIO5[TS3]	
	Divide by 8	0	0	0	
	Divide by 7	0	0	1	
	Divide by 6	0	1	0	
	Divide by 5	0	1	1	
	Divide by 4	1	0	0	
	Divide by 3	1	0	1	
	Divide by 2	1	1	0	
	Divide by 1	1	1	1	
PLL Forward Divider B [2]		**P25** EMCTxD3	**L24** EMCTxD2	**AE8** GPIO6[TS4]	
	Divide by 8	0	0	0	
	Divide by 7	0	0	1	
	Divide by 6	0	1	0	
	Divide by 5	0	1	1	
	Divide by 4	1	0	0	
	Divide by 3	1	0	1	
	Divide by 2	1	1	0	
	Divide by 1	1	1	1	

PPC405GPr New Mode Strapping Pin Assignments (Sheet 2 of 3)

Function	Option	Ball Strapping			
PLL Feedback Divider [2, 3]		**B14** DMAAck2	**C12** DMAAck3	**AF5** GPIO7[TS5]	**AC7** GPIO8[TS6]
	Divide by 16	0	0	0	0
	Divide by 1	0	0	0	1
	Divide by 2	0	0	1	0
	Divide by 3	0	0	1	1
	Divide by 4	0	1	0	0
	Divide by 5	0	1	0	1
	Divide by 6	0	1	1	0
	Divide by 7	0	1	1	1
	Divide by 8	1	0	0	0
	Divide by 9	1	0	0	1
	Divide by 10	1	0	1	0
	Divide by 11	1	0	1	1
	Divide by 12	1	1	0	0
	Divide by 13	1	1	0	1
	Divide by 14	1	1	1	0
	Divide by 15	1	1	1	1
OPB Divider from PLB [2]		**L25** EMCTxD1	**J26** EMCTxD0		
	Divide by 1	0	0		
	Divide by 2	0	1		
	Divide by 3	1	0		
	Divide by 4	1	1		
PCI Divider from PLB [2, 3]		**D18** GPIO1[TS1E]	**C20** GPIO2[TS2E]		
	Divide by 1	0	0		
	Divide by 2	0	1		
	Divide by 3	1	0		
	Divide by 4	1	1		
External Bus Divider from PLB [2]		**K25** EMCTxErr	**K23** EMCTxEn		
	Divide by 2	0	0		
	Divide by 3	0	1		
	Divide by 4	1	0		
	Divide by 5	1	1		
ROM Width		**AC2** UART1_Tx	**AD2** $\overline{\text{UART1\_RTS}}$/ $\overline{\text{UART1\_DTR}}$		
	8-bit ROM	0	0		
	16-bit ROM	0	1		
	32-bit ROM	1	0		
	Reserved	1	1		
ROM Location		**U2** HoldAck			
	PPC405GPr Peripheral Attach	0			
	PPC405GPr PCI Attach	1			

PPC405GPr New Mode Strapping Pin Assignments (Sheet 3 of 3)

Function	Option	Ball Strapping
PCI Asynchronous Mode Enable		**Y3** ExtAck
	Synchronous PCI Mode	0
	Asynchronous Mode	1
External Bus Synchronous Mode Enable [3]		**A22** GPIO3[TS1O]
	Asynchronous Mode	0
	Synchronous Mode	1
PCI Arbiter Enable [3]		**AF18** GPIO4[TS2O]
	Internal Arbiter Disabled	0
	Internal Arbiter Enabled	1
New Mode Enable In Legacy mode the PPC405GPr functions like the PPC405GP. If not strapped, the PPC405GPr defaults to Legacy mode.		**D20** GPIO24
	Legacy (PPC405GP) mode	0
	New (PPC405GPr) mode[4]	1
Flip Circuit Disable (must be strapped low (0) during initilization).		**AB3** GPIO9[TrcClk]
	Normal operation	0

Note:

1. The tune bits adjust parameters that control PLL jitter. The recommended values minimize jitter for the PLL implemented in the PPC405GPr. These bits are shown for information only; and do not require modification except in special clocking circumstances such as spread spectrum clocking. For details on the use of Spread Spectrum Clock Generators (SSCGs) with the PPC405GPr, visit the technical documents area of the AMCC PowerPC web site.
2. Not all combinations of dividers produce valid operating configurations. Frequencies must be within the limits specified in "Clocking Specifications" on page 43. Further requirements are detailed in the Clocking chapter of the *PowerPC 405GPr Embedded Processor User's Manual*.
3. Additional consideration must be given to pins that normally function as Trace signals. Improved design margin can be gained by using three-state buffers instead of strapping resistors, and minimizing trace lengths and stubs.
4. The pull-up initialization strapping resistor must be 1kΩ rather than 3kΩ in order to overcome the internal pull-down resistor.

Revision Log

Date	Contents of Modification
03/13/2003	400MHz part numbers and new power/current numbers
08/28/2003	Add new V_{DD} values for 400MHz parts.
11/22/2004	Correct package drawings and add lead-free part numbers. Add +105°C temperature specification. Add 1 ms. voltage ramp-up restriction.
12/02/2004	Update to AMCC format.
01/06/2005	Correct typographical error in 27mm package drawing.
08/29/2005	Add dashes back into PNs.
03/13/2007	Revise package drawings to add logo view. Update AMCC address and copyright date on last page.
09/07/2007	Change TestEn signal from active low to active high. Correct AMCC telephone numbers.

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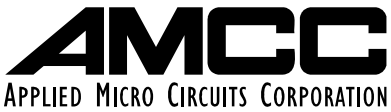

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