Military 54ALS138

1-of-8 Decoder

ELECTRICALLY TESTED PER:
MPG54ALS138

The 54ALS138 is a high-speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allows parallel expansion to a 1-of-24 decoder using just three ALS138 devices or to a 1-of-32 decoder using four ALS138's and one inverter. The ALS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Typical Power Dissipation of 32 mW
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effect

AVAILABLE AS:

1) JAN: N/A
2) SMD: N/A
3) 883C: 54ALS138/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

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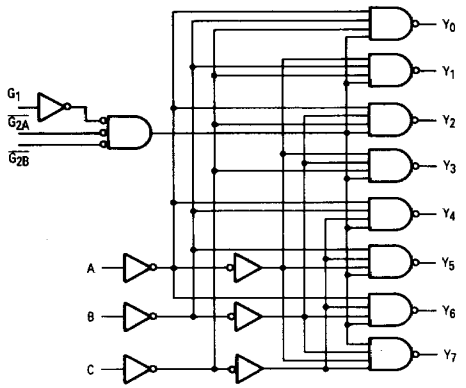
LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
A	1	1	2	V_{CC}
B	2	2	3	V_{CC}
C	3	3	4	V_{CC}
G_{2A}	4	4	5	V_{CC}
G_{2B}	5	5	7	V_{CC}
G_1	6	6	8	V_{CC}
Y_7	7	7	9	OPEN
GND	8	8	10	GND
Y_6	9	9	12	OPEN
Y_5	10	10	13	OPEN
Y_4	11	11	14	OPEN
Y_3	12	12	15	OPEN
Y_2	13	13	17	OPEN
Y_1	14	14	18	OPEN
Y_0	15	15	19	OPEN
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs						Outputs							
$\overline{G}_{2A}$	$\overline{G}_{2B}$	G_1	A	B	C	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Don't Care

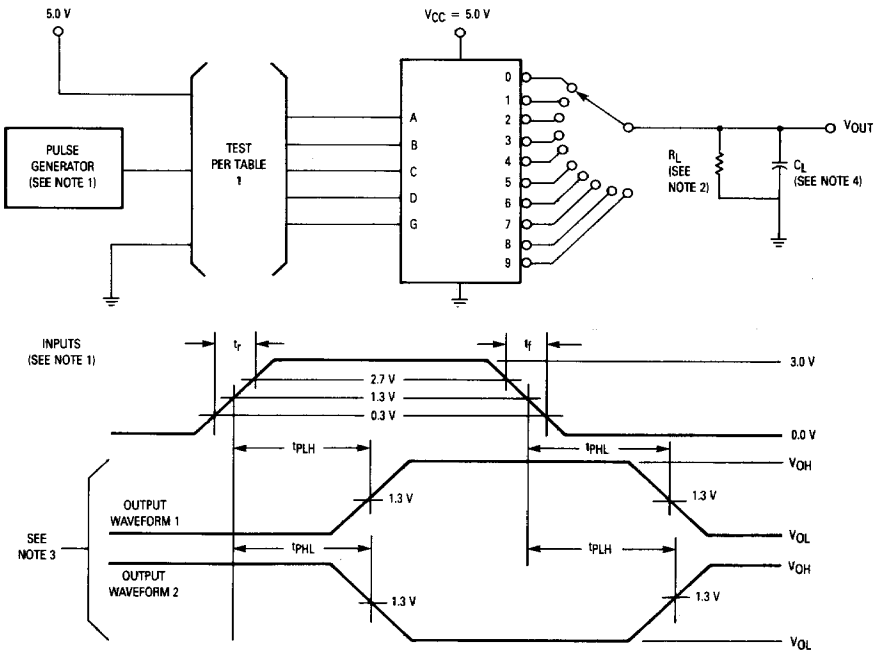
PIN NAMES	
A, B, C	Address Inputs
$\overline{G}_{2A,B}$	Enable (Active LOW) Input
G_1	Enable (Active HIGH) Inputs
$\overline{Y}_0$, $\overline{Y}_3$	Active Low Outputs

FUNCTIONAL DESCRIPTION

The ALS138 is a high-speed dual 1-of-8 Decoder/ Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A, B, C) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{Y}_0$, $\overline{Y}_7$). The ALS138 features three Enable inputs, two active LOW ($\overline{G}_{2A}$, $\overline{G}_{2B}$) and one active HIGH (G_1). All outputs will be HIGH unless $\overline{G}_{2A}$ and $\overline{G}_{2B}$ are LOW and G_1 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four ALS138s and one inverter.

The ALS138 can be used as an 8-output demultiplexer by using one of the active LOW enable inputs as a data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TEST CIRCUIT AND WAVEFORM



NOTES:
1. V_{IN} = Input pulse has the following characteristics: PRR ≤ 1.0 MHz, $t_r = t_f$ = 6.0 ± 1.5 ns and $Z_{out} \approx 50\ \Omega$.
2. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance, without package in test fixture.
3. Input-output waveform combination in accordance with truth table.
4. R_L = 499 Ω ± 1.0%.
5. Voltage measurements are to be made with respect to network ground terminal.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logic "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, Ea = 2.0 V or GND, V_{IN} = 0.8 V.
V_{OL}	Logic "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IN} = 0.8 V or 2.0 V (all inputs), G_1 = 2.0 V, $G_{2A,B}$ = 0.8 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_O	Output Short Circuit Current	−30	−112	−30	−112	−30	−112	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V ($G_{2A,B}$), V_{OUT} = 2.25 V.
I_{IL}	Logical "0" Input Current	0	−100	0	−100	0	−100	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{CC}	Power Supply Current Off		10		10		10	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (G_1).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output A, B, or C to Yn	6.0	18	6.0	22	6.0	22	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output A, B, or C to Yn	6.0	20	6.0	25	6.0	25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output Gn to Yn	5.0	17	5.0	20	5.0	20	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output Gn to Yn	4.0	19	4.0	23	4.0	23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

NOTE:
1. Method 3011 shall be used, except the output voltage shall be as specified herein, and the output current shall be operating rather than short circuit current. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.