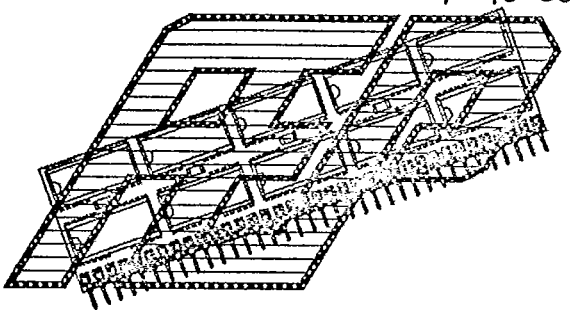
T-46-23-18



- *>> Four 1,048,576 x 5 Organization*
- *>> Module can be organized into three separate configurations:*
  - *I. 1M x 20*
  - *II. 2M x 10*
  - *III. 4M x 5*
- *>> 36 x 2 (72 pins) VDIP edge clip*
- *>> 0.100 inch distance between pins*
- *>> Single +5V power supply*
- *>> TTL compatible*

4 BY 1 MEGAWORD BY 5 BIT DYNAMIC RAM MODULE

DESCRIPTION:

The AEPDD4X1M5 is a 4 x 1 megaword x 5 bit dynamic random access memory module consisting of four 1M x 5 bit banks in a 72 pin double in-line memory module format. Physically it consists of an FR4 PC material substrate mounted with twenty 1M x 1 SOJ (small outline J-leaded package) DRAM ICs, ten 0.22 microfarad capacitors, and 36 x 2 (72 pins) VDIP edge clip I/O pins.

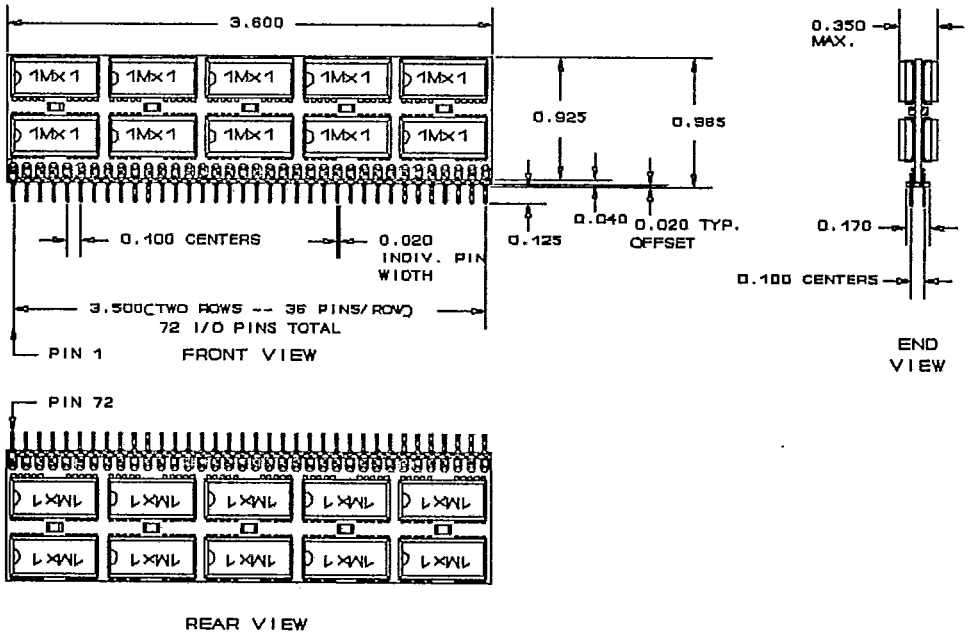
The module is activated by separate row, column and write enable strobes (RE\,CE\,WE\) on each four memory bank. Through proper interconnection of the RE\, CE\, WE\ and I/O pins at the mother board interface, the AEPDD4X1M5 can be organized into three separate memory capability, 1M x 20, 2M x 10 and 4M x 5 bits.

Power dissipation is also determined by the ICs used but is typically 50 milliwatts in standby and 2.5 to 3.5 watts when active (ratings for the CMOS version). A single 5V power supply is required.

Also available is the AEPDD4X4M5, it is a four banks of 4Mx5 DRAM module. By using the new 4Mx1 ICs, this module can be configured into three separate memory capability: 16M x 5 bit, 4M x 20 bit, and 8M x 10 bit.

SPECIFICATION DRAWING

DIMENSIONS IN INCHES, TOLERANCE: +/-0.010 UNLESS SPECIFIED.



4 x 1M x 5 DRAM DIMM

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PIN CONFIGURATION (TOP VIEW)

VCC	1	72	VCC
A10	2	71	NC
A8	3	70	A9
A6	4	69	A7
A4	5	68	A5
Q0	6	67	Q18
Q1	7	66	Q19
D0	8	65	D18
D1	9	64	D19
A2	10	63	A3
A0	11	62	A1
Q2	12	61	Q16
Q3	13	60	Q17
D2	14	59	D16
D3	15	58	D17
*WE1	16	57	WE3*
*WE2	17	56	WE4*
VCC	18	55	VSS
VSS	19	54	VCC
Q4	20	53	Q14
Q5	21	52	Q15
D4	22	51	D14
D5	23	50	D15
*CE1	24	49	CE3*
*CE2	25	48	CE4*
Q6	26	47	Q12
Q7	27	46	Q13
D6	28	45	D12
D7	29	44	D13
*RE1	30	43	RE3*
*RE2	31	42	RE4*
Q8	32	41	Q10
Q9	33	40	Q11
D8	34	39	D10
D9	35	38	D11
VSS	36	37	VCC

* ACTIVE WHEN LOW

FUNCTIONAL DIAGRAM