



CPU Frequency Generator

General Description

The **AV9107C-14** offers a tiny footprint solution for generating two simultaneous clocks. One clock, the REFCLK, is a fixed output frequency which is the same as the input reference crystal (or clock). The other clock, CLK1, can be either 51.84 or 41.472 MHz.

The device has advanced features which include on-chip loop filters, tristate outputs, and power-down capability. A mini-mum of external components - two decoupling capacitors and an optional ferrite bead - are all that are required for jitter-free operation.

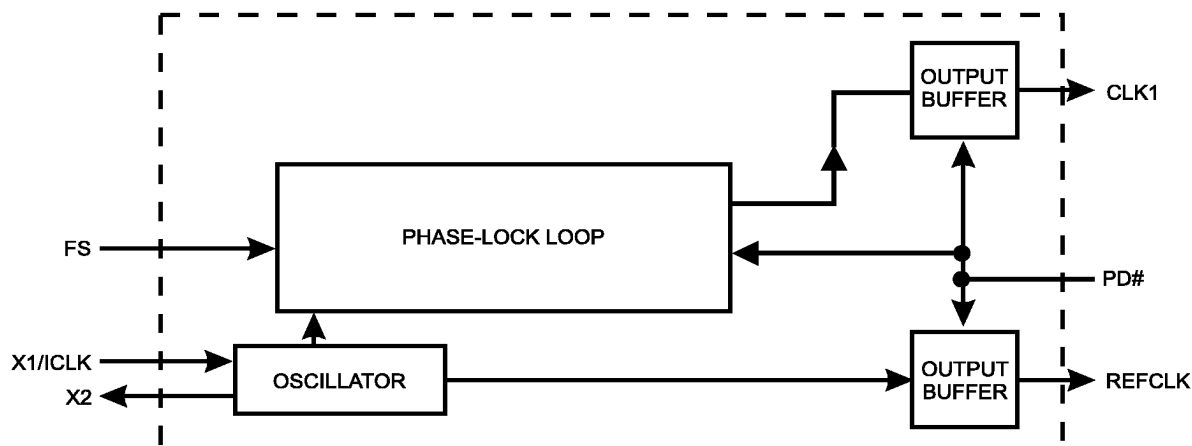
Features

- Patented on-chip Phase-Locked Loop with VCO for clock generation
- Provides reference clock and synthesized clock
- Generates frequencies of 18.432 and 51.84 or 41.472 MHz
- 8-pin DIP or SOIC package
- 18.432MHz input reference frequency
- On-chip loop filter
- Low power CMOS technology
- Single +3.3 or +5 volt power supply

Applications

Computer: The **AV9107C-14** is the ideal solution for replacing high speed oscillators and for reducing clock speeds to save power in computers. The device provides smooth, glitch-free frequency transitions so that the CPU can continue to operate during slow-down or speed-up.

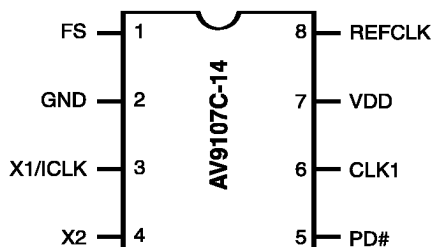
Block Diagram





AV9107C-14

Pin Configuration



8-Pin DIP, SOIC

Functionality

(at 18.432 MHz reference frequency input)

FS	CLK1
0	51.84 MHz
1	41.472 Mhz

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS0	IN	Frequency Select 0 for CLK1.
2	GDN	PWR	Digital Ground.
3	X1/CLK	IN	Crystal Output or Input Clock frequency. Typically 18.432 MHz system clock.
4	X2	OUT	Crystal Output (No Connect when INPUT clock used.).
5	PD#	IN	Powers down loop and causes all output to be forced to a logic low level.
6	CLK1	OUT	Clock 1 Output (see decoding tables).
7	VDD	PWR	Digital power supply (+5V DC).
8	REFCLK	OUT	Reference Clock output. Produces a buffered version of the input clock or crystal frequency (typically 18.432 Mhz).

Frequency Transitions

A key **AV9107C-14** feature is the ability to provide glitch-free frequency transitions between its output frequencies.

Output Enable

The Output Enable feature tristates the specified output clock pins. This places the selected output pin in a high impedance state to allow for system level diagnostic testing.



Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
 Operating temperature under bias. 0°C to +70°C
 Storage temperature -65°C to +150°C
 Voltage on I/O pins referenced to GND. GND -0.5V to VDD +0.5V
 Power dissipation 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5.0V

Operating VDD = +4.5V to +5.5V; TA = 0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V _{IL}		-	-	0.8	V
Input High Voltage	V _{IH}		2.0	-	-	V
Input Low Current	I _{IL}	V _{IN} =0V (Pull-up input)	-	6.0	16.0	μA
Input Low Current	I _{IL}	V _{IN} =0V (Input with no pull-up)	-2.0	-	2.0	μA
Input High Current	I _{IH}	V _{IN} =V _{DD}	-2.0	-	2.0	μA
Output Low Voltage, Note 1	V _{OL}	I _{OL} =10mA	-	0.15	0.40	V
Output High Voltage, Note 1	V _{OH}	I _{OH} =-30mA	2.4	3.25	-	V
Output Low Current, Note 1	I _{OL}	V _{OL} =0.8V	22.0	35.0	-	mA
Output High Current, Note 1	I _{OH}	V _{OH} =2.0V	-	-50.0	-35.0	mA
Supply Current	I _{DD}	Unload, 51.84 MHz	-	18.0	42.0	mA
Supply Current; Power-down	I _{DD} (PD# low)	Unload, Logic Inputs 000	-	-	20.0	μA
Pull-up Resistor, Note 1	R _{pu}		-	380.0	700.0	k ohms
AC Characteristics						
Rise Time 0.8 to 2.0V, Note 1	T _r	15pF load	-	0.60	1.40	ns
Fall Time 2.0 to 0.8V, Note 1	T _f	15pF load	-	0.40	1.00	ns
Rise Time 20% to 80%, Note 1	T _r	15pF load	-	2.0	3.5	ns
Fall Time 80% to 20%, Note 1	T _f	15pF load	-	1.0	2.5	ns
Duty Cycle, Note 1	D _t	15pF load @1.4V	45.0	50.0	55.0	%
Jitter, One Sigma, Note 1	T _{jis}	From 20 to 100 MHz	-	50.0	150.0	ps
Jitter, Absolute, Note 1	T _{jab}	From 20 to 100 MHz	-250.0	-	250.0	ps
Input Frequency, Note 1	F _i		11.0	18.432	19.0	MHz
Output Frequency	F _o		2.0	-	120.0	MHz
Power-up Time, Note 1	T _{pu}		-	7.58	18.0	ms
Transition Time, Note 1	T _{tr}	51.8 to 41.4 MHz	-	6.0	13.0	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



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Electrical Characteristics at 3.3V

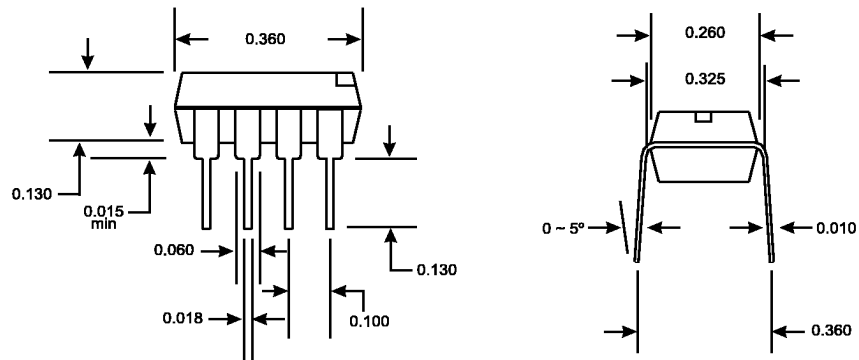
Operating $V_{DD} = +3.0V$ to $+3.7V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$ unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.20V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	$V_{IN}=0V$ (Pull-up input)	-	2.5	7.0	μA
Input Low Current	I_{IL}	$V_{IN}=0V$ (Input with no pull-up)	-2.0		2.0	μA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$	-2.0	-	2.0	μA
Output Low Voltage, Note 1	V_{OL}	$I_{OL}=6mA$	-	0.15	0.1	V
Output High Voltage, Note 1	V_{OH}	$I_{OH}=-5mA$	0.85	0.92	-	V
Output Low Current, Note 1	I_{OL}	$V_{OL}=0.2V_{DD}$	15.0	22.0	-	mA
Output High Current, Note 1	I_{OH}	$V_{OL}=0.7V_{DD}$	-	-17.0	-10.0	mA
Supply Current	I_{DD}	Unloaded, 50 MHz	-	22.0	40.0	mA
Supply Current; Power-down	I_{DD} (PD# low)	Unload, Logic Inputs 000	-	13.0	20.0	μA
Pull-up Resistor	R_{pu}		-	550.0	900.0	k ohms
AC Characteristics						
Rise Time 20% to 80%, Note 1	T_r	15pF load	-	2.2	3.5	ns
Fall Time 80% to 20%, Note 1	T_f	15pF load	-	1.2	2.5	ns
Duty Cycle, Note 1	D_1	15pF load @ 50%	40.0	46.0	53.0	%
Jitter, One Sigma, Note 1	T_{jis}	From 25 to 66 MHz	-	50.0	150.0	ps
Jitter, Absolute, Note 1	T_{jab}	From 25to 66 MHz	-250.0	-	250.0	ps
Input Frequency, Note 1	F_i		13.3	18.432	15.3	MHz
Output Frequency, Note 1	F_o		2.0	-	66.6	MHz
Power-up Time, Note 1	T_{pu}		-	7.58	18.0	ms
Transition Time, Note 1	T_{ft}	51.8 to 41.4 MHz	-	6.0	13.0	ms

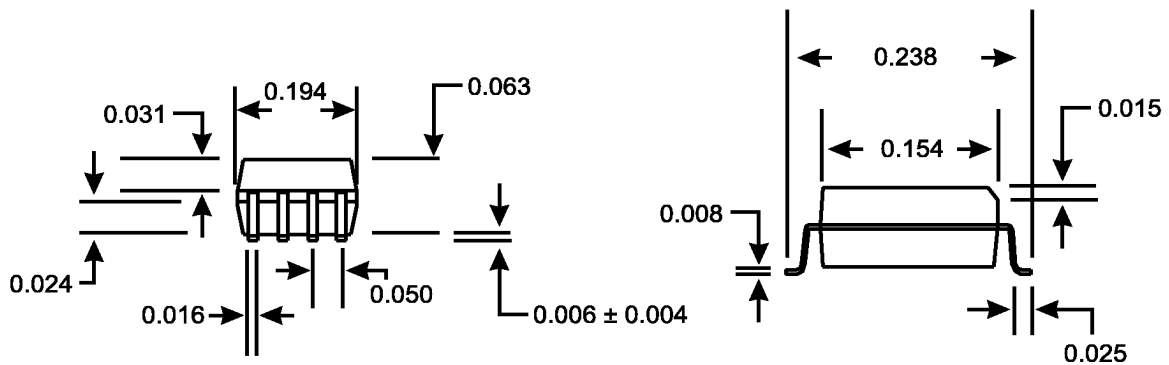
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



AV9107C-14



8-Pin DIP Package



8-Pin Plastic SOIC Package

Ordering Information

AV9107C-14CN08 or AV9107C-14CS08

Example:

XXX XXXX-PPP M X#W

Lead Count & Package Width

Lead Count=1, 2 or 3 digits

W=.3" SOIC or .6" DIP; None=Standard Width

Package Type

N=DIP (Plastic)

S=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns, if applicable)

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV=Standard