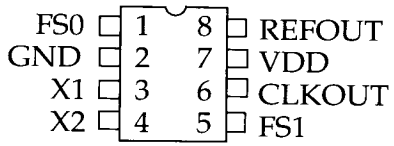
R4000 Frequency Generator

Features

- Ideally suited for R4000 family clock source
- Meets high and low time specifications
- Uses inexpensive 14.318 MHz reference crystal
- Selectable 50, 75 or 100 MHz output frequency
- Patented on-chip Phase Locked Loop with VCO for clock generation
- Power down frequency selection
- 8 pin DIP or SOIC package
- Low power CMOS technology
- +5 volt power supply

Pin Configuration



AV9140-01
8 pin DIP, SOIC

General Description

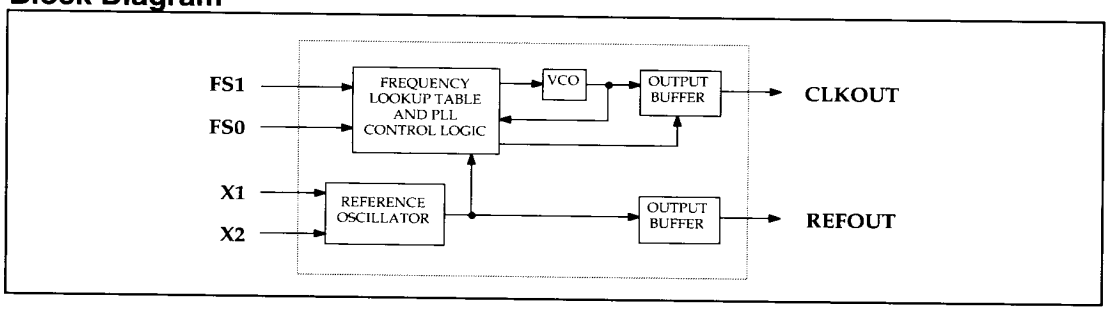
The AV9140 offers a small and inexpensive solution for generating an R4000 processor series master clock. It generates a selectable output frequency of 50, 75 or 100 MHz and generates an output waveform compatible with R4000 series master clock specifications. Output frequency is derived from a 14.318 MHz reference input clock using PLL techniques. The 14.318 reference clock can be either a discrete quartz crystal or a TTL clock signal.

The device includes an on-chip loop filter for the PLL circuit. Required external components include two decoupling capacitors and an optional ferrite bead for power supply conditioning, and two external load capacitors when a crystal reference is used. Custom masked versions, with customized frequencies and features, are available in 6-8 weeks for a small NRE.

Decoding Table for AV9140-01

Input Selection		Output Frequency	
FS1	FS0	Desired CLKOUT Frequency (MHz)	Actual CLKOUT Frequency (MHz)
0	0	OFF	OFF
0	1	50	50.113
1	0	75	74.959
1	1	100	100.227

Block Diagram



Pin Description

Pin Name	Pin #	Pin Type	Description
FS0	1	Input	FREQUENCY SELECT for CLKOUT
GND	2	-	GROUND
X1	3	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318MHz system clock
X2	4	Output	CRYSTAL OUTPUT
FS1	5	Input	FREQUENCY SELECT for CLKOUT
CLKOUT	6	Output	CLOCK OUTPUT
VDD	7	-	Power Supply (+5V DC)
REFOUT	8	Output	REFERENCE CLOCK 14.318 MHz OUTPUT

Input Reference

The reference frequency of 14.31818 MHz was chosen since this is a common system frequency. Quartz crystals cut to this frequency are readily available and inexpensve. When using the AV9140 with a quartz crystal, the crystal is connected between pins X1 and X2. Appropriate load capacitors are also connected from X1 to ground and from X2 to ground, depending on crystal requirements. The AV9140 has an input capacitance of approximately 2.5 pF to ground at both X1 and X2. Refer to the quartz crystal data sheet for total load capacitance requirements.

When driving the AV9140 with an external clock, X1 is used as the clock input and pin X2 is left unconnected.

Power Down

When "OFF" is selected by FS2 and FS3, the chip goes into a power down mode.

Frequency Accuracy

The AV9140 uses PLL (Phase-Lock-Loop) circuitry to establish the output frequency which is based on a fixed ratio of the input frequency. The actual frequencies shown in the AV9140-01 decoding table are for when 14.31818 MHz is used as a reference frequency. Any percent error of this reference frequency will result in the same percent error in the output frequency.

Absolute Maximum Ratings

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect the reliability of the device.

Electric Characteristics

(Operating V_{DD} = +4.5V to +5.5V, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-5	-	5	µA	V_{IN} = 0V
I_{IH}	Input High Current	-5	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	.2 VDD	V	
V_{OH}	Output High Voltage	.8 VDD	-	-	V	
I_{DD}	Supply Current	-	10	20	mA	Note 1
I_{DD}	Supply Current	-	15	30	mA	Note 2
C_i	Input Capacitance	-	-	10	pF	Except X1
$I_{DDSTDBY}$	Standby Supply Current	-	25	-	µA	"OFF" selected
AC Characteristics						
t_w	Enable pulse width	20	-	-	ns	
t_{su}	Setup time data to enable	20	-	-	ns	
f_o	Output Frequency	8		100	MHz	
f_i	Input Frequency	2	14.318	30	MHz	
$ICLK_r$	Input Clock Rise time	-	-	20	ns	(Recommended)
$ICLK_f$	Input Clock Fall time	-	-	20	ns	(Recommended)
t_{hd}	Hold time data to enable	10	-	-	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	15 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	1.5	3	ns	15 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	15 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	1.5	3	ns	15 pf load
d_t	Output Duty cycle	40	48/52	60	%	15 pf load, Note 3
t_{ol}	Output Low time @ 75 MHz	3	-	-	ns	15 pf load
t_{oh}	Output High time @ 75 MHz	3	-	-	ns	15 pf load
T_{jis}	Jitter, 1 sigma	-	60	150	ns	All frequencies
T_{jabs}	Jitter, absolute	-	±250	±450	ns	All frequencies
t_{ft}	Frequency Transition time	-	-	20	ms	From 50 to 100 MHz
t_{pu}	Power up time	-	15	30	ms	From off to 100MHz

Notes
1. AV9140 with no load, with 14.318 MHz crystal input, and CLK1 running at 75 MHz. Power supply current varies with frequency. Consult Avasem for actual current at different frequencies.
2. AV9140 with 15 pF load on CLKOUT and REFOUT, CLKOUT = 100 MHz.
3. Output Duty Cycle measures using threshold voltage of 1.4 volts.

Ordering Information

Part Number	Part Marking	Temperature Range	Package Type
AV9140-01CN8	AV9140-01	0°C to +70°C	8 lead Plastic DIP (300 mils)
AV9140-01CS8	AV40-1	0°C to +70°C	8 lead SOIC (150 mils)
AV9140-01CS8T&R	AV40-1	-----	8 SOIC Tape and Reel (1000/reel)