FAIRCHILD SEMICONDUCTOR™

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SCAN182245A
Non-Inverting Transceiver with 25Ω Series Resistor Outputs

General Description

The SCAN182245A is a high performance BiCMOS bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

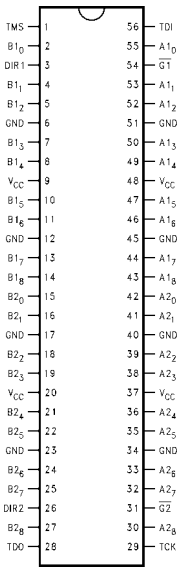
- High performance BiCMOS technology
- 25Ω series resistors in outputs eliminate the need for external terminating resistors
- Dual output enable control signals
- 3-STATE outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- IEEE 1149.1 (JTAG) Compliant
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT
- Power Up 3-STATE for hot insert
- Member of Fairchild's SCAN Products

Ordering Code:

Order Number	Package Number	Package Description
SCAN182245ASSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
SCAN182245AMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
$A1_{(0–8)}$	Side A1 Inputs or 3-STATE Outputs
$B1_{(0–8)}$	Side B1 Inputs or 3-STATE Outputs
$A2_{(0–8)}$	Side A2 Inputs or 3-STATE Outputs
$B2_{(0–8)}$	Side B2 Inputs or 3-STATE Outputs
$\overline{G1}$, $\overline{G2}$	Output Enable Pins (Active LOW)
DIR1, DIR2	Direction of Data Flow Pins

Truth Tables

Inputs		$A1_{(0-8)}$		$B1_{(0-8)}$
$\overline{G1}$ (Note 1)	DIR1			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

H = HIGH Voltage Level
L = LOW Voltage Level

Inputs		$A2_{(0-8)}$		$B2_{(0-8)}$
$\overline{G2}$ (Note 1)	DIR2			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

X = Immaterial
Z = High Impedance

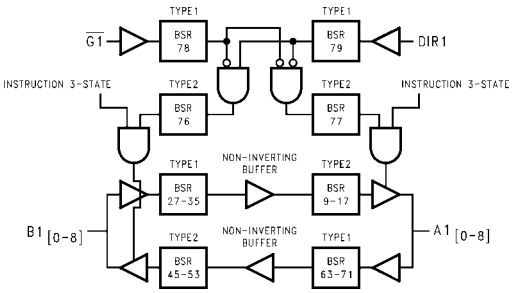
Note 1: Inactive-to-Active transition must occur to enable outputs upon power-up.

Functional Description

The SCAN182245A consists of two sets of nine non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B Ports to A Ports, when HIGH enables data from A Ports to B Ports. The Output Enable pins ($\overline{G1}$ and $\overline{G2}$) when HIGH disables both A and B Ports by placing them in a high impedance condition.

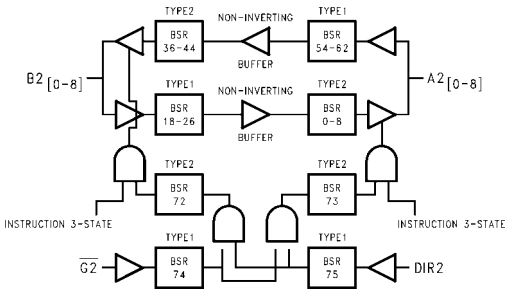
Block Diagrams

A1, B1, $\overline{G1}$ and DIR1



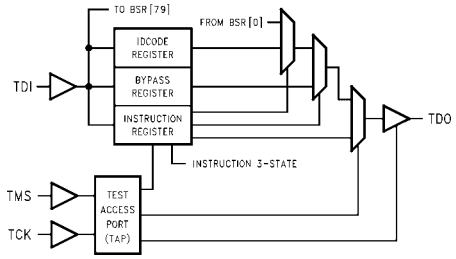
Note: BSR stands for Boundary Scan Register.

A2, B2, $\overline{G2}$ and DIR2



Note: BSR stands for Boundary Scan Register.

Tap Controller



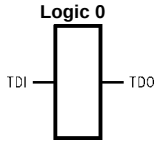
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data.

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0

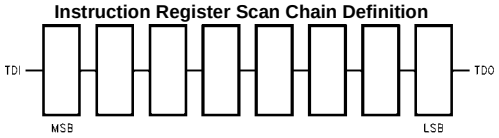


SCAN182245A Product IDCODE
(32-Bit Code per IEEE 1149.1)

Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
0000	111111	00000000	00000001111	1
MSB				**MSB**

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

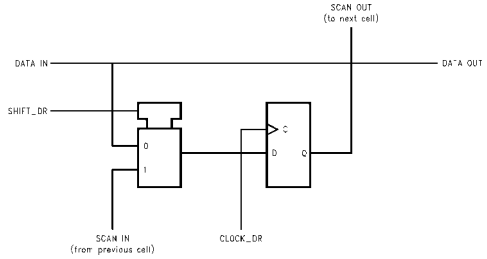
Instruction Register Scan Chain Definition



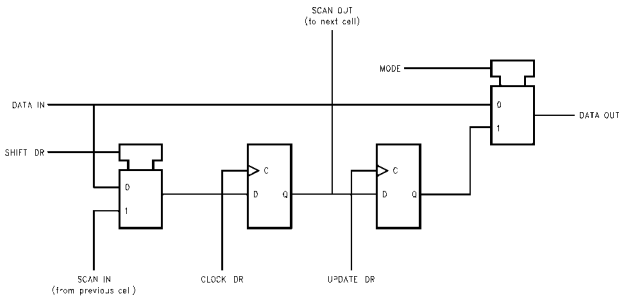
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

Scan Cell TYPE1

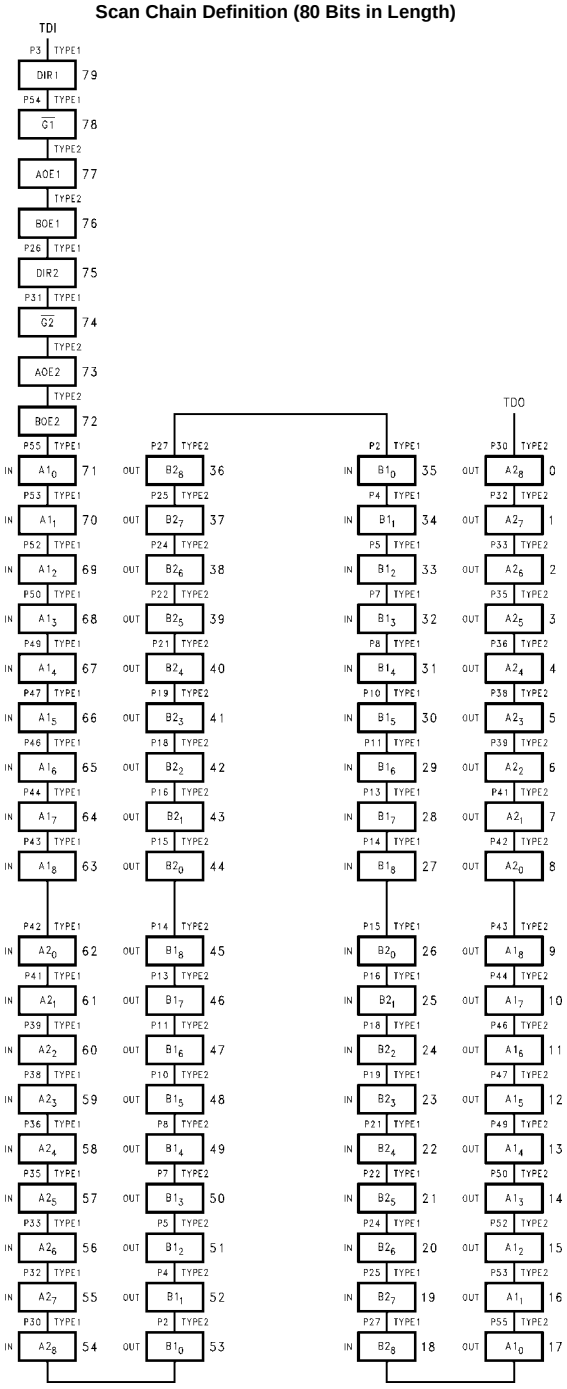


Scan Cell TYPE2



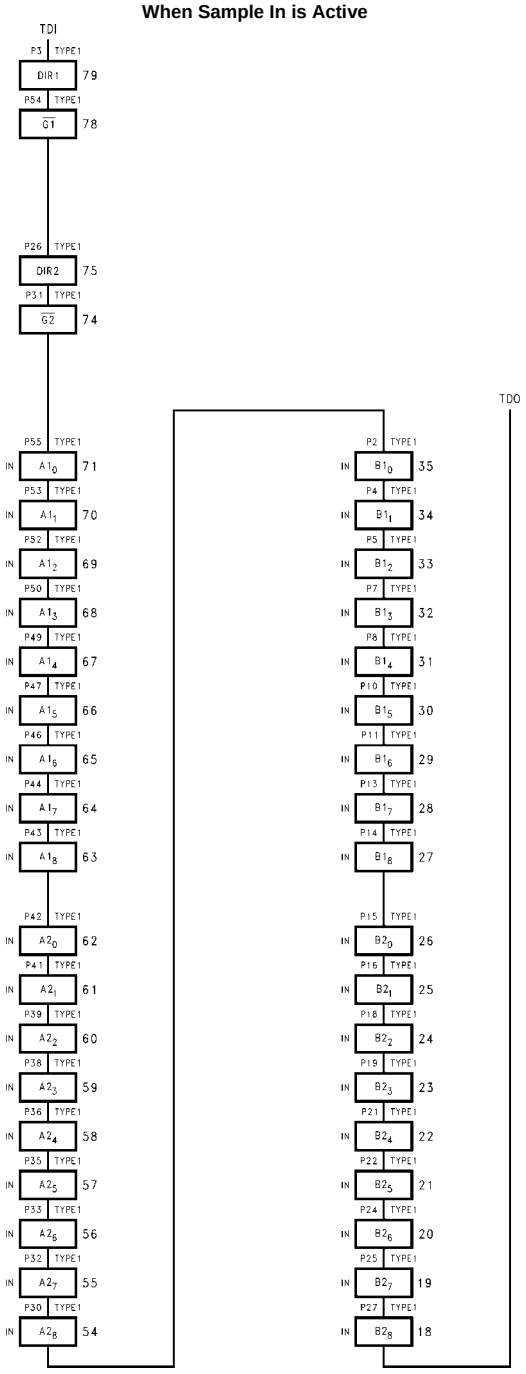
Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register
Scan Chain Definition (80 Bits in Length)



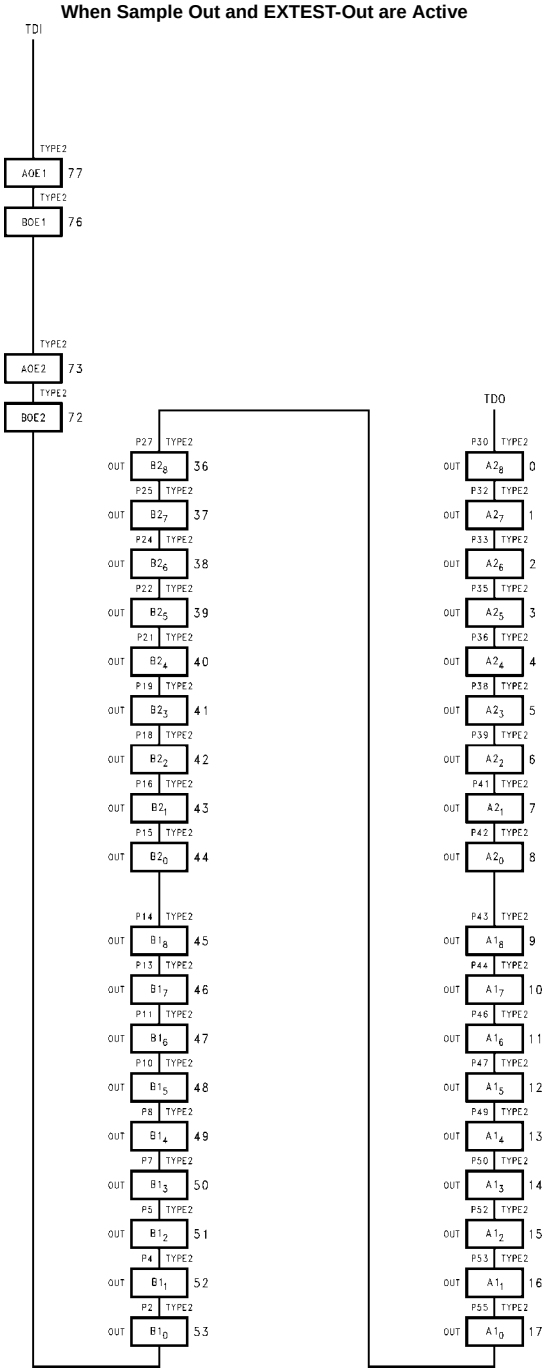
Description of BOUNDARY-SCAN Circuitry (Continued)

Input BOUNDARY-SCAN Register
Scan Chain Definition (40 Bits in Length)
When Sample In is Active



Description of BOUNDARY-SCAN Circuitry (Continued)

Output BOUNDARY-SCAN Register
Scan Chain Definition (40 Bits in Length)
When Sample Out and EXTEST-Out are Active



Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE_1		Internal	TYPE2	
76	BOE_1		Internal	TYPE2	Control
75	DIR2	26	Input	TYPE1	Signals
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE_2		Internal	TYPE2	
72	BOE_2		Internal	TYPE2	
71	$A1_0$	55	Input	TYPE1	
70	$A1_1$	53	Input	TYPE1	
69	$A1_2$	52	Input	TYPE1	
68	$A1_3$	50	Input	TYPE1	
67	$A1_4$	49	Input	TYPE1	A1–in
66	$A1_5$	47	Input	TYPE1	
65	$A1_6$	46	Input	TYPE1	
64	$A1_7$	44	Input	TYPE1	
63	$A1_8$	43	Input	TYPE1	
62	$A2_0$	42	Input	TYPE1	
61	$A2_1$	41	Input	TYPE1	
60	$A2_2$	39	Input	TYPE1	
59	$A2_3$	38	Input	TYPE1	
58	$A2_4$	36	Input	TYPE1	A2–in
57	$A2_5$	35	Input	TYPE1	
56	$A2_6$	33	Input	TYPE1	
55	$A2_7$	32	Input	TYPE1	
54	$A2_8$	30	Input	TYPE1	
53	$B1_0$	2	Output	TYPE2	
52	$B1_1$	4	Output	TYPE2	
51	$B1_2$	5	Output	TYPE2	
50	$B1_3$	7	Output	TYPE2	
49	$B1_4$	8	Output	TYPE2	B1–out
48	$B1_5$	10	Output	TYPE2	
47	$B1_6$	11	Output	TYPE2	
46	$B1_7$	13	Output	TYPE2	
45	$B1_8$	14	Output	TYPE2	
44	$B2_0$	15	Output	TYPE2	
43	$B2_1$	16	Output	TYPE2	
42	$B2_2$	18	Output	TYPE2	
41	$B2_3$	19	Output	TYPE2	
40	$B2_4$	21	Output	TYPE2	B2–out
39	$B2_5$	22	Output	TYPE2	
38	$B2_6$	24	Output	TYPE2	
37	$B2_7$	25	Output	TYPE2	
36	$B2_8$	27	Output	TYPE2	

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
35	$B1_0$	2	Input	TYPE1	
34	$B1_1$	4	Input	TYPE1	
33	$B1_2$	5	Input	TYPE1	
32	$B1_3$	7	Input	TYPE1	
31	$B1_4$	8	Input	TYPE1	B1–in
30	$B1_5$	10	Input	TYPE1	
29	$B1_6$	11	Input	TYPE1	
28	$B1_7$	13	Input	TYPE1	
27	$B1_8$	14	Input	TYPE1	
26	$B2_0$	15	Input	TYPE1	
25	$B2_1$	16	Input	TYPE1	
24	$B2_2$	18	Input	TYPE1	
23	$B2_3$	19	Input	TYPE1	
22	$B2_4$	21	Input	TYPE1	B2–in
21	$B2_5$	22	Input	TYPE1	
20	$B2_6$	24	Input	TYPE1	
19	$B2_7$	25	Input	TYPE1	
18	$B2_8$	27	Input	TYPE1	
17	$A1_0$	55	Output	TYPE2	
16	$A1_1$	53	Output	TYPE2	
15	$A1_2$	52	Output	TYPE2	
14	$A1_3$	50	Output	TYPE2	
13	$A1_4$	49	Output	TYPE2	A1–out
12	$A1_5$	47	Output	TYPE2	
11	$A1_6$	46	Output	TYPE2	
10	$A1_7$	44	Output	TYPE2	
9	$A1_8$	43	Output	TYPE2	
8	$A2_0$	42	Output	TYPE2	
7	$A2_1$	41	Output	TYPE2	
6	$A2_2$	39	Output	TYPE2	
5	$A2_3$	38	Output	TYPE2	
4	$A2_4$	36	Output	TYPE2	A2–out
3	$A2_5$	35	Output	TYPE2	
2	$A2_6$	33	Output	TYPE2	
1	$A2_7$	32	Output	TYPE2	
0	$A2_8$	30	Output	TYPE2	

SCAN ABT Live Insertion and Power Cycling Characteristics

SCAN ABT is intended to serve in Live Insertion backplane applications. It provides 2nd Level Isolation[1] which indicates that while external circuitry to control the output enable pin is unnecessary, there may be a need to implement differential length backplane connector pins for V_{CC} and GND. As well, pre-bias circuitry for backplane pins may be necessary to avoid capacitive loading effects during live insertion.

SCAN ABT provides control of output enable pins during power cycling via the circuit in Figure 1. It essentially controls the $\overline{G}_n$ pin until V_{CC} reaches a known level.

During *power-up*, when V_{CC} ramps through the 0.0V to 0.7V range, all internal device circuitry is inactive, leaving output and I/O pins of the device in high impedance. From approximately 0.8V to 1.8V V_{CC}, the Power-On-Reset circuitry, (POR), in Figure 1 becomes active and maintains device high impedance mode. The POR does this by providing a low from its output that resets the flip-flop The output, $\overline{Q}$, of the flip-flop then goes high and disables the NOR gate from an incidental low input on the $\overline{G}_n$ pin. After 1.8V V_{CC}, the POR circuitry becomes inactive and ceases to control the flip-flop. To bring the device out of high impedance, the $\overline{G}_n$ input must receive an inactive-to-active transition, a high-to-low transition on $\overline{G}_n$ in this case to change the state of the flip-flop. With a low on the $\overline{Q}$ output of the flip-flop, the NOR gate is free to allow propagation of a $\overline{G}_n$ signal.

During *power-down*, the Power-On-Reset circuitry will become active and reset the flip-flop at approximately 1.8V V_{CC}. Again, the $\overline{Q}$ output of the flip-flop returns to a high and disables the NOR gate from inputs from the $\overline{G}_n$ pin. The device will then remain in high impedance for the remaining ramp down from 1.8V to 0.0V V_{CC}.

Some suggestions to help the designer with live insertion issues:

- The $\overline{G}_n$ pin can float during power-up until the Power-On-Reset circuitry becomes inactive.
- The $\overline{G}_n$ pin can float on power-down only after the Power-On-Reset has become active.

The description of the functionality of the Power-On-Reset circuitry can best be described in the diagram of Figure 2.

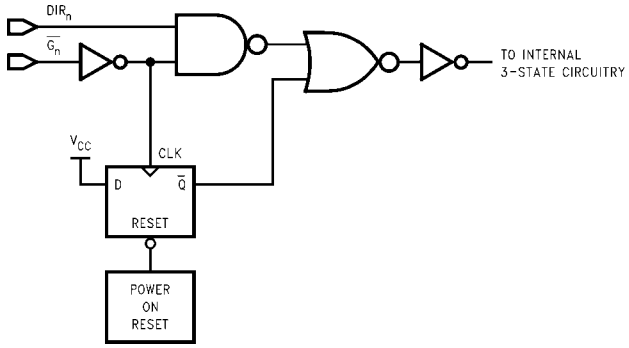
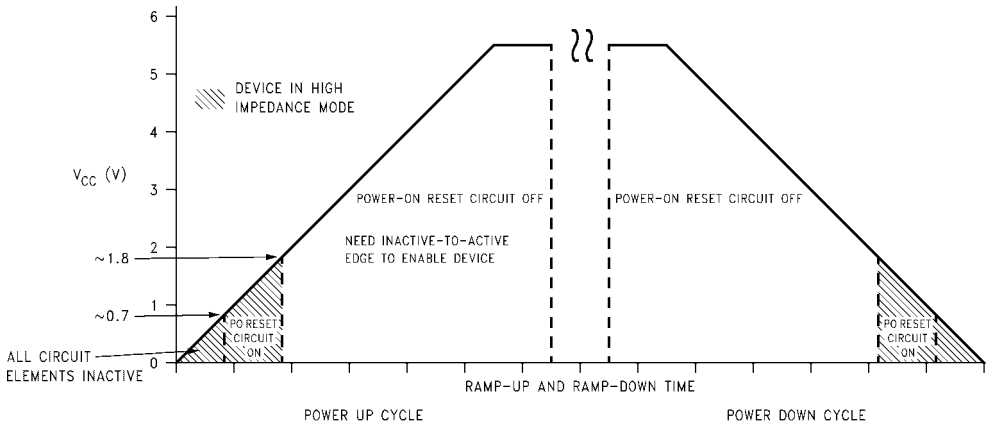


FIGURE 1.



[1]Section 7, "Design Consideration for Fault Tolerant Backplanes", Application Note AN-881.

SCAN ABT includes additional power-on reset circuitry not otherwise included in ABT devices.

FIGURE 2.

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V
ESD (HBM) Min.	2000V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage			2.0			V	Recognized HIGH Signal
V_{IL}	Input LOW Voltage					0.8	V	Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage		Min			−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		Min	2.5			V	I_{OH} = −3 mA
			Min	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage		Min			0.8	V	I_{OL} = 15 mA
I_{IH}	Input HIGH Current	All Others	Max			5	µA	V_{IN} = 2.7V (Note 4)
			Max			5	µA	V_{IN} = V_{CC}
		TMS, TDI	Max			5	µA	V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test		Max			7	µA	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)		Max			100	µA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	All Others	Max			−5	µA	V_{IN} = 0.5V (Note 4)
			Max			−5	µA	V_{IN} = 0.0V
		TMS, TDI	Max			−385	µA	V_{IN} = 0.0V
V_{ID}	Input Leakage Test		0.0	4.75			V	I_{ID} = 1.9 µA All Other Pins Grounded
$I_{IH} + I_{OZH}$	Output Leakage Current		Max			50	µA	V_{OUT} = 2.7V
$I_{IL} + I_{OZL}$	Output Leakage Current		Max			−50	µA	V_{OUT} = 0.5V
I_{OZH}	Output Leakage Current		Max			50	µA	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current		Max			−50	µA	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		Max	−100		−275	mA	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current		Max			50	µA	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test		0.0			100	µA	V_{OUT} = 5.5V, All Others GND
I_{CCH}	Power Supply Current		Max			250	µA	V_{OUT} = V_{CC}; TDI, TMS = V_{CC}
			Max			1.0	mA	V_{OUT} = V_{CC}; TDI, TMS = GND
I_{CCL}	Power Supply Current		Max				mA	V_{OUT} = LOW; TDI, TMS = V_{CC}
			Max			65.8	mA	V_{OUT} = LOW; TDI, TMS = GND
I_{CCZ}	Power Supply Current		Max			250	µA	TDI, TMS = V_{CC}
			Max			1.0	mA	TDI, TMS = GND
I_{CCT}	Additional I_{CC}/Input							
		All Other Inputs	Max			2.9	mA	V_{IN} = V_{CC} − 2.1V
		TDI, TMS inputs	Max			3	mA	V_{IN} = V_{CC} − 2.1V
I_{CCD}	Dynamic I_{CC}	No Load	Max			0.2	mA/ MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

Note 4: Guaranteed not tested.

AC Electrical Characteristics

Normal Operation:

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units
			Min	Typ	Max	
t_{PLH}	Propagation Delay	5.0	1.0	3.1	5.2	ns
t_{PHL}	A to B, B to A		1.5	4.4	6.5	
t_{PLZ}	Disable Time	5.0	1.5	4.8	8.6	ns
t_{PHZ}			1.5	5.2	8.9	
t_{PZL}	Enable Time	5.0	1.5	5.5	9.1	ns
t_{PZH}			1.5	4.6	8.2	

Note 5: Voltage Range 5.0V ± 0.5V

AC Electrical Characteristics

Scan Test Operation

Symbol	Parameter	V_{CC} (V) (Note 6)	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units
			Min	Typ	Max	
t_{PLH}	Propagation Delay	5.0	2.9	6.1	10.2	ns
t_{PHL}	TCK to TDO		4.2	7.7	12.1	
t_{PLZ}	Disable Time	5.0	2.1	5.9	10.7	ns
t_{PHZ}	TCK to TDO		3.3	7.4	12.5	
t_{PZL}	Enable Time	5.0	4.6	8.7	13.7	ns
t_{PZH}	TCK to TDO		2.8	6.8	11.5	
t_{PLH}	Propagation Delay	5.0	2.8	6.3	10.7	ns
t_{PHL}	TCK to Data Out during Update-DR State		4.5	8.2	13.0	
t_{PLH}	Propagation Delay	5.0	3.3	7.2	12.2	ns
t_{PHL}	TCK to Data Out during Update-IR State		5.0	9.3	14.8	
t_{PLH}	Propagation Delay	5.0	3.7	8.4	14.0	ns
t_{PHL}	TCK to Data Out during Test Logic Reset State		5.7	10.8	17.2	
t_{PLZ}	Disable Time	5.0	2.8	7.6	13.9	ns
t_{PHZ}	TCK to Data Out during Update-DR State		3.5	8.4	14.5	
t_{PLZ}	Disable Time	5.0	3.6	8.7	15.1	ns
t_{PHZ}	TCK to Data Out during Update-IR State		3.8	9.2	15.9	
t_{PLZ}	Disable Time	5.0	4.0	9.8	17.1	ns
t_{PHZ}	TCK to Data Out during Test Logic Reset State		4.2	9.9	16.6	
t_{PZL}	Enable Time	5.0	4.4	9.3	15.5	ns
t_{PZH}	TCK to Data Out during Update-DR State		3.0	7.5	13.3	
t_{PZL}	Enable Time	5.0	5.2	10.7	17.4	ns
t_{PZH}	TCK to Data Out during Update-IR State		3.9	9.0	15.4	
t_{PZL}	Enable Time	5.0	5.7	12.0	19.8	ns
t_{PZH}	TCK to Data Out during Test Logic Reset State		3.0	10.2	17.6	

Note 6: Voltage Range 5.0V ± 0.5V

Note: All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements

Scan Test Operation

Symbol	Parameter	V_{CC} (V) (Note 7)	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Guaranteed Minimum	Units
t_S	Setup Time Data to TCK (Note 8)	5.0	4.8	ns
t_H	Hold Time Data to TCK (Note 8)	5.0	2.5	ns
t_S	Setup Time, H or L $\overline{G1}$, $\overline{G2}$ to TCK (Note 9)	5.0	4.1	ns
t_H	Hold Time, H or L TCK to $\overline{G1}$, $\overline{G2}$ (Note 9)	5.0	1.7	ns
t_S	Setup Time, H or L DIR1, DIR2 to TCK (Note 10)	5.0	4.2	ns
t_H	Hold Time, H or L TCK to DIR1, DIR2 (Note 10)	5.0	2.3	ns
t_S	Setup Time Internal OE to TCK (Note 11)	5.0	3.8	ns
t_H	Hold Time, H or L TCK to Internal OE (Note 10)	5.0	2.3	ns
t_S	Setup Time, H or L TMS to TCK	5.0	8.7	ns
t_H	Hold Time, H or L TCK to TMS	5.0	1.5	ns
t_S	Setup Time, H or L TDI to TCK	5.0	6.7	ns
t_H	Hold Time, H or L TCK to TDI	5.0	5.0	ns
t_W	Pulse Width TCK: H L	5.0	10.2 8.5	ns
f_{MAX}	Maximum TCK Clock Frequency	5.0	50	MHz
t_{PU}	Wait Time, Power Up to TCK	5.0	100	ns
t_{DN}	Power Down Delay	0.0	100	ms

Note 7: Voltage Range 5.0V ± 0.5V

Note 8: Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0–8, 9–17, 18–26, 27–35, 36–44, 45–53, 54–62, 63–71).

Note 9: Timing pertains to BSR 74 and 78 only.

Note 10: Timing pertains to BSR 75 and 79 only.

Note 11: Timing pertains to BSR 72, 73, 76 and 77 only.

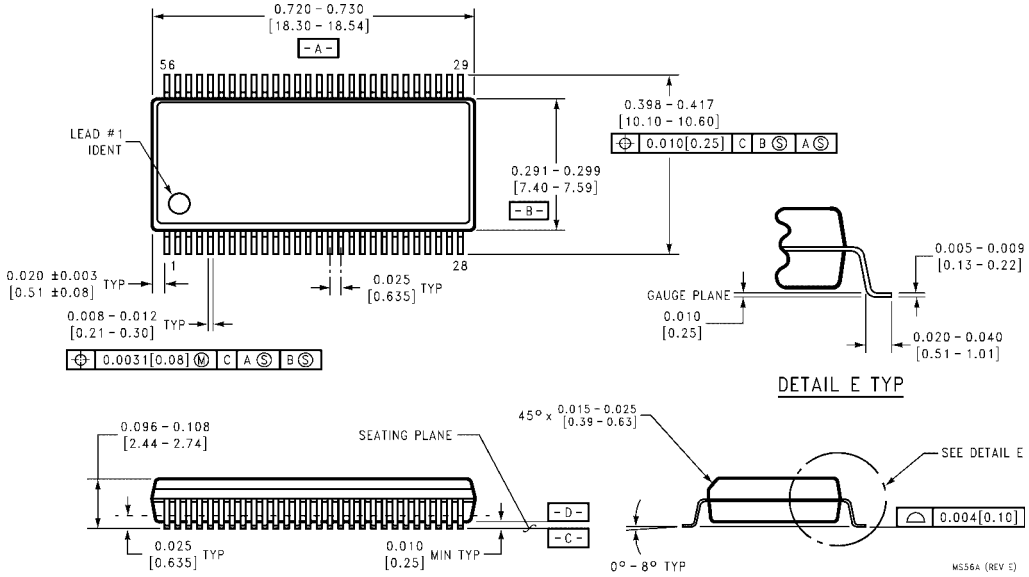
Note: All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.9	pF	$V_{CC} = 0.0V$ ($\overline{G}_n$, DIR_n)
$C_{I/O}$ (Note 12)	Output Capacitance	13.7	pF	$V_{CC} = 5.0V$ (A_n, B_n)

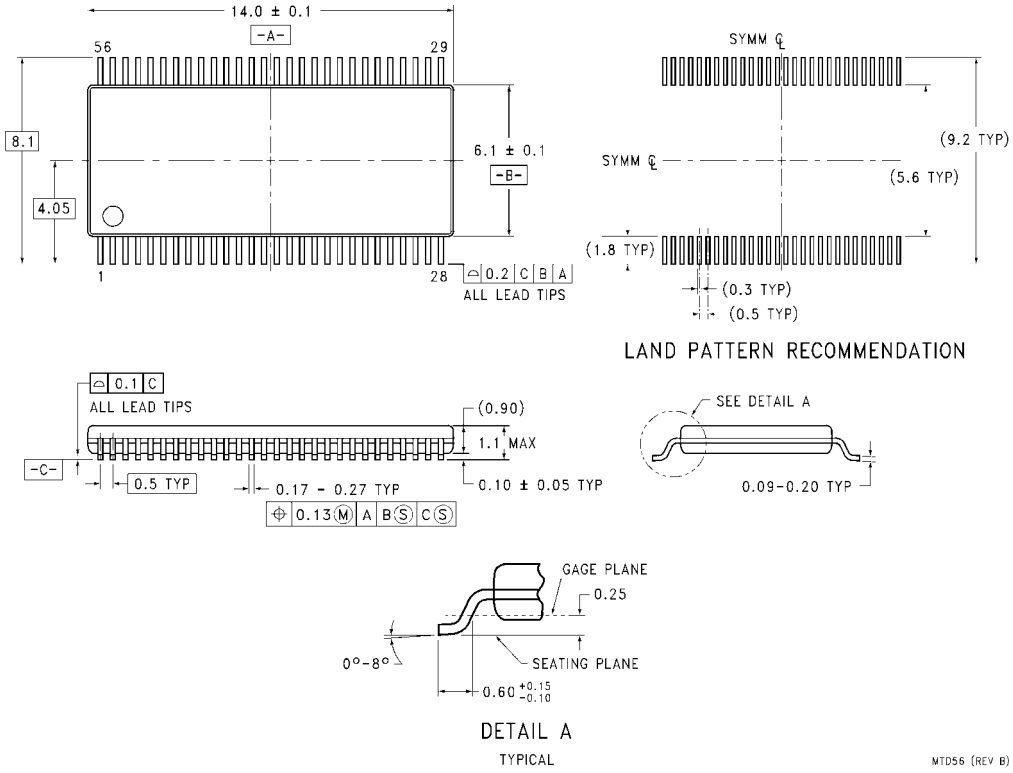
Note 12: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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