DATA SHEET

8-CHANNEL HIGH DEFINITION AUDIO CODEC STAC9220/9221/9223

DESCRIPTION

The STAC9220/9221/9223 are high fidelity, 8-channel audio CODECs compatible with Intel's High Definition (HD) Audio Interface. The STAC9220/9221/9223 CODECs provide stereo 24-bit resolution with sample rates up to 192 KHz. SPDIF I/O provides connectivity to consumer electronic equipment. The STAC9221 CODEC incorporates IDT's proprietary ΣΔ technology to achieve an estimated DAC SNR in excess of 105dB. The STAC9220/9223 CODECs incorporate IDT's proprietary ΣΔ technology to achieve an estimated DAC SNR in excess of 95dB. The STAC9223 has all of the features of the STAC9220 plus ADAT® Optical "Lightpipe." The STAC9220/9221/9223 CODECs provide high quality, HD Audio capability to notebook and media centric desktop PC applications.

FEATURES

- **High performance ΣΔ technology**
  - 105dB DAC SNR (STAC9221)
  - 95dB DAC SNR (STAC9220/9223)
- **Intel HD Audio interface**
- **Eight Channel (4 DAC pairs and 2 stereo ADCs) with 24-bit resolution**
  - Supports 7.1 Audio
  - Supports 5.1 Audio with Auxiliary channel for separate audio stream or Real Time Communication (RTC) channel
- **Sample Rates Up to 192 KHz**
- **Integrated Headphone Amps**
- **Stereo Microphone**
  - Supports Stereo Microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
- **Direct CDROM Recording Mixerless Design**
- **SPDIF In and Out**
- **Two-Pin Volume Up/Down Control**
- **Impedance Sensing**
- **Universal Jacks™ Functionality for Jack Retasking**
  - Headphone, Line Out, Line In & Microphone
    - Pins 35/36
    - Pins 39/41
  - Line Out, Line In and Microphone Support
    - Pins 16/17 (with strong line out)
    - Pins 23/24
    - Pins 21/22
  - Line In/MIC Support
    - Pins 14/15
- **Four Adjustable VREF Out pins for Microphone Bias**
- **I^2S Out (STAC9221)**
- **ADAT® Optical "Lightpipe" Output Support (STAC9221/9223)**
- **Digital PC Beep to all outputs**
- **+3.3 V and +5 V analog power supply options**
- **48-pin LQFP package (7mm x 7mm)**

THIRD PARTY SOFTWARE SUPPORT

- **WOW™ and Tru Surround™ from SRS**
- **Intellisonic Microphone Beam Forming from Knowles™**
- **Maxx BASS™ from Waves**
- **Dolby PC Audio Logo Program**
  - Program Levels
    - Dolby Sound Room™ (STAC9220/9223D)
    - Dolby Home Theater™ (STAC9220/9223D)
    - Dolby Master Studio™ (STAC9221D)
  - Dolby Technologies
    - Dolby Headphone™
    - Dolby ProLogic II™
    - Dolby Virtual Speaker™
- **Smart Stream™ from Sonic Focus**

Table of Contents

List of Figures

List of Tables

1. FEATURES

1.1. Overview

The STAC9220/9221/9223 are high fidelity, 8-channel audio CODECs compatible with Intel's High Definition (HD) Audio Interface. The STAC9220/9221/9223 CODECs provide stereo 24-bit resolution with sample rates up to 192 KHz. SPDIF I/O provides connectivity to consumer electronic equipment. The STAC9221 CODEC incorporate IDT's proprietary ΣΔ technology to achieve an estimated DAC SNR in excess of 105dB. The STAC9220/9223 CODEC incorporates IDT's proprietary ΣΔ technology to achieve an estimated DAC SNR in excess of 95dB. The STAC9223 has all of the features of the STAC9220 plus ADAT® Optical "Lightpipe." The STAC9220/9221/9223 CODECs provide high quality, HD Audio capability to notebook and media centric desktop PC applications.

1.2. Features

- High performance ΣΔ technology
  - 105dB DAC SNR (STAC9221)
  - 95dB DAC SNR (STAC9220/9223)
- Intel HD Audio interface
- Eight Channel (4 DAC pairs and 2 stereo ADCs) with 24-bit resolution
  - Supports 7.1 Audio
  - Supports 5.1 Audio with Auxiliary channel for separate audio stream or Real Time Communication (RTC) channel
- Sample Rates Up to 192 KHz
- Integrated Headphone Amps
- Stereo Microphone
  - Supports Stereo Microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
- Direct CDROM Recording Mixerless Design
- SPDIF In and Out
- Two-Pin Volume Up/Down Control
- Impedance Sensing
- Universal Jacks™ Functionality for jack retasking
  - Headphone, Line Out, Line In & Microphone
    - Pins 35/36
    - Pins 39/41
  - Line Out, Line In and Microphone Support
    - Pins 16/17 (with strong line out)
    - Pins 23/24
    - Pins 21/22
  - Line In/MIC Support
    - Pins 14/15
- Four Adjustable VREF Out pins for Microphone Bias
- I^2S Out (STAC9221)
- ADAT® Optical "Lightpipe" Output Support (STAC9221/9223)

- Digital PC Beep to all outputs
- +3.3V and +5V/4V[1] analog power supply options
- 48-pin LQFP package option (7mm x 7mm)

Note: 1. The +4V Analog voltage is supported by the +5V version of the STAC922x or STAC922xD. Request the +4V configuration of the driver.

1.3. Third Party Software Support

- WOW™ and Tru Surround™ from SRS
- Intellisonic Microphone Beam Forming from Knowles™
- Maxx BASS™ from Waves
- Dolby PC Audio Logo Program[2]
  - Program Levels
    - Dolby Sound Room™ (STAC9220D/9223D)
    - Dolby Home Theater™ (STAC9220D/9223D)
    - Dolby Master Studio™ (STAC9221D)
  - Dolby Technologies
    - Dolby Headphone™
    - Dolby ProLogic II™
    - Dolby Virtual Speaker™
- Smart Stream™ from Sonic Focus

Note: 2. System manufacturers must obtain system license from Dolby.

1.4. Description

The STAC9220/9221/9223 are high fidelity, 8-channel audio CODECs compatible with the Intel High Definition (HD) Audio Interface. The STAC9220/9221/9223 provide high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

The STAC9221 CODEC incorporate IDT's proprietary ΣΔ technology to achieve an estimated DAC SNR in excess of 105dB. The STAC9220/9223 CODEC incorporates IDT's proprietary ΣΔ technology to achieve an estimated DAC SNR in excess of 95dB. The STAC9223 has all of the features of the STAC9220 plus ADAT Optical “Lightpipe.” The higher performance and quality of IDT’s audio solutions brings consumer electronics level performance to the notebook, desktop and media center PC.

The STAC9220/9221/9223 provide stereo 24-bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9220/9221/9223 DAC, ADC and SPDIF In/Out support sample rates of 96 KHz, 48 KHz and 44.1 KHz. Additional sample rates are supported by the driver software.

The STAC9220/9221/9223 support all desired eight channel configurations, including switchable Headphone Out, and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini-disk drives or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC.

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9220/9221/9223 have three General Purpose I/O (GPIO) pins. The STAC920/9221/9223 also provide a single ended CD input for compatibility with DRM solutions and to support legacy OS issues.

The STAC9220/9221/9223 integrates a headphone amplifier which is available on Ports A and D. The headphone amplifier is switchable between these two outputs for increased flexibility, enhanced user experience, and reduced implementation costs. An additional headphone is supported on Port F.

The Universal Jack capabilities allow the CODECs to detect when audio devices are connected to the CODEC, and to allow the CODECs to be reconfigured to support these devices regardless of which port they are plugged into the system. SPDIF input sensing is also supported. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

Note: The Jack Detect circuit and component selection are critical for accurate detection of audio jacks on individual ports. Please see the IDT STAC922x reference design for circuit implementation details.

The STAC9220/9221/9223 operates with a 3.3 V digital supply and is available in either 5 V analog supply or 3.3 V analog supply options.

The STAC9220/9221/9223 are available in a 48-pin LQFP package. The 48-pin LQFP is only available in the Environmental package (Pb-free).

The STAC9220/9221/9223 are supported with IDT's high quality software solutions which include drivers for all major Windows operating systems from Microsoft, parametric SoftEQ, and Digital Rights Management. Third party plug-in capability is easily achieved with the IDT Kernel Processing Interface, to support high-valued, third party technologies like SRS WOW®, Knowles® Microphone Beam Forming, Waves MaxxBASS®, Dolby Headphone®, Dolby ProLogic II® and Dolby Virtual Speaker® and more.

2. CHARACTERISTICS

2.1. Audio Fidelity

DAC SNR:	105dB	(STAC9221)	95dB	(STAC9220/9223)
ADC SNR:	95dB	(STAC9221)	90dB	(STAC9220/9223)

2.2. Electrical Specifications

2.2.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9220/9221/9223. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0^{o}C to +70^{o}C
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		260 ^{o}C for 10 seconds ***** Soldering temperature information for all available packages begins on page 169.

2.2.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: The +4 V Analog voltage is supported by the +5 V version of the STAC922x or STAC922xD.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C

ESD: The STAC9220/9221/9223 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9220/9221/9223 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.3. STAC922x/STAC922xD 5V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0 V ± 5%, DVdd = 3.3 V ± 5%, AVss=DVss=0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 VRMS, 10 KΩ / 50 pF load, Testbench Characterization BW: 20 KHz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	90	-	dB
Analog Frequency Response (Note 3)	10		30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-93	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-88	-	dB
HEADPHONE_OUT (32 Ω load)	-	-85	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-90	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	105	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	93	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to DAC (1 KHz Signal Frequency) Crosstalk		-101		dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-80	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45 X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	5	20	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	µsec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	300	psec

1. With +30dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.4. STAC922x/STAC922xD 4V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 4.0 V ± 5%, DVdd = 3.3 V ± 5%, AVss=DVss=0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 VRMS, 10 KΩ / 50 pF load, Testbench Characterization BW: 20 KHz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	85	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D(-3dBV input Level)	-	-85	-	dB
HEADPHONE_OUT (32 Ω load)	-	-88	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-85	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	85	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-80	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45 X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	100		-	ppm/ºC
DAC Offset Voltage	-	5	20	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-100		-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	µsec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	750	psec

1. With +30dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.5. STAC922x/STAC922xD 3.3V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 3.3 V ± 5%, DVdd = 3.3 V ± 5%, AVss=DVss=0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 VRMS, 10 KΩ / 50 pF load, Testbench Characterization BW: 20 KHz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	0.7	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	80	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D(-3dBV input Level)	-	-75	-	dB
HEADPHONE_OUT (32 Ω load)	-	-85	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-88	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	85	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejcn (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-70	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45 X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	100		-	ppm/ºC
DAC Offset Voltage	-	5	20	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	µsec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	750	psec

1. With +30dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

3. POWER CONSUMPTION

3.1. Digital

Power State	Typical*	Max	units
D0	66	75	mA
D1	66	75	mA
D2	18	30	mA
D3	10	20	mA

Table 1. Digital Power Consumption

3.2. Analog: AVDD = 5 V

Power State	Typical*	Max	units
D0	55	65	mA
D1	55	65	mA
D2	25	35	mA
D3	15	20	mA

Table 2. Analog Power Consumption 5V

3.3. Analog: AVDD = 3.3 V

Power State	Typical*	Max	units
D0	45	55	mA
D1	45	55	mA
D2	20	30	mA
D3	13	18	mA

Table 3. Analog Power Consumption 3.3V

*Typical results are with all DACs and all ADCs on, and with audio playing.

4. DETAILED DESCRIPTION

4.1. Audio Jack Presence Detect

SENSE_A pin is used to detect the presence of plugs in ports A, B, C, and D. SENSE_B pin is used to detect the presence of plugs in ports E and F. Refer to the reference design for port detect circuitry. Select the precision of the resistor used as follows.

Table 4. Audio Jack Presence Detect

Nominal Voltage (+-5%)	Resistor Tolerance Sense A (If port D is used)	Resistor Tolerance Sense A (If port D is not used)	Resistor Tolerance Sense B (For ports E and F)
5V	1%	1%	1%
4.5V	1%	1%	1%
4V	0.50%	1%	1%
3.3V	0.10%	1%	1%

4.2. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz or 96 KHz, and implements internal Jack Sensing.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs. Advanced features such as record-slot select and SPDIF_IN routing to the DAC allows for simultaneous record and play.

4.3. SPDIF Output

SPDIF Output can operate at 44.1 KHz, 48 KHz and 96 KHz, as defined in the Intel High Definition Audio Specification, with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

4.4. Universal Jacks™

IDT's Universal Jacks™ technology allows for the greatest flexibility in board design and implementation. For the STAC9220/9221/9223 the Universal Jacks™ capabilities are as follows[1]:

- Pins 39/41can be used for[2]:
  - Headphone Out
  - Line Out
  - Line In
  - Microphone with 0/10/20/30/40dB Microphone boost[3]
- Pins 35/36 can be used for[2]:
  - Headphone Out
  - Line Out
  - Line In
  - Microphone with 0/10/20/30/40dB Microphone boost[3]
- Pins 23/24 can be used for:
  - Line Out
  - Line In
  - Microphone with 0/10/20/30/40dB Microphone boost[3]
- Pins 21/22 can be used for:
  - Line Out
  - Line In
  - Microphone with 0/10/20/30/40dB Microphone boost[3]
- Pins 16/17 can be used for:
  - Headphone Out
  - Line Out
  - Line In
  - Microphone with 0/10/20/30/40dB Microphone boost[3]
- Pins 14/15 can be used for:
  - Line In
  - Microphone with 0/10/20/30/40dB Microphone boost[3]

Note[1]: On the STAC9220/9221/9223 only one function can be selected on each pin pair at a time. For example, a pin pair cannot be configured as an input and output at the same time. Configuration can be changed at any time.

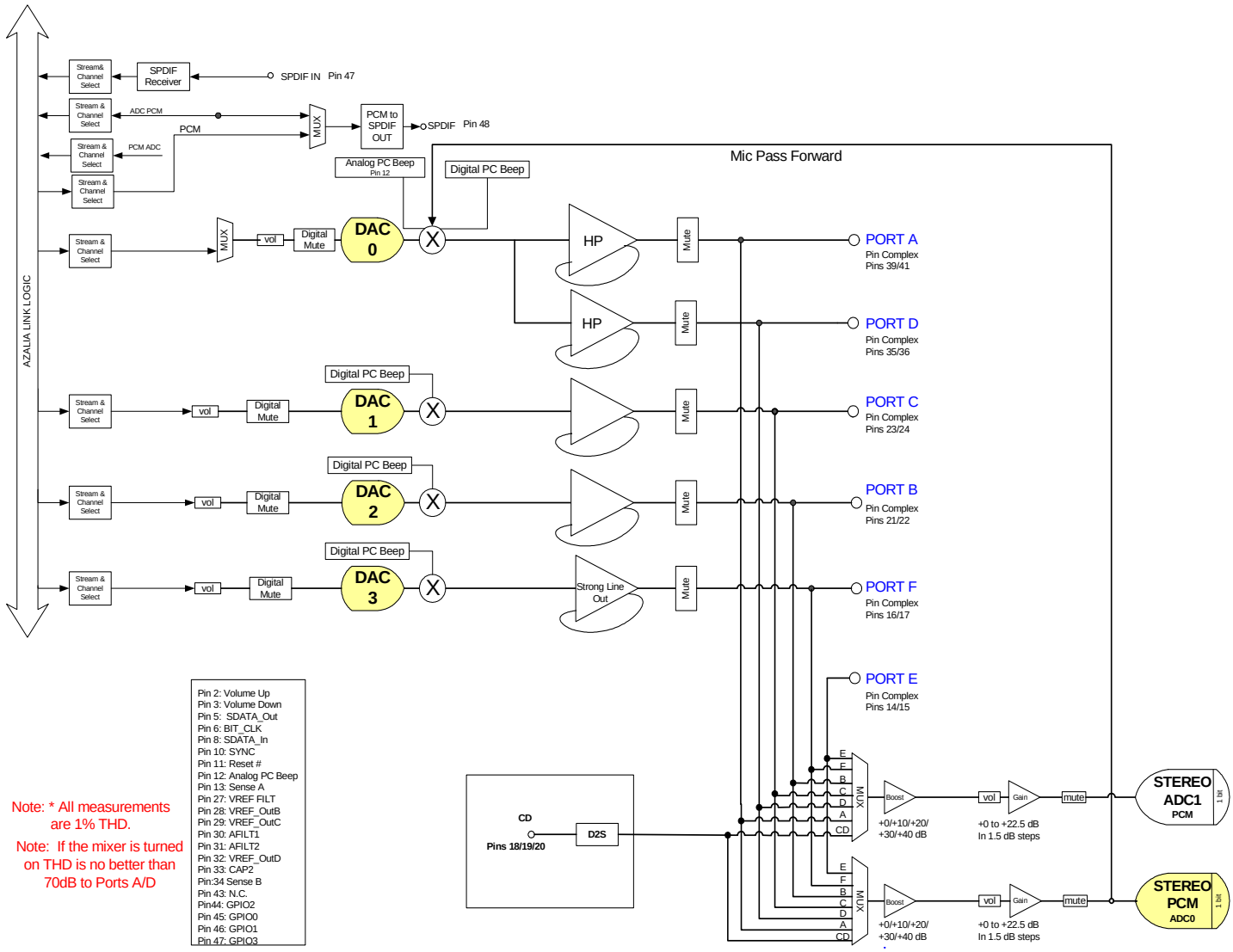
Note[2]: Headphone capabilities are provided on pins 39/41 and 35/36, but one should not put headphone loads on both sets of pins at the same time.

Note[3]: 40dB Microphone boost is not recommended.

5. FUNCTIONAL BLOCK DIAGRAMS AND CONNECTION DIAGRAMS

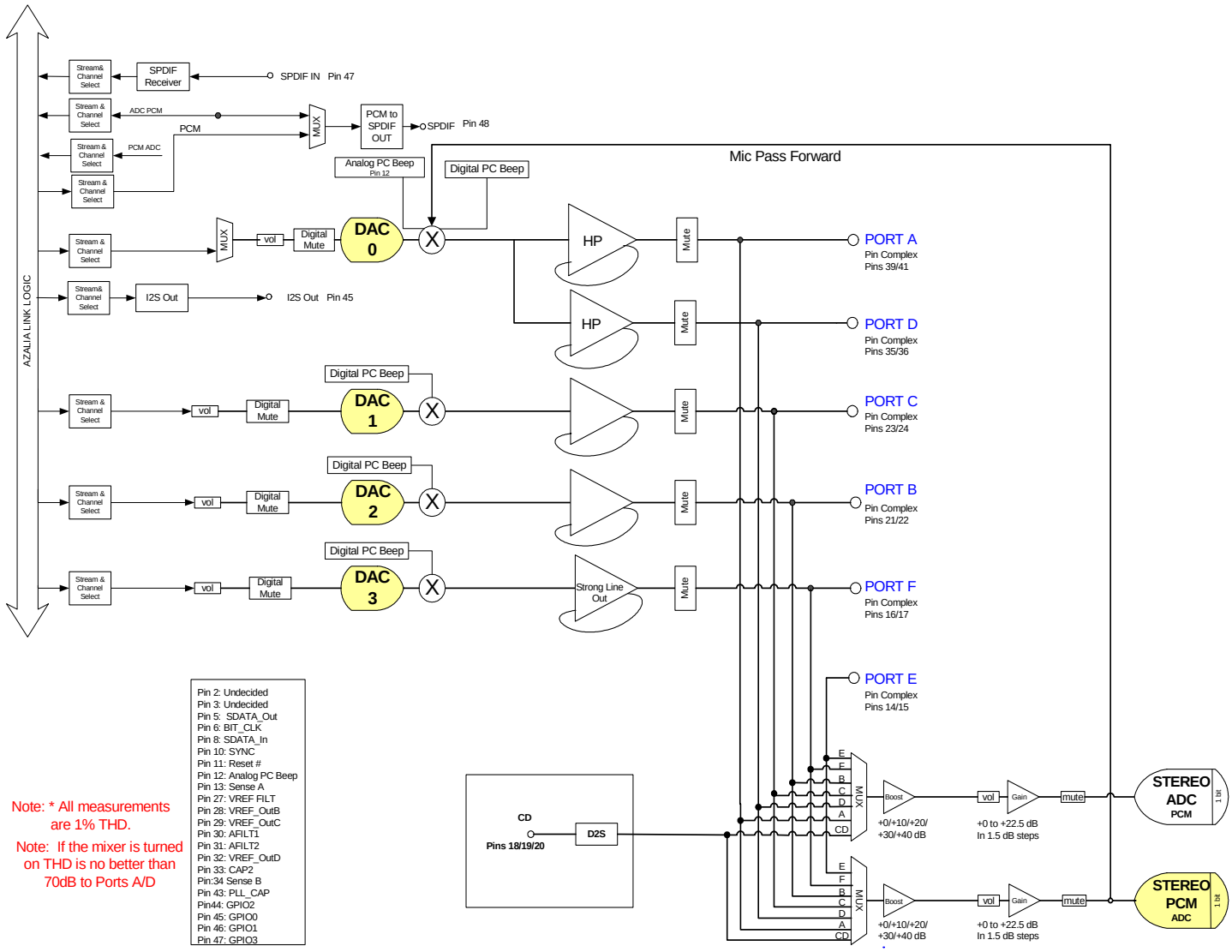
5.1. STAC9220/9223 Functional Block Diagram

Figure 1. Functional Block Diagram STAC9220/9223



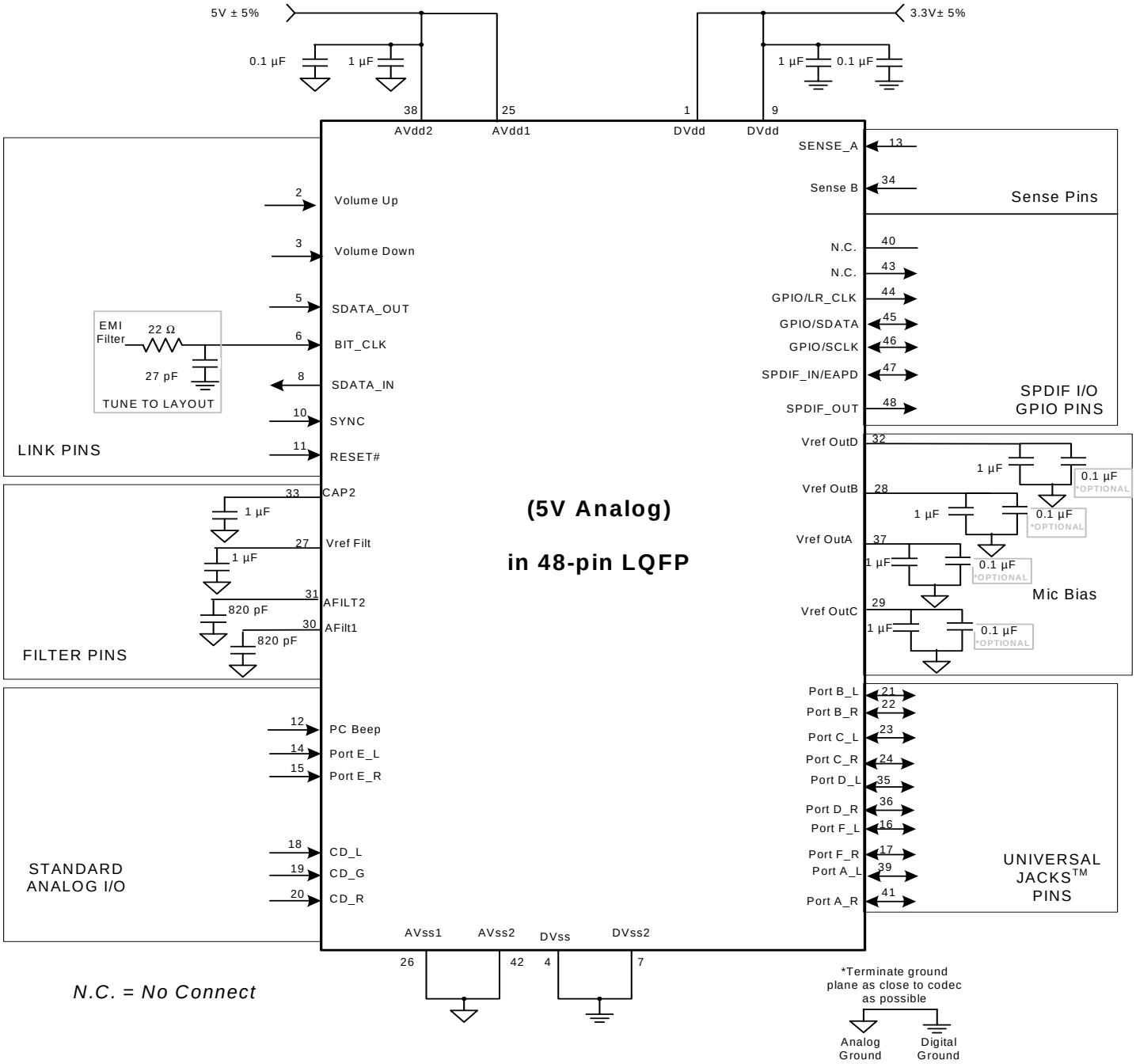
5.2. STAC9221 Functional Block Diagram

Figure 2. Functional Block Diagram STAC9221



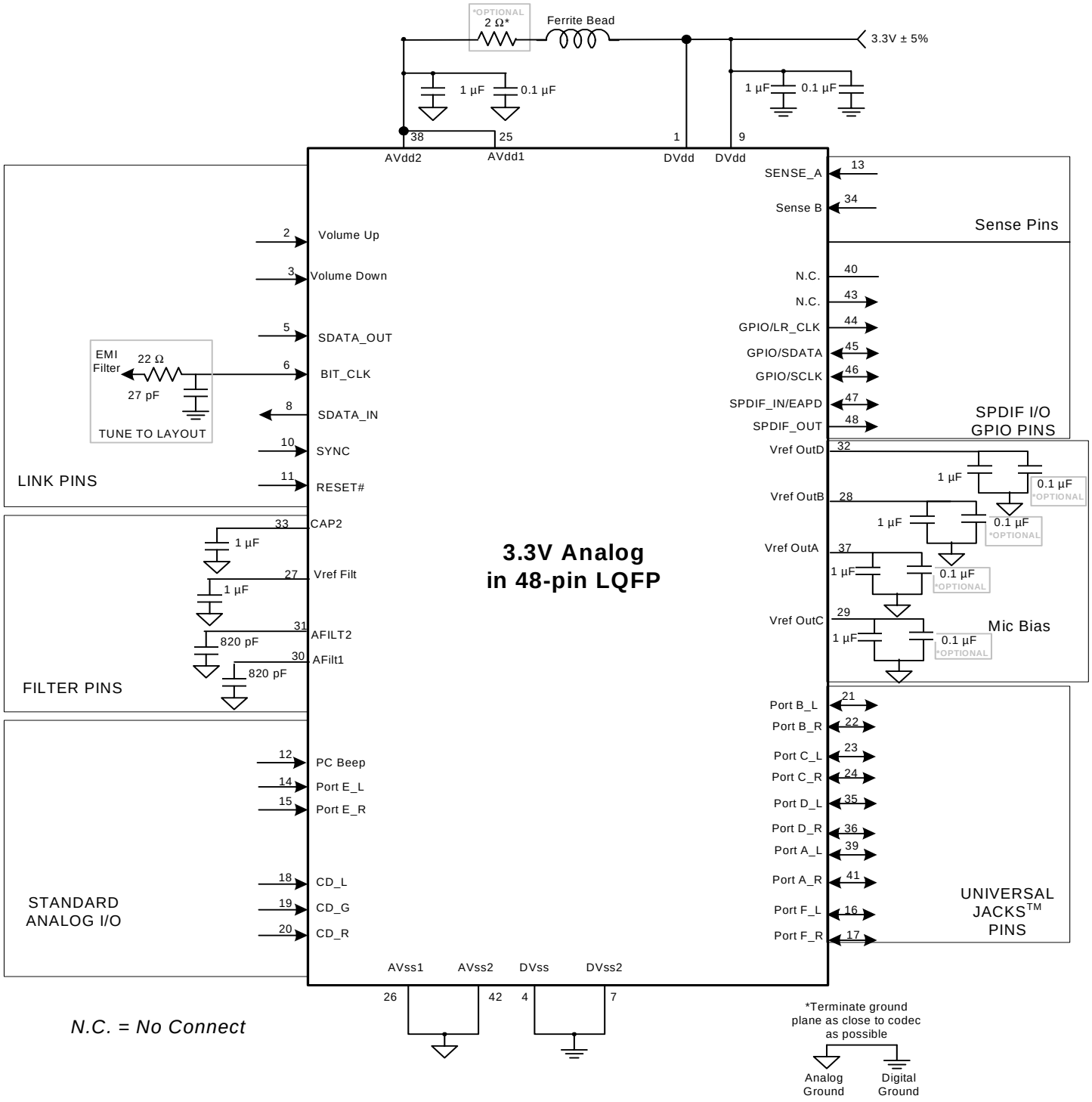
5.3. STAC9220/9223 Typical Connection Diagram for 48-pin LQFP

Figure 3. Typical Connection Diagram STAC9220/9223



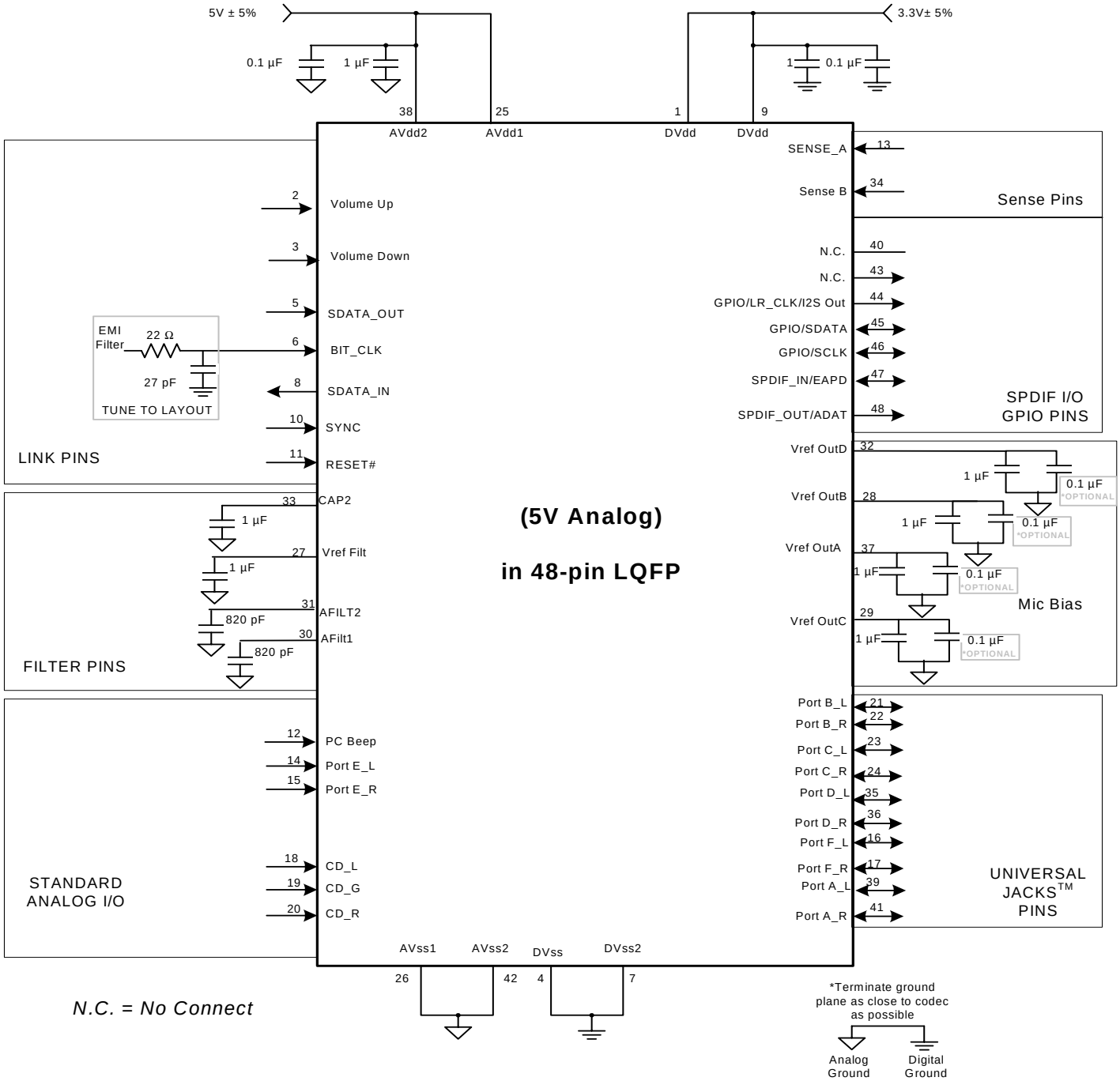
5.4. STAC9220/9223 Split Independent Power Supply for 48-pin LQFP

Figure 4. Split Independent Power Supply STAC9220/9223



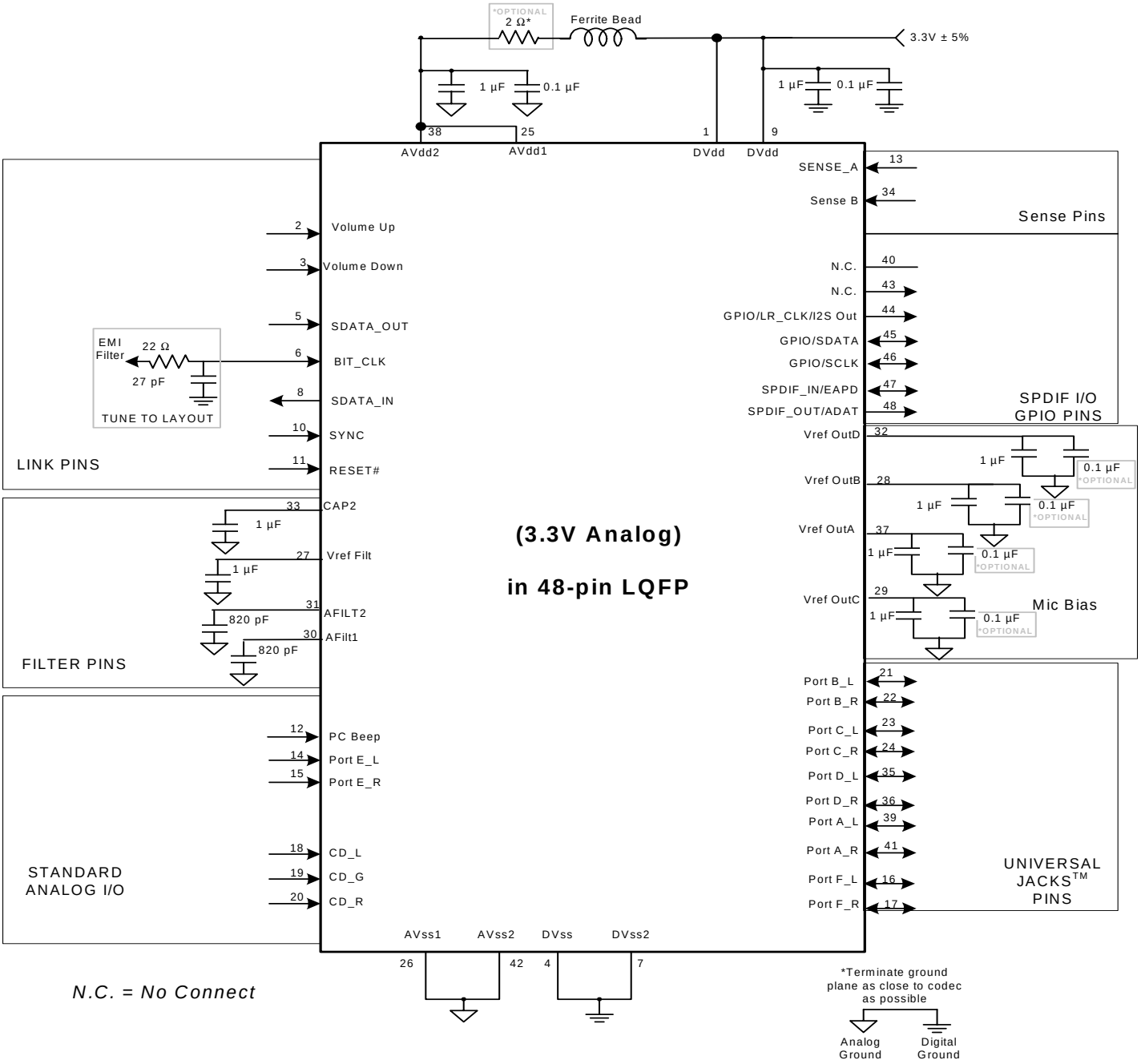
5.5. STAC9221 Typical Connection Diagram for 48-pin LQFP

Figure 5. Typical Connection Diagram STAC9221



5.6. STAC9221 Split Independent Power Supply for 48-pin LQFP

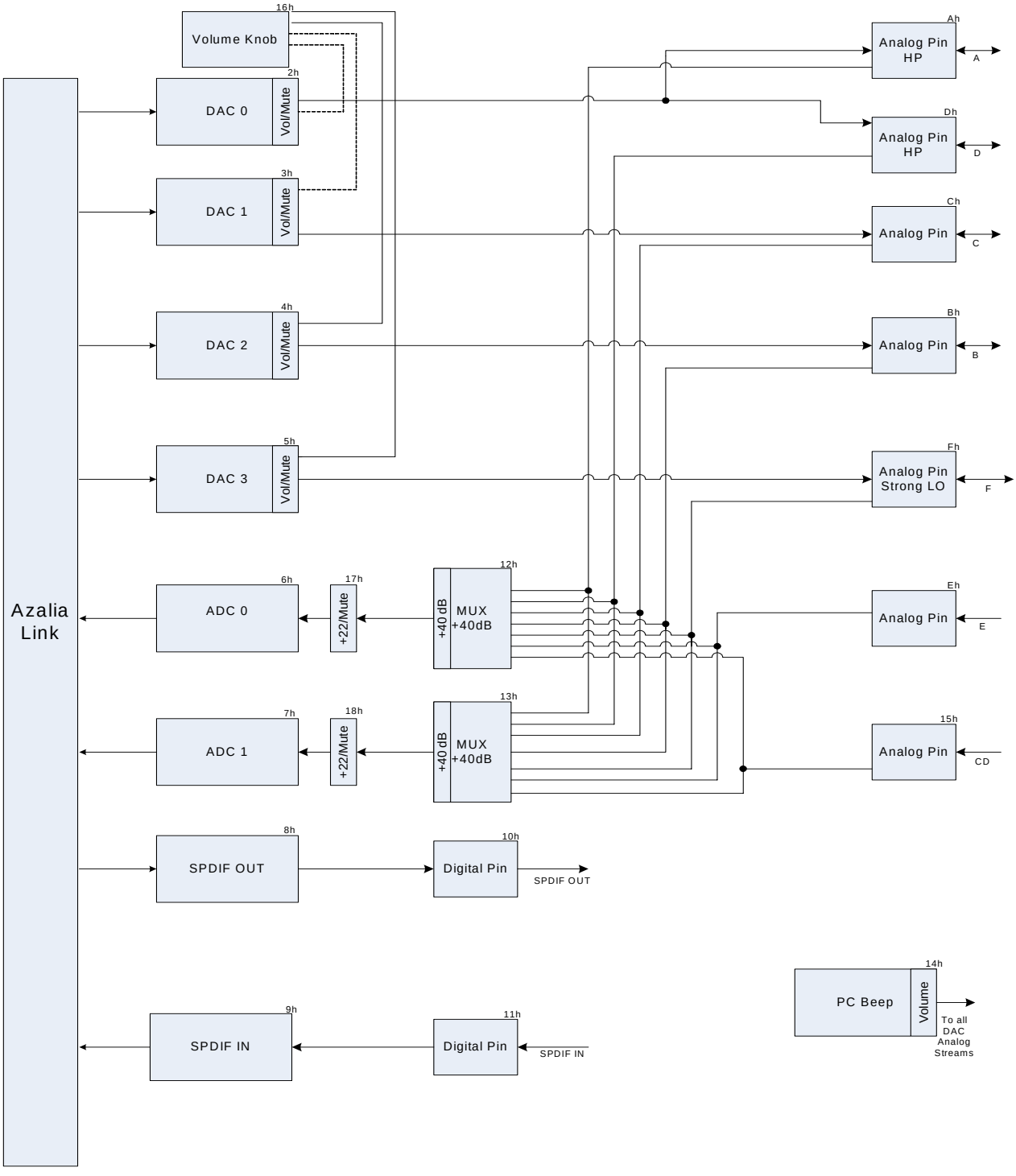
Figure 6. Split Independent Power Supply STAC9221



6. WIDGET INFORMATION

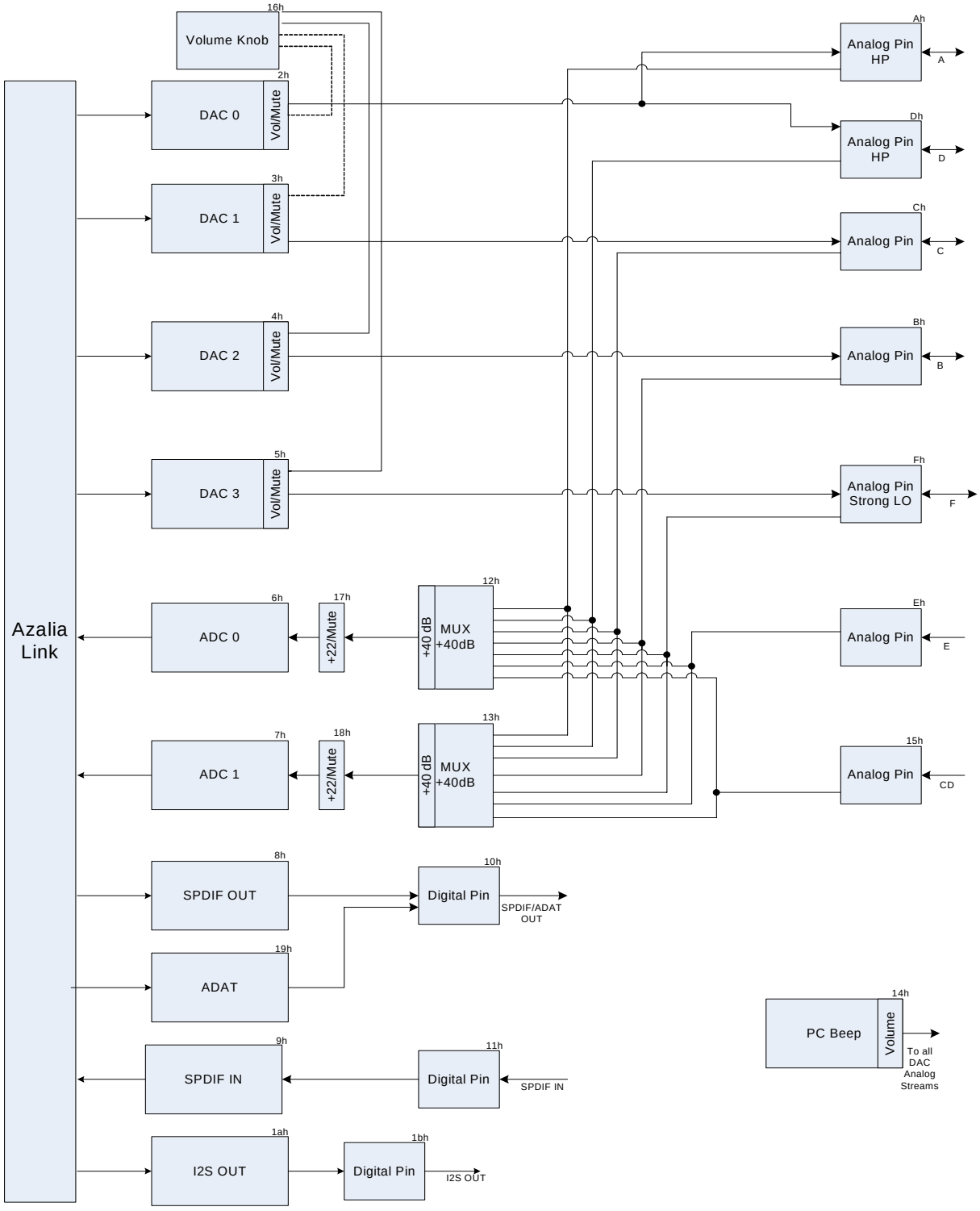
6.1. STAC9220/9223 Widget Diagrams

Figure 7. Widget Diagram STAC9220/9223



6.2. STAC9221Widget Diagrams

Figure 8. Widget Diagram STAC9221



6.3. Widget List STAC9220/9221/9223

Table 5. High Definition Audio Widget

ID	Widget Name	Description
1h	Audio Function Group	Audio Function Group
2h	DAC0	Stereo Output to DAC
3h	DAC1	Stereo Output to DAC
4h	DAC2	Stereo Output to DAC
5h	DAC3	Stereo Output to DAC
6h	ADC0	Stereo Input Mux from ADC
7h	ADC1	Stereo Input Mux from ADC
8h	SPDIF_OUT	Stereo Output for SPDIF_Out
9h	SPDIF_IN	Stereo Input for SPDIF_In
10h	SPDIF-Out Pin	Pin Widget for SPDIF_Out pin 48
11h	SPDIF-In Pin	Pin Widget for SPDIF_In pin 47
12h	ADC0Mux	ADC Mux and Boost for inputs to ADC
13h	ADC1Mux	ADC Mux and Boost for inputs to ADC
14h	Digital PC Beep	Digital PC Beep
15h	CD	CD Pin Widget pins 18/19/20
16h	Master Volume	Master Volume Controls
17h	ADC0Vol	ADC Mux and Volume for inputs to ADC
18h	ADC1Vol	ADC Mux and Volume for inputs to ADC
19h	ADAT †	Stereo Output for ADAT † (STAC9221/9223)
Ah	Headphone	Headphone Pin Widget pins 39/41 (can also act as Line In, Line Out, or Microphone)
Dh	Headphone	Headphone Pin Widget pins 35/36 (can also act as Line In, Line Out, or Microphone)
Ch	Line In	Line In Pin Widget pins 23/24 (can also act as Microphone or Line Out)
Bh	Microphone	Microphone Pin Widget pins 21/22 (can also act as Line Out and Line In)
Fh	Line Out	Line Out Pin Widget pins 16/17 (can also act as HP, Line In, or Microphone)
Eh	Line In	Line In Pin Widget pins 14/15 (can also act as Microphone)
1ah	I2S Out *	Stereo Output for I2S Out *
1bh	I2S Out Pin *	Pin Widget for I2S Out pin 44 *

*Note: *: Functionality for STAC9221 only.*
†: Functionality for STAC9221 and STAC9223.

6.4. Root Node (NID = 0x00)

6.4.1. Root ID

Table 6. Root ID Command Verb Format

	Verb ID	Payload	Response
Get	F00	00	See bitfield table

Table 7. Root ID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Vendor	R	0x8384	Vendor ID: STAC9220/21/23 = 8384h
[15:8]	DeviceFix	R	0x76	Device ID: STAC9221 = 7682h; STAC9221-Dolby = 7683h; STAC9220 = 7880h; STAC9220/9223-Dolby = 7681h
[7:0]	DeviceProg	R	0x80	Device ID: STAC9221 = 7682h; STAC9221-Dolby = 7683h; STAC9220 = 7880h; STAC9220/9223-Dolby = 7681h

6.4.2. Root RevID

Table 8. Root RevID Command Verb Format

	Verb ID	Payload	Response
Get	F00	02	See bitfield table

Table 9. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd	R	0x00	Reserved
[23:20]	Major	R	0x1	Major rev number of compliant HD Audio specification
[19:16]	Minor	R	0x0	Minor rev number of compliant HD Audio specification

Table 9. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:12]	VendorFix	R	0x3	Vendor's rev number for this device: STAC9220/9221/9223 = xxh
[11:8]	VendorProg	R	0x1	Vendor's rev number for this device: STAC9220/9221/9223 = xxh
[7:4]	SteppingFix	R	0x0	Vendor stepping number within the Vendor RevID: STAC9220/9221/9223 = xxh
[3:0]	SteppingProg	R	0x1	Vendor stepping number within the Vendor RevID: STAC9220/9221/9223 = xxh

6.4.3. Root NodeInfo

Table 10. Root NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 11. Root NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x00	Reserved
[23:16]	StartNID	R	0x01	Starting node number (NID) of first function group
[15:8]	Rsvd1	R	0x00	Reserved
[7:0]	TotalNodes	R	0x01	Total number of nodes

6.5. AFG Node (NID = 0x01)

6.5.1. AFG Reset

Table 12. AFG Reset Command Verb Format

	Verb ID	Payload	Response
Get	7FF	00	See bitfield table
Set1	7FF	See bits [7:0] of bitfield table	0000_0000h

Table 13. AFG Reset Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:0]	Response	R	0x0	Reserved. Overlaps Execute.
[0]	Execute	W	0x0	Function Reset. Function Group reset is executed when the Set verb (7FF) is written with 8-bit payload of 00h. The CODEC should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.

6.5.2. AFG NodeInfo

Table 14. AFG NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 15. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:16]	StartNID	R	0x2	Starting node number for function group subordinate nodes.

Table 15. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Rsvd1	R	0x0	Reserved
[7:0]	TotalNodes	R	0x1A	Total number of nodes.

6.5.3. AFG Type

Table 16. AFG Type Command Verb Format

	Verb ID	Payload	Response
Get	F00	05	See bitfield table

Table 17. AFG Type Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:9]	Rsvd	R	0x0	Reserved
[8]	UnSol	R	0x1	This node is capable of generating an unsolicited response, and will respond to the Unsolicited Response verb (Verb ID 708h).
[7:0]	NodeType	R	0x01	Node type = Audio Function Group

6.5.4. AFG Cap

Table 18. AFG Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	08	See bitfield table

Table 19. AFG Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd3	R	0x0	Reserved
[16]	BeepGen	R	0x1	Optional Beep Generator is present
[15:12]	Rsvd2	R	0x0	Reserved

Table 19. AFG Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[11:8]	InputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.
[7:4]	Rsvd1	R	0x0	Reserved
[3:0]	OutputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.

6.5.5. AFG PCMCap

Table 20. AFG PCMCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 21. AFG PCMCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported

Table 21. AFG PCMCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) supported

6.5.6. AFG Stream

Table 22. AFG Stream Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table

Table 23. AFG Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x0	No support for non-PCM data.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

6.5.7. AFG InAmpCap

Table 24. AFG InAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0D	See bitfield table

Table 25. AFG InAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x5	Size of each step in the gain range = 1.5dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x0E	Number of steps in the gain range = 15 (0dB to 22.5 dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.5.8. AFG SupPwrState

Table 26. AFG SupPwrState Command Verb Format

	Verb ID	Payload	Response
Get	F00	0F	See bitfield table

Table 27. AFG SupPwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	D3Sup	R	0x1	Power State D3 is supported. Allows for lowest possible power consuming state under software control (and still properly respond to a subsequent Power State command).

Table 27. AFG SupPwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	D2Sup	R	0x1	Power State D2 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10 msec.
[1]	D1Sup	R	0x1	Power State D1 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10 msec, excepting analog pass-through circuits which must remain fully on.
[0]	D0Sup	R	0x1	Power State D0 is supported. Node power state is fully on.

6.5.9. AFG GPIOCnt

Table 28. AFG GPIOCnt Command Verb Format

	Verb ID	Payload	Response
Get	F00	11	See bitfield table

Table 29. AFG GPIOCnt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	GPIWake	R	0x1	Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIO's configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.
[30]	GPIUnsol	R	0x1	Unsolicited Response capability. Assuming the Unsolicited Enable Mask controls are enabled, GPIO's configured as inputs can generate an Unsolicited Response on the link when there is a change in level on the pin.
[29:24]	Rsvd	R	0x0	Reserved
[23:16]	NumGPIs	R	0x00	Number of GPI pins supported by function
[15:8]	NumGPOs	R	0x00	Number of GPO pins supported by function
[7:0]	NumGPIOs	R	0x04	Number of GPIO pins supported by function

6.5.10. AFG GPIO Polarity

Table 30. AFG GPIO Polarity Command Verb Format

	Verb ID	Payload	Response
Get	FE7	00	See bitfield table
Set1	70E7	See bits [7:0] of bitfield table	0000_0000h

Table 31. AFG GPIO Polarity Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
3	GP3	RW	0x1	GPIO 3 Input Polarity Control (used in conjunction with GPIOSticky) and Output Type Control. When configured as a level-sensitive input: 0 = inverted 1 = not inverted (default) When configured as an edge-sensitive input: 0 = falling-edge triggered 1 = rising-edge triggered When configured as an output: 0 = push-pull (CMOS) 1 = open drain (default)
2	GP2	RW	0x1	GPIO 2 Input Polarity Control (used in conjunction with GPIOSticky) and Output Type Control. When configured as a level-sensitive input: 0 = inverted 1 = not inverted (default) When configured as an edge-sensitive input: 0 = falling-edge triggered 1 = rising-edge triggered When configured as an output: 0 = push-pull (CMOS) 1 = open drain (default)

Table 31. AFG GPIO Polarity Command Response Format

Bit	Bitfield Name	RW	Reset	Description
1	GP1	RW	0x1	GPIO 1 Input Polarity Control (used in conjunction with GPIOSticky) and Output Type Control. When configured as a level-sensitive input: 0 = inverted 1 = not inverted (default) When configured as an edge-sensitive input: 0 = falling-edge triggered 1 = rising-edge triggered When configured as an output: 0 = push-pull (CMOS) 1 = open drain (default)
0	GP0	RW	0x1	GPIO 0 Input Polarity Control (used in conjunction with GPIOSticky) and Output Type Control. When configured as a level-sensitive input: 0 = inverted 1 = not inverted (default) When configured as an edge-sensitive input: 0 = falling-edge triggered 1 = rising-edge triggered When configured as an output: 0 = push-pull (CMOS) 1 = open drain (default)

6.5.11. AFG OutAmpCap

Table 32. AFG OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 33. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x02	Size of each step in the gain range = 0.75dB
[15]	Rsvd2	R	0x0	Reserved

Table 33. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14:8]	NumSteps	R	0x7F	Number of steps in the gain range = 128 (-96dB to +0dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x7F	0dB-step is programmed with this offset

6.5.12. AFG PwrState

Table 34. AFG PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 35. AFG PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x2	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x2	PS-Set: Current power setting of referenced node. 0: All Powered-On 1: D1 = > PR0, PR1 2: D2 = > PR0, PR1, PR2, PR6, EAPD 3: D3 = > PR6, PR5, PR3, PR2, PR1, PR0, EAPD Note: PR4 is not mapped in HD Audio

6.5.13. AFG UnsolResp

Table 36. AFG UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 37. AFG UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x0	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.5.14. AFG GPIO

Table 38. AFG GPIO Command Verb Format

	Verb ID	Payload	Response
Get	F15	00	See bitfield table
Set1	715	See bits [7:0] of bitfield table	0000_0000h

Table 39. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Data3	RW	0x0	Data for GPIO3 (Pin 47). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[2]	Data2	RW	0x0	Data for GPIO2 (Pin 44). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

Table 39. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	Data1	RW	0x0	Data for GPIO1 (Pin 46). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[0]	Data0	RW	0x0	Data for GPIO0 (Pin 45). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

6.5.15. AFG GPIOEn

Table 40. AFG GPIOEn Command Verb Format

	Verb ID	Payload	Response
Get	F16	00	See bitfield table
Set1	716	See bits [7:0] of bitfield table	0000_0000h

Table 41. AFG GPIOEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Mask3	RW	0x0	Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[2]	Mask2	RW	0x0	Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[1]	Mask1	RW	0x0	Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[0]	Mask0	RW	0x0	Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control

6.5.16. AFG GPIODir

Table 42. AFG GPIODir Command Verb Format

	Verb ID	Payload	Response
Get	F17	00	See bitfield table
Set1	717	See bits [7:0] of bitfield table	0000_0000h

Table 43. AFG GPIODir Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Control3	RW	0x0	Direction control for GPIO3 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[2]	Control2	RW	0x0	Direction control for GPIO2 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[1]	Control1	RW	0x0	Direction control for GPIO1 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[0]	Control0	RW	0x0	Direction control for GPIO0 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output

6.5.17. AFG GPIOWakeEn

Table 44. AFG GPIOWakeEn Command Verb Format

	Verb ID	Payload	Response
Get	F18	00	See bitfield table
Set1	718	See bits [7:0] of bitfield table	0000_0000h

Table 45. AFG GPIOWakeEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	W3	RW	0x0	Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[2]	W2	RW	0x0	Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[1]	W1	RW	0x0	Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[0]	W0	RW	0x0	Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.

6.5.18. AFG GPIOUnsol

Table 46. AFG GPIOUnsol AFG GPIOUnsol Command Verb Format

	Verb ID	Payload	Response
Get	F19	00	See bitfield table
Set1	719	See bits [7:0] of bitfield table	0000_0000h

Table 47. AFG GPIOUnsol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	EnMask3	RW	0x0	Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO3 is configured as input and changes state.
[2]	EnMask2	RW	0x0	Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[1]	EnMask1	RW	0x0	Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO1 is configured as input and changes state.
[0]	EnMask0	RW	0x0	Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.

6.5.19. AFG GPIOSticky

Table 48. AFG GPIOSticky Command Verb Format

	Verb ID	Payload	Response
Get	F1A	00	See bitfield table
Set1	71A	See bits [7:0] of bitfield table	0000_0000h

Table 49. AFG GPIOSticky Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Mask3	RW	0x0	GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[2]	Mask2	RW	0x0	GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[1]	Mask1	RW	0x0	GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[0]	Mask0	RW	0x0	GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.

6.5.20. AFG SubID

Table 50. AFG SubID Command Verb Format

	Verb ID	Payload	Response
Get	F20	00	See bitfield table
Set1	720	See bits [7:0] of bitfield table	0000_0000h
Set2	721	See bits [15:8] of bitfield table	0000_0000h
Set3	722	See bits [23:16] of bitfield table	0000_0000h
Set4	723	See bits [31:24] of bitfield table	0000_0000h

Table 51. AFG SubID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Subsys3	RW	0x00	Subsystem ID. (Any non-zero value)
[23:16]	Subsys2	RW	0x00	Subsystem ID. (Any non-zero value)
[15:8]	Subsys1	RW	0x01	Subsystem ID. (Any non-zero value)
[7:0]	Assembly	RW	0x00	Assembly ID. (Not applicable to CODEC vendors)

6.6. DAC0 Node (NID = 0x02)

6.6.1. DAC0 Cnvtr

Table 52. DAC0 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 53. DAC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz/44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 53. DAC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.6.2. DAC0 AmpRight

Table 54. DAC0 AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 55. DAC0 AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.6.3. DAC0 AmpLeft

Table 56. DAC0 AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 57. DAC0 AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.6.4. DAC0 WCap

Table 58. DAC0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 59. DAC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 59. DAC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.6.5. DAC0 PwrState

Table 60. DAC0 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 61. DAC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 61. DAC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.6.6. DAC0 CnvtrID

Table 62. DAC0 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 63. DAC0 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.6.7. DAC0 LR

Table 64. DAC0 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 65. DAC0 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.7. DAC1 Node (NID = 0x03)

6.7.1. DAC1 Cnvtr

Table 66. DAC1 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 67. DAC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 67. DAC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.7.2. DAC1 AmpRight

Table 68. DAC1 AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 69. DAC1 AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.7.3. DAC1 AmpLeft

Table 70. DAC1 AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 71. DAC1 AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.7.4. DAC1 WCap

Table 72. DAC1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 73. DAC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 73. DAC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.7.5. DAC1 PwrState

Table 74. DAC1 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 75. DAC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 75. DAC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.7.6. DAC1 CnvtrID

Table 76. DAC1 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 77. DAC1 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.7.7. DAC1 LR

Table 78. DAC1 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 79. DAC1 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.8. DAC2 Node (NID = 0x04)

6.8.1. DAC2 Cnvtr

Table 80. DAC2 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 81. DAC2 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 81. DAC2 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.8.2. DAC2 AmpRight

Table 82. DAC2 AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 83. DAC2 AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.8.3. DAC2 AmpLeft

Table 84. DAC2 AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 85. DAC2 AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.8.4. DAC2 WCap

Table 86. DAC2 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 87. DAC2 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 87. DAC2 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.8.5. DAC2 PwrState

Table 88. DAC2 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 89. DAC2 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 89. DAC2 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.8.6. DAC2 CnvtrID

Table 90. DAC2 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 91. DAC2 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.8.7. DAC2 LR

Table 92. DAC2 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 93. DAC2 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.9. DAC3 Node (NID = 0x05)

6.9.1. DAC3 Cnvtr

Table 94. DAC3 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 95. DAC3 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 95. DAC3 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.9.2. DAC3 AmpRight

Table 96. DAC3 AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 97. DAC3 AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.9.3. DAC3 AmpLeft

Table 98. DAC3 AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 99. DAC3 AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.9.4. DAC3 WCap

Table 100. DAC3 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 101. DAC3 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 101. DAC3 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.9.5. DAC3 PwrState

Table 102. DAC3 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 103. DAC3 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 103. DAC3 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.9.6. DAC3 CnvtrID

Table 104. DAC3 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 105. DAC3 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.9.7. DAC3 LR

Table 106. DAC3 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 107. DAC3 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.10. ADC0 Node (NID = 0x06)

6.10.1. ADC0 Cnvtr

Table 108. ADC0 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 109. ADC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 109. ADC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.10.2. ADC0 WCap

Table 110. ADC0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 111. ADC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved

Table 111. ADC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x1	Software should query the Processing Controls parameter for this widget.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.10.3. ADC0 ConLst

Table 112. ADC0 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 113. ADC0 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.

Table 113. ADC0 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	Coal	R	0x01	Number of NID entries in connection list.

6.10.4. ADC0 ConLstEntry

Table 114. ADC0 ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 115. ADC0 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x17	ADC0 Vol widget

6.10.5. ADC0 ProcState

Table 116. ADC0 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table
Set1	703	See bits [7:0] of bitfield table	0000_0000h

Table 117. ADC0 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

6.10.6. ADC0 PwrState

Table 118. ADC0 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 119. ADC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

6.10.7. ADC0 CnvtrID

Table 120. ADC0 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 121. ADC0 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.11. ADC1 Node (NID = 0x07)

6.11.1. ADC1 Cnvtr

Table 122. ADC1 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 123. ADC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.

Table 123. ADC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.11.2. ADC1 WCap

Table 124. ADC1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 125. ADC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x1	Software should query the Processing Controls parameter for this widget.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.11.3. ADC1 ConLst

Table 126. ADC1 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 127. ADC1 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.11.4. ADC1 ConLstEntry

Table 128. ADC1 ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 129. ADC1 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x18	ADC1 Vol widget

6.11.5. ADC1 ProcState

Table 130. ADC1 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table
Set1	703	See bits [7:0] of bitfield table	0000_0000h

Table 131. ADC1 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

6.11.6. ADC1 PwrState

Table 132. ADC1 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 133. ADC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

6.11.7. ADC1 CnvtrID

Table 134. ADC1 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 135. ADC1 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention, stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.12. SPDIFOut Node (NID = 0x08)

6.12.1. SPDIFOut Cnvtr

Table 136. SPDIFOut Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 137. SPDIFOut Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	FrmtNonPCM	RW	0x0	Stream Type 0 = PCM 1 = Non-PCM (remaining bits in this verb have other meanings)

Table 137. SPDIFOut Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.12.2. SPDIFOut WCap

Table 138. SPDIFOut WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 139. SPDIFOut WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0x4	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x1	Widget contains format info; software should query
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.12.3. SPDIFOut PCM

Table 140. SPDIFOut PCM Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 141. SPDIFOut PCM Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

6.12.4. SPDIFOut Stream

Table 142. SPDIFOut Stream Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table

Table 143. SPDIFOut Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

6.12.5. SPDIFOut CnvtrID

Table 144. SPDIFOut CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 145. SPDIFOut CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.12.6. SPDIFOut DigCnvtr

Table 146. SPDIFOut DigCnvtr Command Verb Format

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table
Set1	70D	See bits [7:0] of bitfield table	0000_0000h
Set2	70E	See bits [15:8] of bitfield table	0000_0000h

Table 147. SPDIFOut DigCnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	Rsvd1	R	0x0	Reserved
[14:8]	CC	RW	0x00	CC[6:0] - Category Code
[7]	L	RW	0x0	L - Generation Level
[6]	PRO	RW	0x0	PRO - Professional
[5]	AUDIO	RW	0x0	/AUDIO - Non-Audio
[4]	COPY	RW	0x0	COPY - Copyright
[3]	PRE	RW	0x0	PRE - Preemphasis
[2]	VCFG	RW	0x0	VCFG - Validity Config
[1]	V	RW	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

6.13. SPDIFIn Node (NID = 0x09)

6.13.1. SPDIFIn Cnvtr

Table 148. SPDIFIn Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 149. SPDIFIn Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	FrmtNonPCM	RW	0x0	Stream Type 0 = PCM 1 = Non-PCM (remaining bits in this verb have other meanings)
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 149. SPDIFIn Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.13.2. SPDIFIn WCap

Table 150. SPDIFIn WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 151. SPDIFIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0x4	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	Unsolicited Response is not supported

Table 151. SPDIFIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x1	Widget contains format info; software should query
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.13.3. SPDIFIn PCMCap

Table 152. SPDIFIn PCMCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 153. SPDIFIn PCMCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported

Table 153. SPDIFIn PCMCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10]	R11	R	0x0	192.0 KHz rate (4/1*48 KHz) NOT supported
[9]	R10	R	0x0	176.4 KHz rate (4/1*44.1 KHz) NOT supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x0	88.2 KHz rate (2/1*44.1 KHz) NOT supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

6.13.4. SPDIFIn Stream

Table 154. SPDIFIn Stream Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table

Table 155. SPDIFIn Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

6.13.5. SPDIFIn ConLst

Table 156. SPDIFIn ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 157. SPDIFIn ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.13.6. SPDIFIn ConLstEntry

Table 158. SPDIFIn ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 159. SPDIFIn ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x11	SPDIF In Pin widget.

6.13.7. SPDIFIn CnvtrID

Table 160. SPDIFIn CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 161. SPDIFIn CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.13.8. SPDIFIn DigCnvtr

Table 162. SPDIFIn DigCnvtr Command Verb Format

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table
Set1	70D	See bits [7:0] of bitfield table	0000_0000h
Set2	70E	See bits [15:8] of bitfield table	0000_0000h

Table 163. SPDIFIn DigCnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:15]	Rsvd2	R	0x0	Reserved
[14:8]	CC	R	0x00	CC[6:0] - Category Code
[7]	L	R	0x0	L - Generation Level
[6]	PRO	R	0x0	PRO - Professional

Table 163. SPDIFIn DigCnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	AUDIO	R	0x0	/AUDIO - Non-Audio
[4]	COPY	R	0x0	COPY - Copyright
[3]	PRE	R	0x0	PRE - Preemphasis
[2]	Rsvd1	R	0x0	Reserved (VCFG bit applies only to output streams)
[1]	V	R	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

6.14. PortA Node (NID = 0x0A)

6.14.1. PortA WCap

Table 164. PortA WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 165. PortA WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present

Table 165. PortA WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.14.2. PortA PinCap

Table 166. PortA PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 167. PortA PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.

Table 167. PortA PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement.
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.14.3. PortA ConLst

Table 168. PortA ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 169. PortA ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.14.4. PortA ConLstEntry

Table 170. PortA ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 171. PortA ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x02	DAC0 Converter widget

6.14.5. PortA PinWCntrl

Table 172. PortA PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 173. PortA PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = Enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.14.6. PortA UnsolResp

Table 174. PortA UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 175. PortA UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.14.7. PortA ChSense

Table 176. PortA ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 177. PortA ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.14.8. PortA ConfigDefault

Table 178. PortA ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 179. PortA ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x02	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x21	Configuration bits used by software to determine devices attached to the CODEC.

Table 179. PortA ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Config2	RW	0x40	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x20	Configuration bits used by software to determine devices attached to the CODEC.

6.15. PortB Node (NID = 0x0B)

6.15.1. PortB WCap

Table 180. PortB WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 181. PortB WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 181. PortB WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.15.2. PortB PinCap

Table 182. PortB PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 183. PortB PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.

Table 183. PortB PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.15.3. PortB ConLst

Table 184. PortB ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 185. PortB ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.15.4. PortB ConLstEntry

Table 186. PortB ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 187. PortB ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.

Table 187. PortB ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x04	DAC2 Converter widget

6.15.5. PortB PinWCntrl

Table 188. PortB PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 189. PortB PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x1	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.15.6. PortB UnsolResp

Table 190. PortB UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 191. PortB UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.15.7. PortB ChSense

Table 192. PortB ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 193. PortB ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.15.8. PortB ConfigDefault

Table 194. PortB ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24]of bitfield table	0000_0000h

Table 195. PortB ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x11	Configuration bits used by software to determine devices attached to the CODEC.

Table 195. PortB ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Config2	RW	0x60	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x11	Configuration bits used by software to determine devices attached to the CODEC.

6.16. PortC Node (NID = 0x0C)

6.16.1. PortC WCap

Table 196. PortC WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 197. PortC WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 197. PortC WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.16.2. PortC PinCap

Table 198. PortC PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 199. PortC PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.

Table 199. PortC PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.16.3. PortC ConLst

Table 200. PortC ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 201. PortC ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.16.4. PortC ConLstEntry

Table 202. PortC ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 203. PortC ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.

Table 203. PortC ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x03	DAC1 Converter widget

6.16.5. PortC PinWCntrl

Table 204. PortC PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 205. PortC PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x1	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.16.6. PortC UnsolResp

Table 206. PortC UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 207. PortC UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.16.7. PortC ChSense

Table 208. PortC ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 209. PortC ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.16.8. PortC ConfigDefault

Table 210. PortC ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 211. PortC ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x11	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x40	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x10	Configuration bits used by software to determine devices attached to the CODEC.

6.17. PortD Node (NID = 0x0D)

6.17.1. PortD WCap

Table 212. PortD WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 213. PortD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.17.2. PortD PinCap

Table 214. PortD PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 215. PortD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.17.3. PortD ConLst

Table 216. PortD ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 217. PortD ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved

Table 217. PortD ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.17.4. PortD ConLstEntry

Table 218. PortD ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 219. PortD ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x02	DAC0 Converter widget

6.17.5. PortD PinWCntrl

Table 220. PortD PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 221. PortD PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = Enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.17.6. PortD UnsolResp

Table 222. PortD UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 223. PortD UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.

Table 223. PortD UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.17.7. PortD ChSense

Table 224. PortD ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 225. PortD ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.17.8. PortD ConfigDefault

Table 226. PortD ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 227. PortD ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x02	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0xA1	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x90	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x50	Configuration bits used by software to determine devices attached to the CODEC.

6.18. PortE Node (NID = 0x0E)

6.18.1. PortE WCap

Table 228. PortE WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 229. PortE WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.18.2. PortE PinCap

Table 230. PortE PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 231. PortE PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.18.3. PortE PinWCntrl

Table 232. PortE PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 233. PortE PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x1	1 = CODEC input path of Pin Widget is enabled

Table 233. PortE PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	R	0x0	Vref Out not supported on this Port

6.18.4. PortE UnsolResp

Table 234. PortE UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 235. PortE UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.18.5. PortE ChSense

Table 236. PortE ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table

Table 237. PortE ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x0	No impedance sense for Port E.

6.18.6. PortE ConfigDefault

Table 238. PortE ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 239. PortE ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x81	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x30	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x51	Configuration bits used by software to determine devices attached to the CODEC.

6.19. PortF Node (NID = 0x0F)

6.19.1. PortF WCap

Table 240. PortF WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 241. PortF WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.19.2. PortF PinCap

Table 242. PortF PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 243. PortF PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.19.3. PortF ConLst

Table 244. PortF ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 245. PortF ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.19.4. PortF ConLstEntry

Table 246. PortF ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 247. PortF ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x05	DAC3 Converter widget

6.19.5. PortF PinWCntrl

Table 248. PortF PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 249. PortF PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = Enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	R	0x0	Vref Out not supported on this Port

6.19.6. PortF UnsolResp

Table 250. PortF UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 251. PortF UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.19.7. PortF ChSense

Table 252. PortF ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 253. PortF ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.19.8. PortF ConfigDefault

Table 254. PortF ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 255. PortF ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x11	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x60	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x12	Configuration bits used by software to determine devices attached to the CODEC.

6.20. DigOut0 Node (NID = 0x10)

6.20.1. DigOut0 WCap

Table 256. DigOut0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 257. DigOut0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No support for swapping left and right channels
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present

Table 257. DigOut0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.20.2. DigOut0 PinCap

Table 258. DigOut0 PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 259. DigOut0 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on this pin
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x0	Pin complex is not input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.

Table 259. DigOut0 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.20.3. DigOut0 ConLst

Table 260. DigOut0 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 261. DigOut0 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x03	Number of NID entries in connection list.

6.20.4. DigOut0 ConSelectCtrl

Table 262. DigOut0 ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 263. DigOut0 ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

6.20.5. DigOut0 ConLstEntry

Table 264. DigOut0 ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 265. DigOut0 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection
[23:16]	ConL2	R	0x19	ADAT Out Converter widget
[15:8]	ConL1	R	0x17	ADC0 Vol widget
[7:0]	ConL0	R	0x08	SPDIF Out Converter widget

6.20.6. DigOut0 PinWCntrl

Table 266. DigOut0 PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 267. DigOut0 PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5:0]	Rsvd1	R	0x0	Reserved

6.20.7. DigOut0 ConfigDefault

Table 268. DigOut0 ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 269. DigOut0 ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x45	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x10	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x30	Configuration bits used by software to determine devices attached to the CODEC.

6.21. DigIn Node (NID = 0x11)

6.21.1. DigIn WCap Command

Table 270. DigIn WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 271. DigIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x3	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x1	Power State control capability for support of EAPD
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.21.2. DigIn PinCap

Table 272. DigIn PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 273. DigIn PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x1	This widget controls EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on input pins.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable. (EAPD is not the output stream)
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.21.3. DigIn PwrState

Table 274. DigIn PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 275. DigIn PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - EAPD powered down (Hi-Z). 11 - Powered down (default)

6.21.4. DigIn PinWCntrl

Table 276. DigIn PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 277. DigIn PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

6.21.5. DigIn UnsolResp

Table 278. DigIn UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 279. DigIn UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon lock or loss-of-lock of SPDIF-in clock recovery circuit.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.21.6. DigIn ChSense

Table 280. DigIn ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h

Table 281. DigIn ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex. For this widget, Presence Detect indicates that the SPDIF-in clock recovery circuit has locked onto a valid SPDIF-in sampling frequency. Any change in status will generate an Unsolicited Response, if enabled with verb 708.
[30:0]	Rsvd	R	0x0	Reserved. Impedance sense not supported for this Pin Complex.

6.21.7. DigIn EAPD

Table 282. DigIn EAPD Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 283. DigIn EAPD Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd2	R	0x0	Reserved
[1]	Data	RW	0x0	EAPD value reflected on the EAPD pin. 0 = power down external amplifier; 1 = power up external amplifier if PwrState < 0x2. If PwrState > = 0x2, Pin47 is Hi-Z. An external pull-down is required if EAPD must be low when Pin Widget is powered down.
[0]	Rsvd1	R	0x0	Reserved

6.21.8. DigIn ConfigDefault

Table 284. DigIn ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 285. DigIn ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC. Port = no physical connection Location = internal, riser
[23:16]	Config3	RW	0xC5	Configuration bits used by software to determine devices attached to the CODEC. Default Device = SPDIF In Connection = optical
[15:8]	Config2	RW	0x10	Configuration bits used by software to determine devices attached to the CODEC. Color = black Misc = Jack detect override -- no external circuitry support for Presence Detect function
[7:0]	Config1	RW	0x60	Configuration bits used by software to determine devices attached to the CODEC.

6.22. ADC0Mux Node (NID = 0x12)

6.22.1. ADC0Mux WCap

Table 286. ADC0Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 287. ADC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.22.2. ADC0Mux ConLst

Table 288. ADC0Mux ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 289. ADC0Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x07	Number of NID entries in connection list.

6.22.3. ADC0Mux AmpCap

Table 290. ADC0Mux AmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 291. ADC0Mux AmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.22.4. ADC0Mux AmpRight

Table 292. ADC0Mux AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 293. ADC0Mux AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.22.5. ADC0Mux AmpLeft

Table 294. ADC0Mux AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 295. ADC0Mux AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.22.6. ADC0Mux ConSelectCtrl

Table 296. ADC0Mux ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 297. ADC0Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2:0]	Index	RW	0x0	Connection select control index. (Default = Port E)

6.22.7. ADC0Mux ConLstEntry0

Table 298. ADC0Mux ConLstEntry0 Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 299. ADC0Mux ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x0B	Port B
[23:16]	ConL2	R	0x0F	Port F
[15:8]	ConL1	R	0x15	CD In
[7:0]	ConL0	R	0x0E	Port E (default)

6.22.8. ADC0Mux ConLstEntry4

Table 300. ADC0Mux ConLstEntry4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table

Table 301. ADC0Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection.
[23:16]	ConL2	R	0x0A	Port A
[15:8]	ConL1	R	0x0D	Port D
[7:0]	ConL0	R	0x0C	Port C

6.23. ADC1Mux Node (NID = 0x13)

6.23.1. ADC1Mux WCap

Table 302. ADC1Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 303. ADC1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control

Table 303. ADC1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.23.2. ADC1Mux ConLst

Table 304. ADC1Mux ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 305. ADC1Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x07	Number of NID entries in connection list.

6.23.3. ADC1Mux AmpCap

Table 306. ADC1Mux AmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 307. ADC1Mux AmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.23.4. ADC1Mux AmpRight

Table 308. ADC1Mux AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 309. ADC1Mux AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.23.5. ADC1Mux AmpLeft

Table 310. ADC1Mux AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 311. ADC1Mux AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.23.6. ADC1Mux ConSelectCtrl

Table 312. ADC1Mux ConSelectCtrl Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 313. ADC1Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2:0]	Index	RW	0x1	Connection select control index. (Default = CD)

6.23.7. ADC1Mux ConLstEntry0

Table 314. ADC1Mux ConLstEntry0 Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 315. ADC1Mux ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x0B	Port B
[23:16]	ConL2	R	0x0F	Port F
[15:8]	ConL1	R	0x15	CD In
[7:0]	ConL0	R	0x0E	Port E

6.23.8. ADC1Mux ConLstEntry4

Table 316. ADC1Mux ConLstEntry4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table

Table 317. ADC1Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection.
[23:16]	ConL2	R	0x0A	Port A

Table 317. ADC1Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x0D	Port D
[7:0]	ConL0	R	0x0C	Port C

6.24. PCBEEP Node (NID = 0x14)

6.24.1. PCBEEP Amp

Table 318. PCBEEP Amp Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 319. PCBEEP Amp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x0	1 = Disable Digital PC Beep
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	Gain	RW	0x0	Mono (left) amplifier gain step number

6.24.2. PCBEEP WCap

Table 320. PCBEEP WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 321. PCBEEP WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x7	Widget type = Beep Generator
[19:4]	Rsvd1	R	0x0	Reserved
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	N/A
[0]	Stereo	R	0x0	Mono widget

6.24.3. PCBEEP AmpCap

Table 322. PCBEEP AmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 323. PCBEEP AmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x17	Size of each step in the gain range = 6 dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x03	Number of steps in the gain range = 4 (-18dB to 0dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x03	0dB-step is programmed with this offset

6.24.4. PCBEEP Gen

Table 324. PCBEEP Gen Command Verb Format

	Verb ID	Payload	Response
Get	F0A	00	See bitfield table
Set1	70A	See bits [7:0] of bitfield table	0000_0000h

Table 325. PCBEEP Gen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:0]	Divider	RW	0x0	Enable internal PC-Beep generation. Divider = 00h - disables internal PC Beep generation and enables normal operation of the CODEC. When the Divider is not 00h - generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency: F = (48 KHz HD Audio SYNC rate) / (4*Divider) producing tones from 47 Hz to 12 KHz (logarithmic scale). This part generates tones with frequency: F = 48000 * (257 - Divider) / 1024 yielding a linear range from 12 KHz to 93.75 Hz in steps of 46.875 Hz. If JackSenseVSR[Rate2x], then the beep tones generated have frequency: F = 48000 * (513 - Divider) / 1024 yielding a range of 24 KHz to 12093.75 Hz in steps of 46.875 Hz.

6.25. CD Node (NID = 0x15)

6.25.1. CD WCap

Table 326. CD WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 327. CD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.25.2. CD PinCap

Table 328. CD PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 329. CD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on this pin
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.25.3. CD PinWCntrl

Table 330. CD PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 331. CD PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

6.25.4. CD ConfigDefault

Table 332. CD ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 333. CD ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x90	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x33	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x00	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x52	Configuration bits used by software to determine devices attached to the CODEC.

6.26. VolumeKnob Node (NID = 0x16)

6.26.1. VolumeKnob WCap

Table 334. VolumeKnob WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 335. VolumeKnob WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x6	Widget type = Volume Knob Widget
[19:0]	Rsvd1	R	0x0	Reserved. Software assumes capability of unsolicited responses and a connection list for this widget type.

6.26.2. VolumeKnob VolKnobCap

Table 336. VolumeKnob VolKnobCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	13	See bitfield table

Table 337. VolumeKnob VolKnobCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Delta	R	0x1	Indicates if software can write a base volume to the Volume Control Knob.
[6:0]	NumSteps	R	0x7F	Total number of steps in the range of the volume knob = 128

6.26.3. VolumeKnob ConLst

Table 338. VolumeKnob ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 339. VolumeKnob ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x04	Number of NID entries in connection list.

6.26.4. VolumeKnob ConLstEntry

Table 340. VolumeKnob ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 341. VolumeKnob ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x05	DAC3
[23:16]	ConL2	R	0x04	DAC2
[15:8]	ConL1	R	0x03	DAC1
[7:0]	ConL0	R	0x02	DAC0

6.26.5. VolumeKnob UnsolResp

Table 342. VolumeKnob UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 343. VolumeKnob UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.26.6. VolumeKnob Cntrl

Table 344. VolumeKnob Cntrl Command Verb Format

	Verb ID	Payload	Response
Get	F0F	00	See bitfield table
Set1	70F	See bits [7:0] of bitfield table	0000_0000h

Table 345. VolumeKnob Cntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Direct	RW	0x0	Direct = 1 causes the volume control to directly control the hardware volume of the slave amps. Direct = 0 causes unsolicited responses to be generated.
[6:0]	Volume	RW	0x7F	Volume, specified in steps of amplifier gain

6.27. ADC0Vol Node (NID = 0x17)

6.27.1. ADC0Vol WCap

Table 346. ADC0Vol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 347. ADC0Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x1	Input amplifier is present
[0]	Stereo	R	0x1	Stereo widget

6.27.2. ADC0Vol ConLst

Table 348. ADC0Vol ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 349. ADC0Vol ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.27.3. ADC0Vol AmpRight

Table 350. ADC0Vol AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B00	00	See bitfield table
Set1	350	See bits [7:0] of bitfield table	0000_0000h

Table 351. ADC0Vol AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.27.4. ADC0Vol AmpLeft

Table 352. ADC0Vol AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	B20	00	See bitfield table
Set1	360	See bits [7:0] of bitfield table	0000_0000h

Table 353. ADC0Vol AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.27.5. ADC0Vol ConLstEntry

Table 354. ADC0Vol ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 355. ADC0Vol ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No Connection
[23:16]	ConL2	R	0x00	No Connection
[15:8]	ConL1	R	0x00	No Connection
[7:0]	ConL0	R	0x12	ADC0 Mux widget

6.27.6. ADC0Vol LR

Table 356. ADC0Vol LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 357. ADC0Vol LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.28. ADC1Vol Node (NID = 0x18)

6.28.1. ADC1Vol WCap

Table 358. ADC1Vol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 359. ADC1Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control

Table 359. ADC1Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x1	Input amplifier is present
[0]	Stereo	R	0x1	Stereo widget

6.28.2. ADC1Vol ConLst

Table 360. ADC1Vol ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 361. ADC1Vol ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.28.3. ADC1Vol AmpRight

Table 362. ADC1Vol AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B00	00	See bitfield table
Set1	350	See bits [7:0] of bitfield table	0000_0000h

Table 363. ADC1Vol AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.28.4. ADC1Vol AmpLeft

Table 364. ADC1Vol AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	B20	00	See bitfield table
Set1	360	See bits [7:0] of bitfield table	0000_0000h

Table 365. ADC1Vol AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.28.5. ADC1Vol ConLstEntry

Table 366. ADC1Vol ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 367. ADC1Vol ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No Connection
[23:16]	ConL2	R	0x00	No Connection
[15:8]	ConL1	R	0x00	No Connection
[7:0]	ConL0	R	0x13	ADC1 Mux widget

6.28.6. ADC1Vol LR

Table 368. ADC1Vol LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 369. ADC1Vol LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

7. ORDERING INFORMATION

7.1. STAC9220/9221/9223 Family Options and Part Order Numbers

The +4 V Analog voltage operation is supported by the +5 V version of the STAC9220/9221/9223.

*Dolby requires the 5 V version of this part except for Dolby Digital Live (DDL).

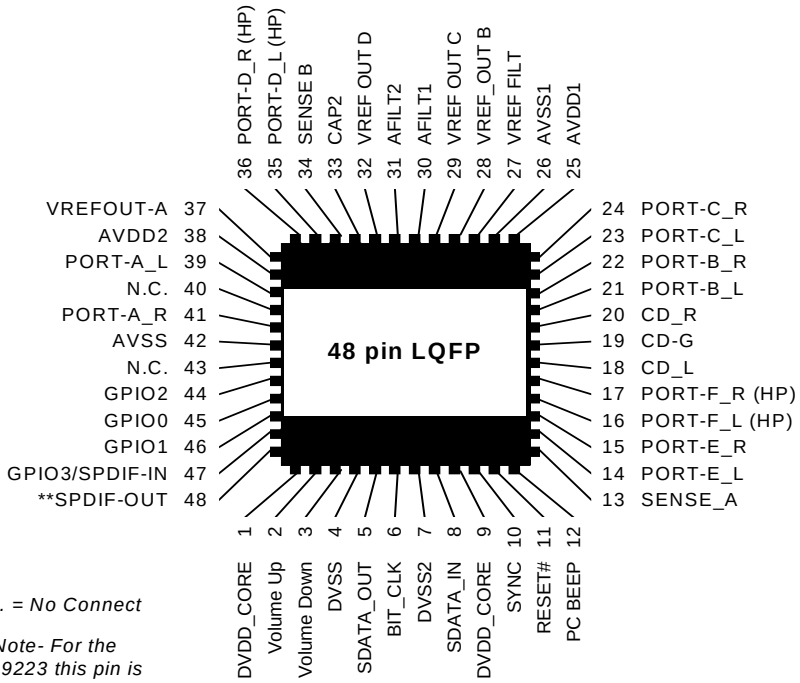
Table 370. STAC9220/9221/9223 Ordering Information

Part Order Number	Voltage	DAC SNR	I^2S	ADAT	Dolby*	Pkg Pins
STAC9220D5TAEyyX	5 V / 4 V	95dB	No	No	Yes	48 LQFP
STAC9220D3TAEyyX	3.3 V	95dB	No	No	Yes (DDL)	48 LQFP
STAC9220X5TAEyyX	5 V / 4 V	95dB	No	No	No	48 LQFP
STAC9220X3TAEyyX	3.3 V	95dB	No	No	No	48 LQFP
STAC9221D5TAEyyX	5 V / 4 V	105dB	Yes	Yes	Yes	48 LQFP
STAC9221D3TAEyyX	3.3 V	105dB	Yes	Yes	Yes (DDL)	48 LQFP
STAC9221X5TAEyyX	5 V / 4 V	105dB	Yes	Yes	No	48 LQFP
STAC9221X3TAEyyX	3.3 V	105dB	Yes	Yes	No	48 LQFP
STAC9223D5TAEyyX	5 V / 4 V	95dB	No	Yes	Yes	48 LQFP
STAC9223D3TAEyyX	3.3 V	95dB	No	Yes	Yes (DDL)	48 LQFP

NOTE: When ordering these parts the “yy” will be replaced with the CODEC revision. Add an “R” to the end of any of these part numbers for delivery on Tape and Reel. The minimum order quantity for Tape and Reel is 2,000 units for both package options.

8. PIN INFORMATION

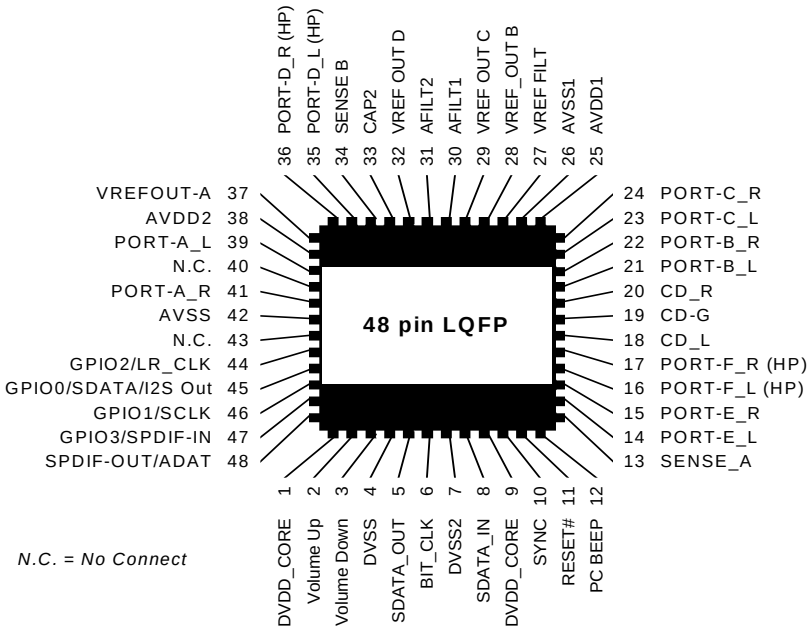
8.1. STAC9220/9223 Pin Diagram



N.C. = No Connect

*** Note- For the STAC9223 this pin is SPDIF_OUT/ADAT*

8.2. STAC9221 Pin Diagram



N.C. = No Connect

8.3. Pin Table for STAC9220/9223

Pin Name	Pin Function	I/O	Internal Pull-up /Pull-down	Pin Location
DVDD_CORE1	Digital Vdd = 3.3 V	I(Digital)	None	1
Volume Up	Volume Control	I(Digital)	Pull-Up	2
Volume Down	Volume Control	I(Digital)	Pull-Up	3
DVSS2	Digital Ground	I(Digital)	None	4
SDATA_OUT	HD Audio Serial Data output (inbound stream)	I/O(Digital)	None	5
BIT_CLK	HD Audio Bit Clock	I(Digital)	None	6
DVSS3	Digital Ground	I(Digital)	None	7
SDATA_IN	HD Audio Serial Data input (outbound stream)	O(Digital)	None	8
DVDD_CORE3	Digital Vdd = 3.3 V	I(Digital)	None	9
SYNC	HD Audio Frame Sync	I(Digital)	None	10
RESET#	HD Audio Reset	I(Digital)	None	11
PC BEEP	PC Beep	I(Analog)	None	12
Sense A	Jack insertion detection Ports A, B, C, D	I(Analog)	None	13
PORT-E_L	Input Left Channel Port E	I(Analog)	None	14
PORT-E_R	Input Right Channel Port E	I(Analog)	None	15
PORT-F_L (HP*)	Input/Output of Left DAC3	I/O(Analog)	None	16
PORT-F_R (HP*)	Input/Output of Right DAC3	I/O(Analog)	None	17
CD-L	CD Audio Left Channel	I(Analog)	None	18
CD-G	CD Audio Analog Ground	I(Analog)	None	19
CD-R	CD Audio Right Channel	I(Analog)	None	20
PORT-B_L	Input/Output of Left DAC2	I/O(Analog)	None	21
PORT-B_R	Input/Output of Right DAC2	I/O(Analog)	None	22
PORT-C_L	Input/Output of Left DAC1	I/O(Analog)	None	23
PORT-C_R	Input/Output of Right DAC1	I/O(Analog)	None	24
AVDD1	Analog Vdd = 5.0 V or 3.3 V	I(Analog)	None	25
AVSS1	Analog Ground	I(Analog)	None	26
VREF FILT	Analog Virtual Ground	O(Analog)	None	27
VREFOUT-B	Reference Voltage out drive (intended for microphone bias) for Port B	O(Analog)	None	28
VREFOUT-C	Reference Voltage out drive (intended for microphone bias) for Port C	O(Analog)	None	29
AFILT1	Anti-Aliasing Filter Cap-ADC left channel	O(Analog)	None	30
AFILT2	Anti-Aliasing Filter Cap-ADC right channel	O(Analog)	None	31
VREFOUT-D	Reference Voltage out drive (intended for microphone bias) for Port D	O(Analog)	None	32
CAP2	ADC reference Cap	O(Analog)	None	33
Sense B	Jack Insertion Detection Port E, F, G, H	I(Analog)	None	34

Pin Name	Pin Function	I/O	Internal Pull-up /Pull-down	Pin Location
PORT-D_L(HP)	Input/Output of Left DAC0	I/O(Analog)	None	35
PORT-D_R(HP)	Input/Output of Right DAC0	I/O(Analog)	None	36
VREFOUT-A	Reference Voltage out drive (intended for microphone bias) for Port A	O(Analog)	None	37
AVDD2	Analog Vdd = 5.0 V or 3.3 V	I(Analog)	None	38
PORT-A_L (HP)	Input/Output of Left DAC0	I/O(Analog)	None	39
NC	No Connect	N/C	None	40
PORT-A_R (HP)	Input/Output of Right DAC0	I/O(Analog)	None	41
AVSS3	Analog Ground	I(Analog)	None	42
NC	No Connect	O(Digital)	None	43
GPIO2	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 KΩ or more	44
GPIO0	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 KΩ or more	45
GPIO1	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 KΩ or more	46
GPIO3 / SPDIFIN	General Purpose I/O / SPDIF Input	I/O(Digital)	Pull-up 50 KΩ or more	47
SPDIF-OUT**	SPDIF digital output / ADAT (STAC9223 only)	O(Digital)	None	48

*Port F can drive 32 ohm headphones but is designed to provide less power than the headphone amplifiers on ports A and D.

**Note: For the STAC9223 this pin is SPDIF_OUT / ADAT

8.4. Pin Table for STAC9221

Pin Name	Pin Function	I/O	Internal Pull-up /Pull-down	Pin Location
DVDD_CORE1	Digital Vdd = 3.3 V	I(Digital)	None	1
Volume Up	Volume Control	I(Digital)	Pull-Up	2
Volume Down	Volume Control	I(Digital)	Pull-Up	3
DVSS2	Digital Ground	I(Digital)	None	4
SDATA_OUT	HD Audio Serial Data output (inbound stream)	I/O(Digital)	None	5
BIT_CLK	HD Audio Bit Clock	I(Digital)	None	6
DVSS3	Digital Ground	I(Digital)	None	7
SDATA_IN	HD Audio Serial Data input (outbound stream)	O(Digital)	None	8
DVDD_CORE3	Digital Vdd = 3.3 V	I(Digital)	None	9
SYNC	HD Audio Frame Sync	I(Digital)	None	10
RESET#	HD Audio Reset	I(Digital)	None	11
PC BEEP	PC Beep	I(Analog)	None	12
Sense A	Jack insertion detection Ports A, B, C, D	I(Analog)	None	13
PORT-E_L	Input Left Channel Port E	I(Analog)	None	14
PORT-E_R	Input Right Channel Port E	I(Analog)	None	15
PORT-F_L (HP*)	Input/Output of Left DAC3	I/O(Analog)	None	16
PORT-F_R (HP*)	Input/Output of Right DAC3	I/O(Analog)	None	17
CD-L	CD Audio Left Channel	I(Analog)	None	18
CD-G	CD Audio Analog Ground	I(Analog)	None	19
CD-R	CD Audio Right Channel	I(Analog)	None	20
PORT-B_L	Input/Output of Left DAC2	I/O(Analog)	None	21
PORT-B_R	Input/Output of Right DAC2	I/O(Analog)	None	22
PORT-C_L	Input/Output of Left DAC1	I/O(Analog)	None	23
PORT-C_R	Input/Output of Right DAC1	I/O(Analog)	None	24
AVDD1	Analog Vdd = 5.0 V or 3.3 V	I(Analog)	None	25
AVSS1	Analog Ground	I(Analog)	None	26
VREF FILT	Analog Virtual Ground	O(Analog)	None	27
VREFOUT-B	Reference Voltage out drive (intended for microphone bias) for Port B	O(Analog)	None	28
VREFOUT-C	Reference Voltage out drive (intended for microphone bias) for Port C	O(Analog)	None	29
AFILT1	Anti-Aliasing Filter Cap-ADC left channel	O(Analog)	None	30
AFILT2	Anti-Aliasing Filter Cap-ADC right channel	O(Analog)	None	31
VREFOUT-D	Reference Voltage out drive (intended for microphone bias) for Port D	O(Analog)	None	32
CAP2	ADC reference Cap	O(Analog)	None	33
Sense B	Jack Insertion Detection Port E, F, G, H	I(Analog)	None	34

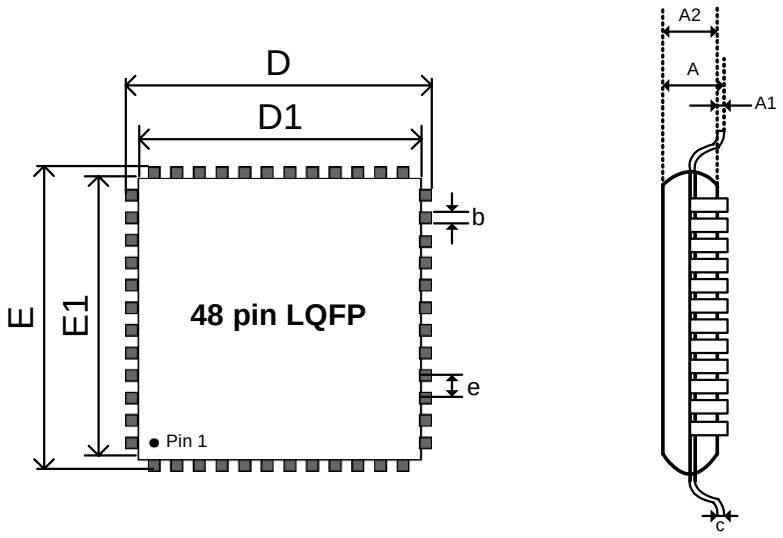
Pin Name	Pin Function	I/O	Internal Pull-up /Pull-down	Pin Location
PORT-D_L(HP)	Input/Output of Left DAC0	I/O(Analog)	None	35
PORT-D_R(HP)	Input/Output of Right DAC0	I/O(Analog)	None	36
VREFOUT-A	Reference Voltage out drive (intended for microphone bias) for Port A	O(Analog)	None	37
AVDD2	Analog Vdd = 5.0 V or 3.3 V	I(Analog)	None	38
PORT-A_L (HP)	Input/Output of Left DAC0	I/O(Analog)	None	39
NC	No Connect	N/C	None	40
PORT-A_R (HP)	Input/Output of Right DAC0	I/O(Analog)	None	41
AVSS3	Analog Ground	I(Analog)	None	42
NC	No Connect	O(Digital)	None	43
GPIO2 / LR_CLK	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 KΩ or more	44
GPIO0/SDATA / IS OUT	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 KΩ or more	45
GPIO1 / SCLK	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 KΩ or more	46
GPIO3 / SPDIFIN	General Purpose I/O/SPDIF Input	I/O(Digital)	Pull-up 50 KΩ or more	47
SPDIF-OUT/ADAT	SPDIF digital output / ADAT	O(Digital)	None	48

*Port F can drive 32 ohm headphones but is designed to provide less power than the headphone amplifiers on ports A and D.

9. PACKAGE DRAWINGS

9.1. 48-Pin LQFP

Figure 9. 48-Pin LQFP Package Outline and Package Dimensions



Key	LQFP Dimensions in mm		
	Min	Nom	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
L	0.45	0.60	0.75
e		0.50	
C	0.09	-	0.20
b	0.17	0.22	0.27

10. SOLDER REFLOW PROFILE

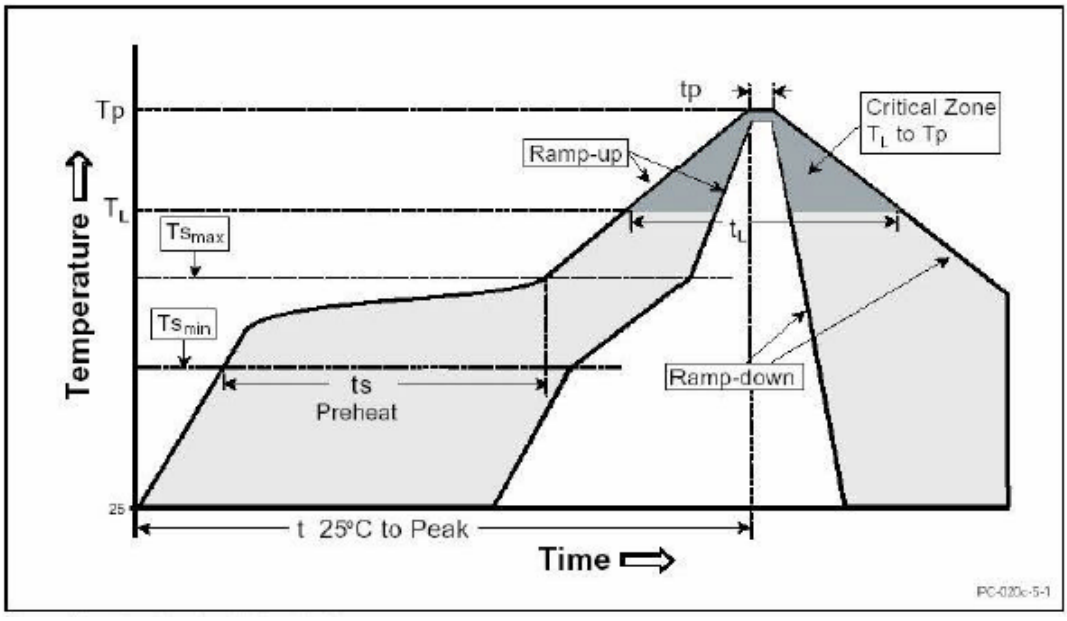
10.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices” (www.jedec.org/download).

Profile Feature		Pb Free Assembly
Average Ramp-Up Rate (Ts_{max} - Tp)		3 °C / second max
Preheat	Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} - ts_{max})	150 °C 200 °C 60 - 180 seconds
Time maintained above:	Temperature (T_L) Time (t_L)	217 °C 60 - 150 seconds
Peak / Classification Temperature (Tp)		See “Package Classification Reflow Temperatures” on page 170.
Time within 5 °C of actual Peak Temperature (tp)		20 - 40 seconds
Ramp-Down rate		6 °C / second max
Time 25 °C to Peak Temperature		8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.		

Figure 10. Solder Reflow Profile



10.2. Pb Free Process - Package Classification Reflow Temperatures

Package Type	MSL	Reflow Temperature
LQFP 48-pin	3	260 + 0 ^{o}C*

11. REVISION HISTORY

Revision	Date	Description of Change
		FOR STAC9220/9221REVISION CA1
0.5	September 2004	Initial Document
0.6	October 2004	Updated 9221 Block and Widget Diagram
0.7	November 2004	Updated Typical Connection Diagram- Fixed the D1 value for the JEDEC 48 pin drawing to say 6.90.
0.8	November 2004	Added Widget Information for CA1. Updated Block Diagrams. fixed Pin out. Updated Connection Diagrams.l
0.9	December 2004	Updated 9221 Block Diagram
0.91	January 2005	Updated 48 pin drawing. Updated Reflow Profile information.
		FOR STAC9220/9221/9223 REVISION CA2
0.92	January 2005	Added Widget information for STAC9220/9221 CA2.
0.93	February 2005	Added Ordering Information, Corrected Reflow profile Note, Added 9223 information.
0.94	July 2005	Added Power Consumption Tables. Added Performance Tables for 5V, 4V, and 3.3V Analog. Changed Note 4 on AC tables. Updated ESD statement.
		FOR STAC9220/9221/9223 All Revisions
0.95	January 2006	Updated IDT logo. Added ADAT logo. Added “Audio Jack Presence Detect” section.
0.96	27 October 2006	Released in IDT format.

Innovate with IDT audio for high fidelity. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
HA.CM@idt.com

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339